Ryerson University

Department of Electrical & Computer Engineering
Faculty of Engineering & Architectural Science

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*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a “0” on the work, an “F” in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: http://www.ryerson.ca/senate/current/pol60.pdf

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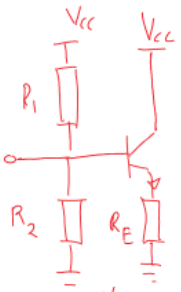
Amplifier Design Choice

The multistage configuration of the amplifier was chosen as CC -> CE -> CC. The first CC stage is there to easily meet the requirements for a high enough input resistance. The final CC stage is there to ensure a low enough output resistance to drive a small load without significantly hurting the gain of the amplifier. The CE amplifier was chosen to meet the specified voltage gains and thus the amplifier will be an inverting amplifier.

Manual Calculations

Note: Assumption made from prelab 7 for the value of beta. Using Beta = 150 for all calculations.

Input CC stage



$R_{in} = \frac{V_T}{I_B} + (\beta+1) R_E \,||\, R_1 \,||\, R_2$

$R_E > \left[20k - \frac{V_T}{I_B}\right] \div (\beta+1)$

Set I_B to be small, $I_B = 5\mu A$

$R_E > \left[100k - \frac{0.026}{5\mu A}\right] / (151)$

$R_E > 632$, set $R_E = 1k\Omega$ so $\frac{V_T}{I_B} + (\beta+1)R_E = 5200 + 151k = 156\,200\Omega$

$I_E = \beta I_B = 150(5\times10^{-6}) = 0.75mA$

$V_E = R_E I_E = 1k(0.75mA) = 0.75V$

$V_B = V_E + 0.7 = 1.45V$

$V_B = \frac{10 R_2}{R_1 + R_2}$

$\frac{1.45}{10} = \frac{R_2}{R_1 + R_2} \rightarrow R_2 = 5.9 R_1$

set $R_1 = 30k$, $R_2 = 177k$

$\frac{1}{R_{in}} = \frac{1}{30} + \frac{1}{177} + \frac{1}{156.2}$

$R_{in} = 156k \,||\, 30k \,||\, 177k = \boxed{22k}$

Figure 1. Biasing calculation for first stage (CC)

Calculation explanation:

According to the formula of the input resistance of the CC amplifier, an expression for the R_E was derived in terms of I_B such that the internal resistance of the amplifier would be at least 20k. This way, the input resistance can be easily controlled by the parallel combination of the DC bias network. Next, to meet the DC current draw, a small enough I_B was chosen such that 20K - V_T/I_B would not be negative and that the resulting I_E would be < 1mA to stay well below the current requirement. The value of R_E was chosen to be 1k resulting in the internal resistance of the amplifier to be 156.2k. R_1 was set to be 30k so that the resultant parallel combination would be less than 30k ohms. Calculating internal resistance gave 22k which meets the design requirements.

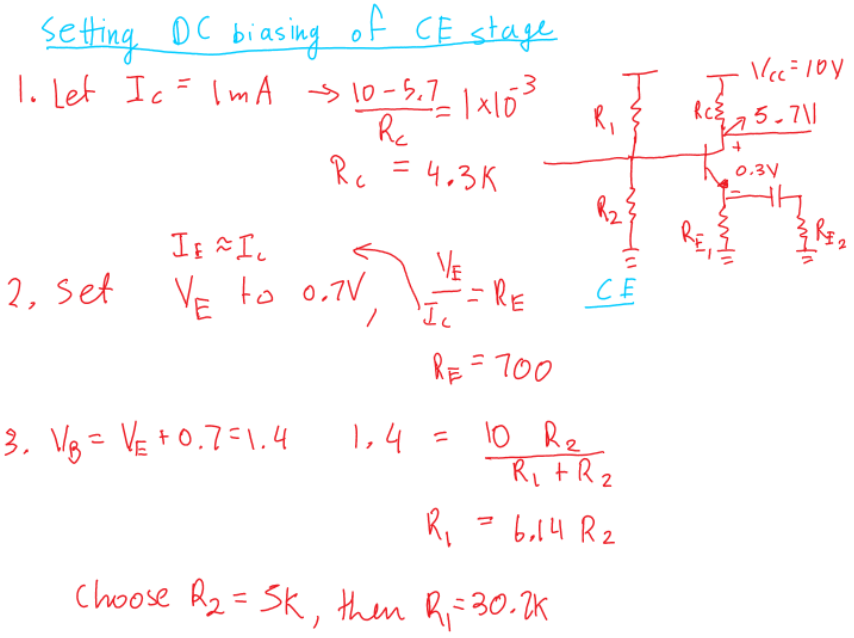


Figure 2. Biasing calculation for second stage (CE)

Calculation explanation:

To set the DC parameter for CE, a small I_C current to stay under the current requirement was chosen first. The biasing voltage at Rc was chosen at 5.7V since the CE stage and the output CC stage are DC coupled. This makes it so that the final CC stage won't need the DC voltage divider network. At a 5.7V CE bias, the V_{BE} drop on the CC stage would result in V_{Out} biasing at 5V, leaving enough room for the swing to be 8 Vpp. The V_E was chosen to allow for the max swing on the CE stage. Max swing is Vcc-$V_{CE,Sat}$ = 10 - (V_E + 0.3). This value should be minimum 8V so V_E was chosen such that Vcc - $V_{CE,Sat}$ = 9V. Using the known current and voltage, the value of R_E was determined using ohm's law, V_B was also calculated after the value of V_E was determined. Using voltage division, R_1 and R_2 were determined to set V_B at 1.4V. Any resistance values of R_1 and R_2 should suffice as long as the ratio was met, thus I arbitrarily chose 5k to be R_2 and R_1 = 30.7k.

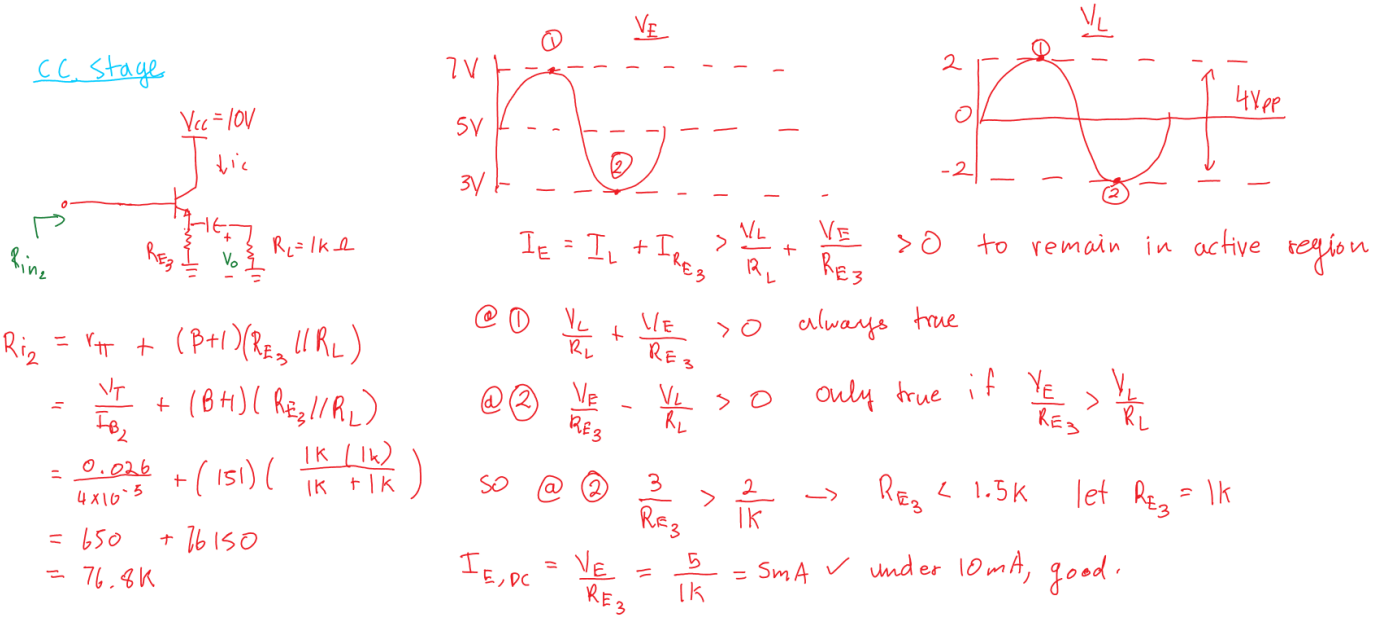


Figure 3. Resistance calculation for Output CC stage

Calculation explanation:

After testing the CC stage in multisim, it was found that the transistor was going into cutoff mode, causing heavy clipping. After analyzing, the reason for the cutoff was that R_{E3} was too high. As highlighted in the analysis above, the cutoff mode was prevented by using a smaller R_{E3} at the price of higher current usage. However, the current usage still falls under the DC requirement, making the current solution valid. The input resistance was calculated using the standard equation for the input resistance of the transistor.

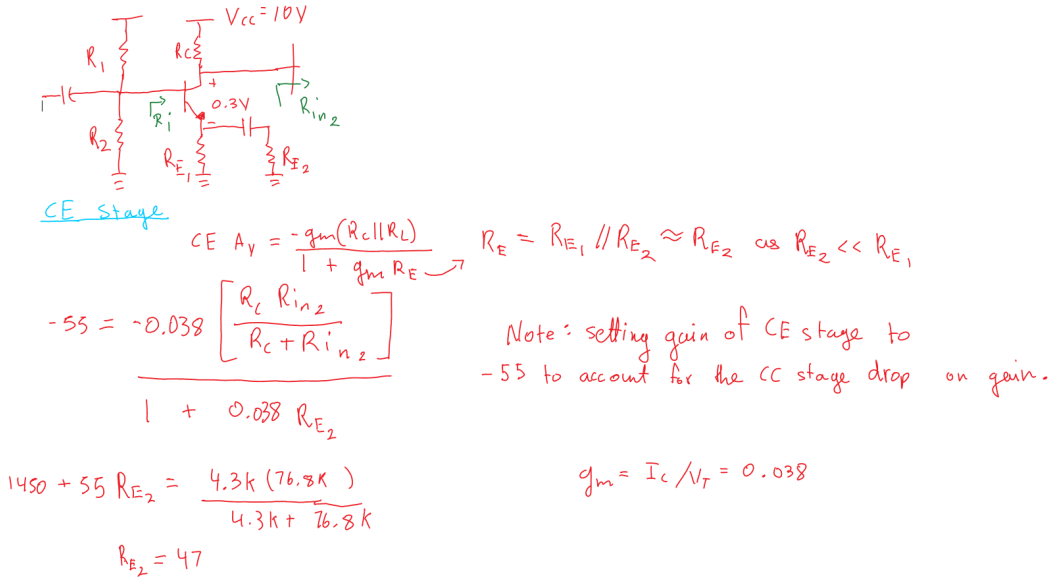


Figure 4. Gain calculation for CE stage

Calculation explanation:

The gain of CE was calculated with the load being the input resistance of the output CC stage. Using the formula helped determine the exact value of R_{E2} to achieve the following gain. Also, as stated in the calculations, the gain of CE amplifier was set to -55 to account for the drop in gain from the CC stage and other possible deviations. It was set to -55 so that even after the drops, the gain would still fall in between -50 ± 5. Also the assumption of $R_{E2} << R_{E1}$ holds true as 47 << 700, making the calculation accurate.

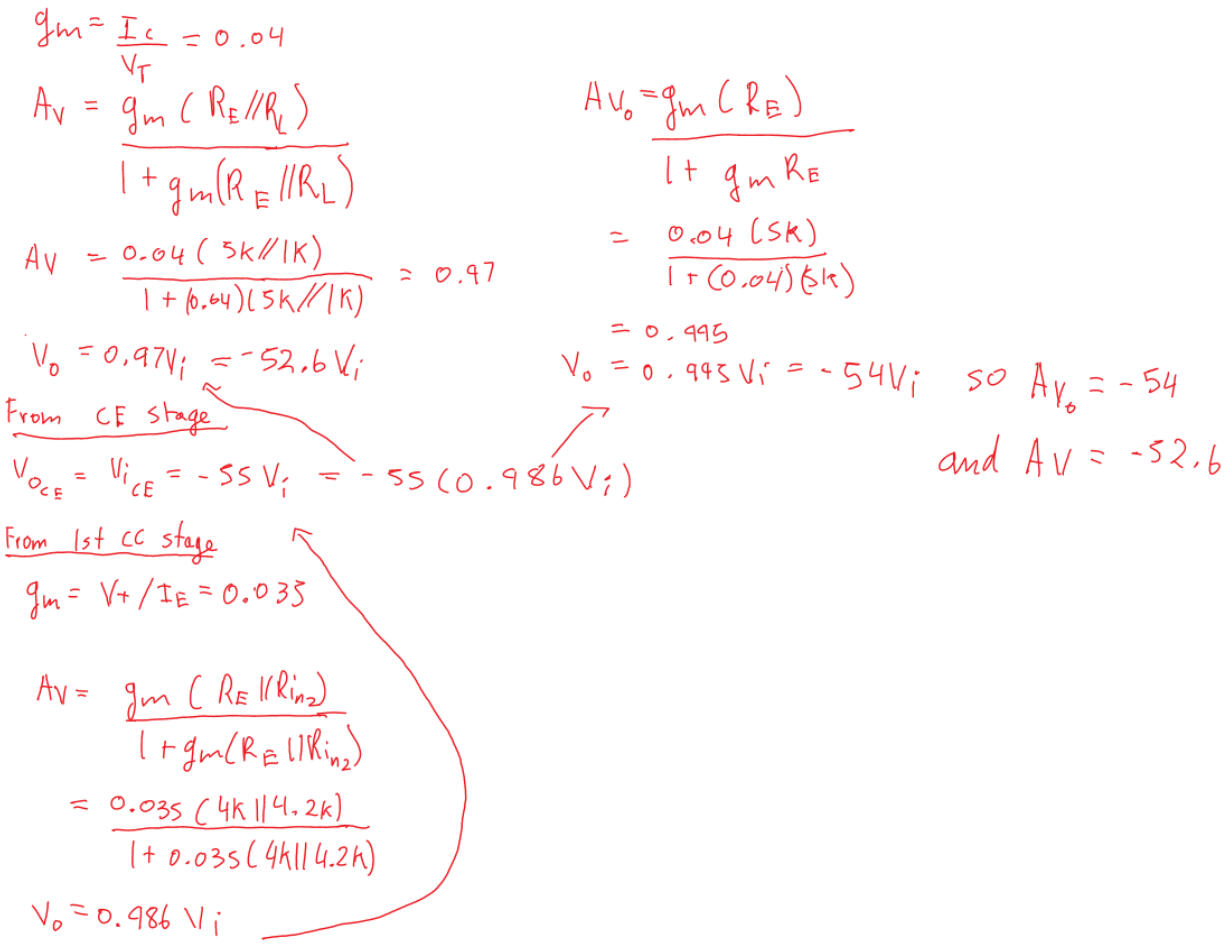


Figure 5. Overall gain calculation (From 3rd stage)

Calculation explanation:

The calculation for the overall gain accounts for the loading impact of each stage. The gain of the first stage is dependent on input resistance of the second stage and the gain of the second stage is dependent on the gain of the third stage. Thus, the gains of each stage were calculated and cascaded into the gain equations of other stages to find the overall gain of the third stage.

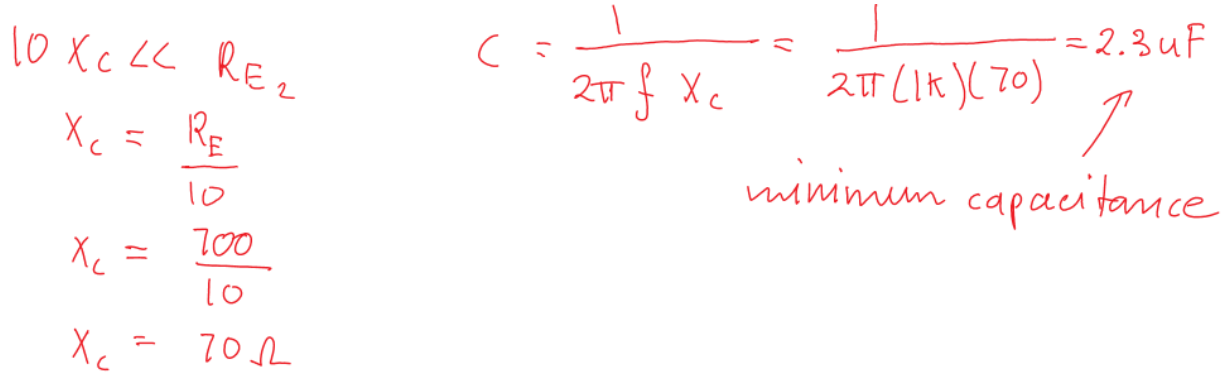


Figure 6. Bypass capacitance calculation

Capacitance value justification:

The role of the capacitors in the circuit configuration is to act as open in DC and short in AC. As capacitance is inversely proportional with impedance, all capacitance values were made to be as big as permitted with the exception of R_{E2} bypass capacitor. Having 220uF capacitors would ensure minimal possible resistance in AC. However, capacitance needs to be at least 2.3uF to be big enough to act as a bypass capacitor in the CE amplifier. The other capacitors will have minimum required capacitance value to be less than 2.3uF as the resistances in series with those capacitors are much larger. The bypass capacitor on R_{E2} has a direct impact on the gain and thus the frequency response of the whole circuit. Using multisim AC sweep, the value of the bypass capacitor was found to be approximately 110uF which would allow it a frequency response of -3dB.

Simulation Results

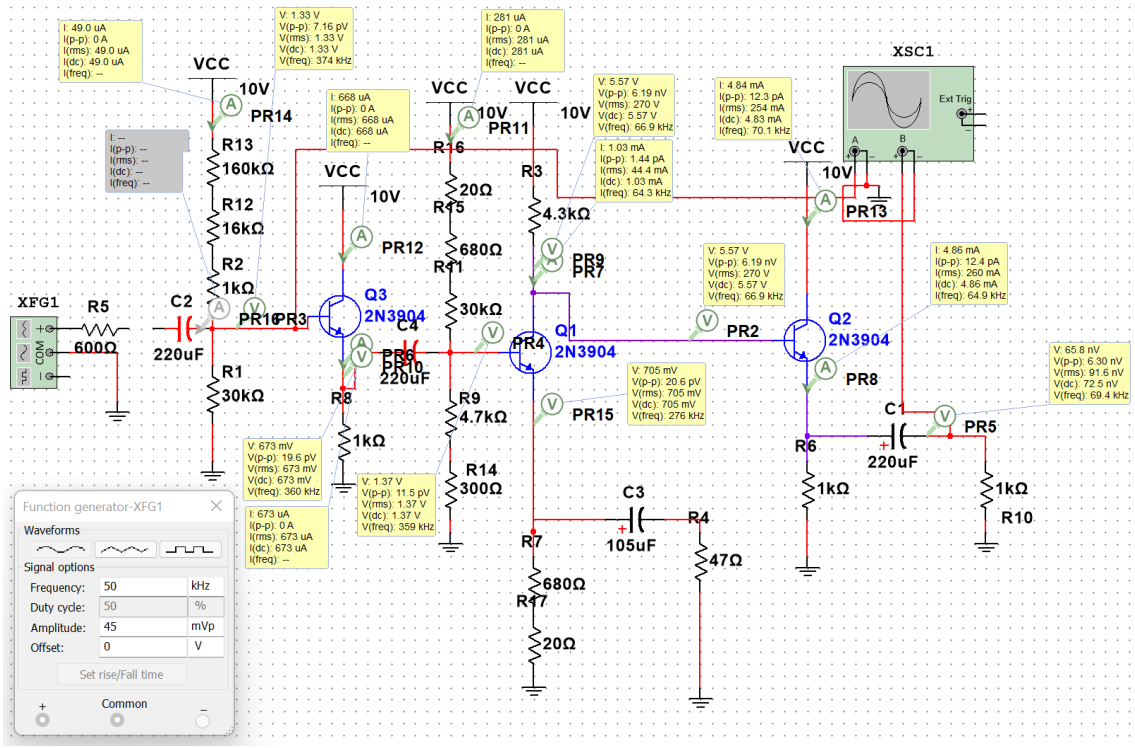


Figure 7. Simulated DC biasing values

DC current requirement (I < 10mA)

Sum of all DC currents provided by power supply is:

49uA + 668uA + 281uA + 1.03mA + 4.84mA = 6.9mA < 10mA. Meets requirements.

A_{Vo} gain (A_{VO} = 50 ± 5) and 8Vpp requirement

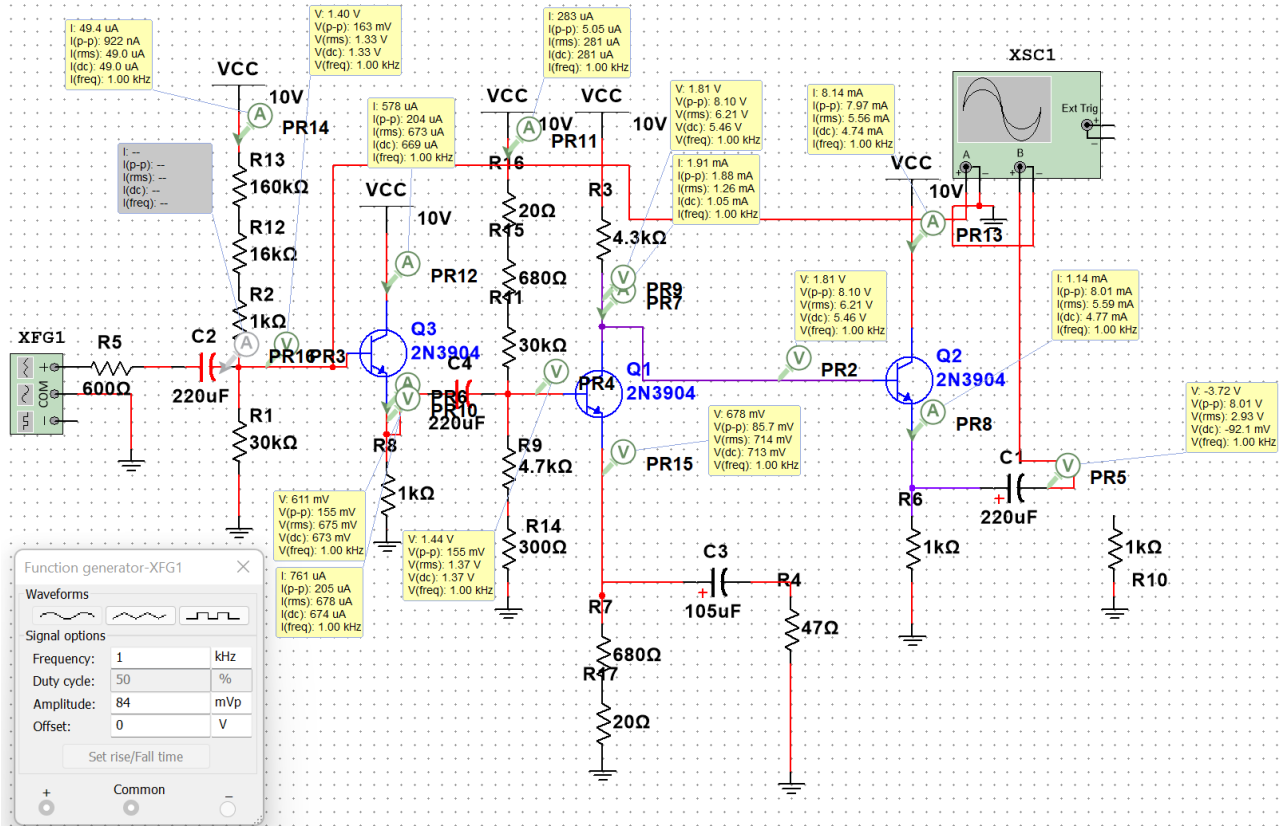


Figure 8. No load voltage gain simulation circuit

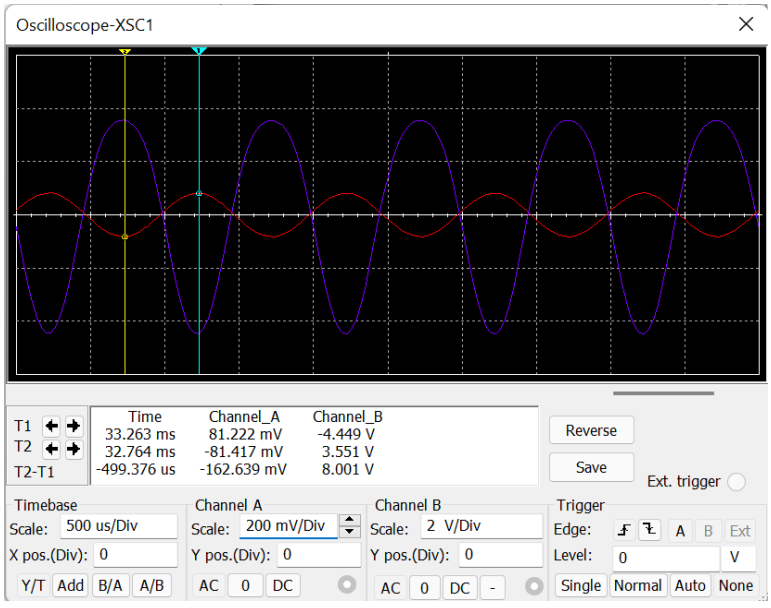


Figure 9. No load voltage gain simulation graph

$|A_{Vo}| = |V_{Out}/V_{in}| = 8.01/163mV = 49.1 = 50 \pm 10\%$

Thus $|A_{Vo}|$ meets the requirements. Also, the peak to peak voltage indicated by the voltage probe reads 8Vpp showing that the 8Vpp requirement is met.

Av gain (Av > 0.9A_{Vo} → Av > 44.226), 4Vpp requirement and Rin requirement

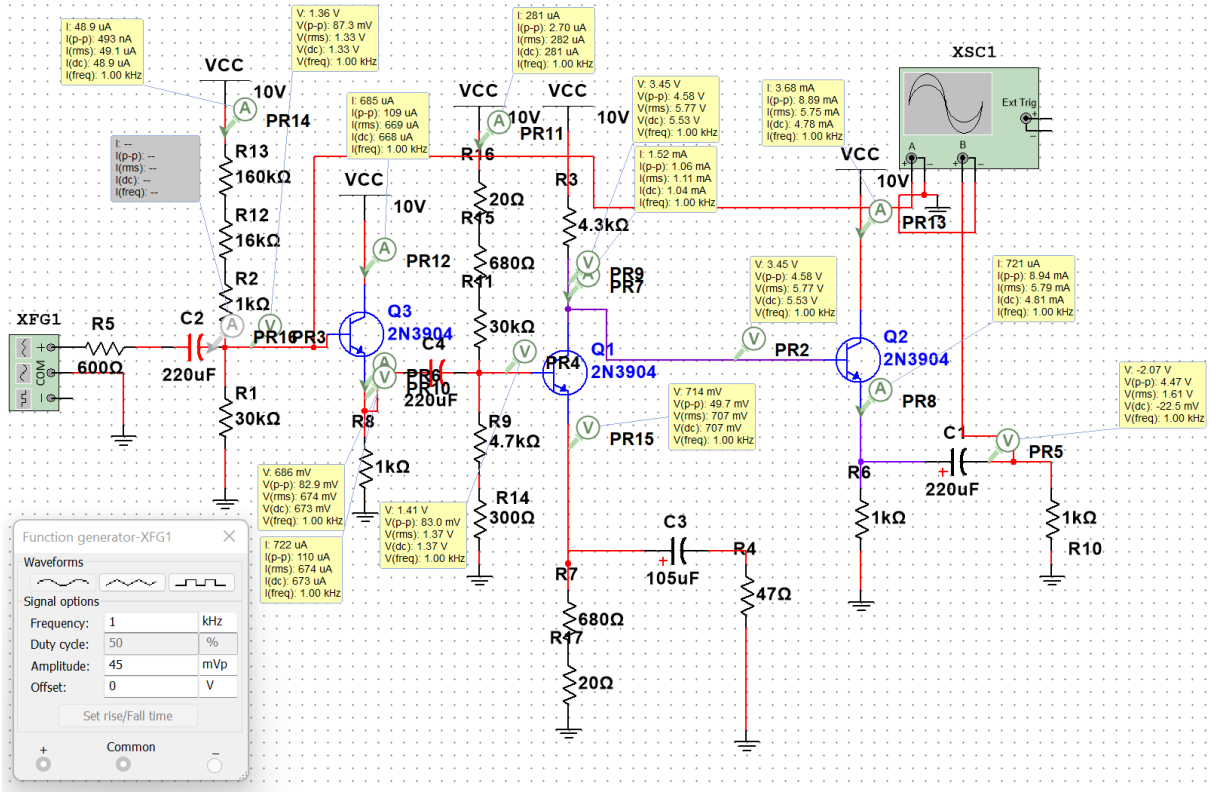


Figure 10. Loaded voltage gain simulation circuit

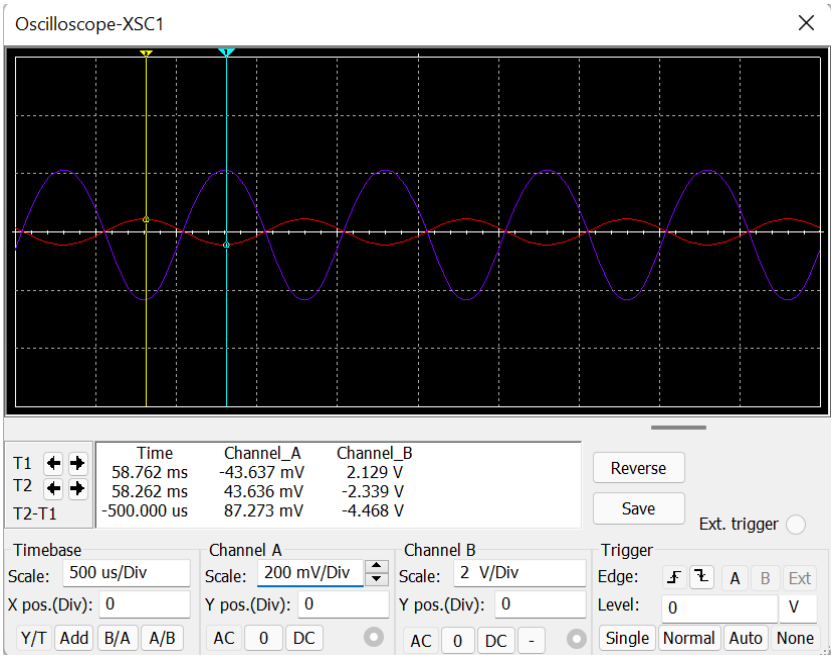


Figure 11. Loaded voltage gain simulation graph

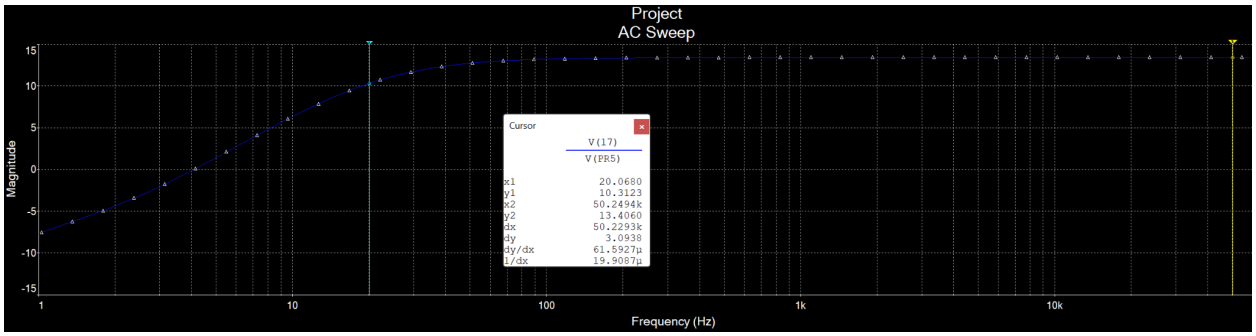
$|A_V| = V_{Out}/V_{in}$ = 4.47/87.3mV = 51.2 > 44.226

Thus, $|A_V|$ meets the requirements. Also, the peak to peak voltage indicated by the voltage probe reads 4.47Vpp showing that the 8Vpp requirement is met.

$R_{in} = V_{in}/I_{in}$ = 87.3mV/ 4.09uA = 21.3k

Thus, R_{in} also meets the requirement of being at least 20k.

Frequency Response requirement (-3db)



As y2 - y1 = 13.4 - 10.3 = 3.1 the configuration meets the -3db frequency response requirement.

<u>Accuracy and Deviations Justification</u>

	R_{in}	$V_{B,stage1}$	$V_{B,stage2}$	$V_{B,stage3}$	$I_{C,stage1}$	$I_{C,stage2}$	$I_{C,stage3}$	A_{Vo}	A_V
Calculated	22k	1.45	1.4	5.7V	0.75mA	1mA	5mA	-54	-52.6
Measured	21.3k	1.33	1.37	5.57V	0.67mA	1.03mA	4.84mA	-49.1	-51.2

Table 1. Comparison for any possible deviations between calculated and measured values

All values are accurate to the calculations. The small deviations in the measurements and calculations can be justified with uncertainty in the beta value as it was just taken from lab 7, approximations made in the calculations and also rounding done in the calculations. An unexpected thing to note is that the unloaded voltage gain was actually smaller than the voltage gain. This obviously does not make sense, however after playing around with input voltages, it was found that the gain is dependent on the input voltage and decreases with higher input voltages. The only explanation I can think of for this is that as the voltage swing approaches the upper and lower limits, the circuit becomes increasingly unstable which may in turn lower the gains. This probably also explains why there is a higher deviation from the calculated A_{Vo} compared to the A_V.