CSE216: Computer Organization and Architecture

Programme: B.Tech. (CSE, CCE) Year: 2 Semester: 3
Course: Core Credits: 4 Hours: 40 lecture + 20 lab

Course Context and Overview:
The course aims to provide a basic understanding of a digital computer. The course will familiarize students with the von Neumann architecture. Functioning of processors, trends and issues in modern processors will be discussed (pipelining, performance etc.). The course will cover memory hierarchy including cache and virtual memory. Different ways of communicating with I/O devices and concept of bus system within the computer will be studied. The course will also discuss the design of an instruction set and how instructions are executed, along with identifying different addressing modes.

Prerequisites Courses:
Basic Electronics

Course outcomes (COs):

On completion of this course, the students will have the ability to:
CO1 Describe the organization of a typical computer and internal representation of data
C02 Design processor architecture including datapath, control unit and instruction set
C03 Explain instruction level parallelism
C04 Describe and demonstrate memory hierarchy
C05 Describe interfacing and communication mechanisms with I/O devices and functional units.

Course Topics:

Topics	Contact Hours	
UNIT - I **1. Introduction:**		4 + 2
1.1 Introduction to computers	1	
1.2 Data representation and arithmetic	2	
1.3 RISC/CISC, Superscalar architecture, Array and vector processors, Multiprocessors, Multicomputers, advanced processors, Flynn taxonomy	1	

1.4 Lab	2	
UNIT – II **2. Instruction Set Architecture:**		13 + 8
2.1 Memory models, Registers	1	
2.2 Instruction types	1	
2.3 Instruction formats	1	
2.4 Addressing modes	1	
2.5 Expanding opcodes	2	
2.6 Flow of control: Sequential, Branching, Co-routines, Traps, Interrupts, I/O	3	
2.7 Lab	2	
3. Assembly language:		
3.1 Introduction to assembly language	1	
3.2 Pseudoinstructions, Macros	1	
3.3 Assemblers, Symbol Table, Linkers, Loaders	2	
3.4 Lab	6	
UNIT – III **4. Central Processing Unit:**		8 + 4
4.1 Instruction execution cycle	1	
4.2 Data Path	1	
4.3 Control Unit: hardwired, microprogrammed	2	
4.4 Performance, benchmarks	1	
4.5 Lab	2	
5. Pipelining:		
5.1 Pipelines: branch prediction, speculative execution, out of order execution; hazards	3	
5.2 Lab	2	
UNIT-IV **5. Memory system:**		8 + 4
5.1 Storage systems: Magnetic disks, CDs, Blu-Ray, RAID; Memory hierarchy	1	
5.2 Byte ordering	0.5	
5.3 Error correcting codes	0.5	
5.4 Cache memory: principle of locality, main memory to cache mapping, cache coherence	2	
5.5 Virtual memory: Paging, page replacement, segmentation, fragmentation, TLB	3	
5.6 Memory and cache performance metrics	1	
5.7 Lab	4	
UNIT – V **6. Bus System:**		7 + 2
6.1 Bus width, bus clocking	1	
6.2 Bus arbitration	2	
6.3 Bus operations	1	

6.4 Lab	2	
7. I/O interfacing:		
7.1 Handshaking, buffering, programmed I/O, interrupt driven I/O	1	
7.2 Interrupt structures: vectorized, prioiritized, interrupt acknowledgment	1	
7.3 Interrupt handling, DMA	1	

Textbook references:
Text Book:
A.S. Tanenbaum, *Structured Computer Organization*, 5th ed. Prentice Hall, 2005.
Carl Hamacher, Zvonko Vranesic, Safwat Zaky, *Computer Organization*, 5th ed. McGraw Hill, 2002.

Reference books:
D.A. Patterson and J.L. Hennessy, *Computer Architecture: Hardware/Software Interface*, 4th ed. Morgan Kaufmann, 2011.

Evaluation Methods:

LECTURE	
Component	**Weightage**
Quiz/Assignments	20%
Midterm	30%
Final Examination	50%
LAB	
Component	**Weightage**
Regular assessment	40%
Endterm	60%

NOTE: 75% weightage will be given to lecture component marks and 25% to lab component marks for final grading

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