THE LNM INSTITUTE OF INFORMATION TECHNOLOGY

COA MID-TERM (2016-2017)

MAX MARKS: 30 **TIME: 90 MINS**

Q1 Suppose there exists one uniprocessor machine which can use either of two different instruction sets i.e. one-address instruction set (Eg. MOVE R_i, ADD R_i, MUL R_i etc.) **OR** zero-address instruction set (Eg. PUSH A, ADD etc).

a) Write two different programs (using these two different instruction sets) for the given set of statements (2+2=4)

$v = a + b$

$w = b * 2$

$x = v - w$

$y = v + w$

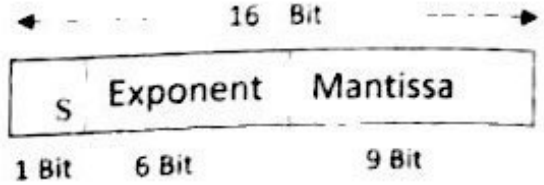
$z = x * y$

(b) Compare their performance if Clock cycles per Instruction (CPI) for one-address instruction set is 2.0 and for zero-address instruction set is 1.2 (2)

(c) Is it possible to ensure parallelism using this machine? Justify your answer (1)

Q2 How many carry-save addition levels are required to reduce 16 summands using 3-2 carry save addition method? Explain using diagram. (2)

Q3 Perform addition of the given numbers A and B. Use two guard bits and round-off the result using von-Neumann method. The following modified format of numbers following IEEE floating point numbers with excess-31 coding is used (5)



A = 0 100001111111110
B = 0 011111 001010101

Q4. A digital computer has a memory unit with 32 bits per word. The instruction set consists of 110 different operations. All instructions have an operation code part (opcode) and two address fields: one for a memory address and one for a register address. This particular system includes eight general-purpose registers. Registers may be loaded directly from memory, and memory

may be updated directly from the registers. Direct memory-to-memory data movement operations are not supported. Each instruction is stored in one word of memory. Justify all your answers.

a) How many bits are needed for the opcode? (5)

b) How many bits are needed to specify the register?

c) How many bits are left for the memory address part of the instruction?

d) What is the maximum allowable size for memory?

e) What is the largest unsigned binary number that can be accommodated in one word of memory?

Q5 Consider the following assembly language code: (1+1+2+2+2=8)

```
        Load R1, 2000        //Assume 2000 location contains value 3
        Mov R0, #0
        Mov R2, #1
Loop:   Add R0, R0, R2       //First operand is destination register
        Add R2, R2, #1       //Statement 1
        Sub R1, R1, #1
        Jnz loop
```

a) What is the final output?

b) For Statement 1, can you think of an alternative instruction which can convert the dyadic instruction into a monadic instruction?

c) Assume memory access and control transfer instructions are 4 bytes long, data transfer instructions are 2 bytes long, arithmetic instructions are 3 bytes long. Construct the symbol table.

d) Assume memory access instructions take 5 cycles to execute, data transfer instructions and arithmetic operations take 1 cycle and control transfer operations take 3 cycles. How many cycles are required by the program?

e) If the clock frequency is 4 Ghz, compute time required by the program to run.

Q6. Multiply 13 and -6 using Booth's algorithm. (3)