LNM INSTITUTE OF INFORMATION TECHNOLOGY

COA END-TERM PAPER (2012-2013, 1st Semester)

MAX MARKS: 100 **TIME: 3 hours**

Q1. Give one line answers. (10 x 1=10)

(a) Full form of the acronym MMX.

(b) A large number of identical processors performing same sequence of instructions on different datasets.

(c) Principle on which caches are based on.

(d) The set of tracks at a given radial position in a magnetic disk.

(e) The time taken by the arm in a magnetic disk to move to the right radial position.

(f) The problem of signal on different lines of a bus traveling at slightly different speeds.

(g) The number of 1M x 1 RAM chips required to have a 4MB memory.

(h) Commands to the assembler itself.

(i) The problem of wasted bytes in pages of a virtual memory.

(j) The device for doing the virtual-to-physical mapping for a virtual memory.

Q2. Generate an even parity Hamming code for the listed ASCII characters. Show all steps. (6)

A 100 0001

B 100 0010

C 100 0011

Q3. A computer is available without a program counter. Instead, all instructions contain three parts: an operation code, memory address of an operand and address of next instruction. The operation code consists of 6 bits and the computer has a memory unit of 8192 words. How many bits must be in a memory word if an instruction is stored in one word? Show the instruction word format. (4)

Q4. Write a program to evaluate the given arithmetic statement using a stack organized computer with zero-address operation instructions. X= (A+B*C)/(D-E*F+G*H) (5)

Q5. A virtual memory system has an address space of 8K words, a memory space of 4K words and page and block sizes of 1K words. The following page reference changes occur during a given time interval.

4 2 0 1 2 6 1 4 0 1 0 2 3

Determine the four pages that are resident in main memory after EACH page reference if the replacement algorithm used is (a) FIFO (b) LRU. Give in table form (Page reference / Resident pages). Also specify the number of page faults in each case. (3 + 3 = 6)

Q6. An 8-bit computer has a register R. Determine the value of overflow flag V, carry flag C, sign flag S and zero flag Z after each of the following instruction. The initial value of register R in each case is (72) H. Assume numbers are unsigned. (2+2+2=6)

(a) Add immediate operand (C6)H to R.

(b) Add immediate operand (1E)H to R.

(c) Exclusive-OR R with R.

Q7. A computer has a memory unit with 32-bit address and a cache memory of 1K words. The cache uses direct mapping with a block size of eight words (word size =32 bits). (3+2+2=7)

(a) How many bits are there in tag, index and word fields of the address format?

(b) How many total bits are contained in this cache? Include a valid bit.

(c) To what block number will memory word address 1800 map to?

Q8. A digital camera has a resolution of 3000 x 2000 pixels, with 3 bytes/pixel for RGB color. The manufacturer of the camera wants to be able to write a JPEG image at a 5x compression factor to the flash memory in 2 sec. What data rate is required? (4)

Q9. Discuss the data hazards encountered by a pipeline. Outline ways of dealing with them. (5)

Q10. The logical address space in a computer system consists of 1024 words, eight virtual pages. The physical memory consists of four page frames. Formulate the logical to physical address mapping. (5)

Q11. Is it possible to design an expanding opcode to allow the following to be encoded in a 12-bit instruction? A register is 3 bits. 4 instructions with 3 registers, 255 instructions with one register, 16 instructions with zero registers. (5)

Q12. Discuss: (5 x 5 =25)

(a) The implications of increasing the bus width in reference to the address bus and data bus.

(b) A two-level centralized bus arbiter.

(c) Flow of control in a recursive procedure.

(d) Problem of external fragmentation in a segmented memory.

(e) Handling of interrupts by the CPU.

Q13. What are the differences between: (3 x 4 =12)

(a) An I/O program-controlled transfer and DMA transfer.

(b) ~~Synchronous and asynchronous buses.~~ Macros and procedures

(c) RISC and CISC