Name:_____ Roll No. _____

COMPUTER ORGNAIZATION & ARCHITECTURE

COMMON QUIZ 2 (2017-18, I)

TIME: 40 mins **Max. Marks: 20**

1. Write-through protocol is used to:
   a) **Achieve Coherency** (b) Reduce time for data transfer (c) Both (d) None of these

2. A machine has a 32-bit architecture, with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is ____**2^{14} - 1**_____.

3. Which of the following statements are true for vertical microinstruction encoding?
   a. If there are *k* control signals, every control word stored in control memory consists of *k* bits, one bit for every control signal.
   b. ***k* control signals can be encoded in $\log_2 k$ bits.**
   c. Parallel activation of several micro-operations in a single time step can be performed.
   d. None of the above

4. How many address and data lines will be there for a 16K x 16 memory system?
   a. 14 and 4
   b. 16 and 16
   c. **14 and 16**
   d. None of the above

5. To build a 1G x 32 memory system, the number of 256M x 8 memory modules required will be _____**4**_____

6. Consider a memory system that takes 10 ns to service the access of a single 64-bit word. The bandwidth of the processor-memory interface will be _____**800**_____ Mbytes per second.

7. Assume that a 1G x 1 DRAM memory cell array is organized as 1M rows and 1K columns. The number of address bits required to select a row and a column will be:

   a. 30 and 1 b) **20 and 10** c) 2^{20} and 2^{10} d) None of the above

8. Assume that a read request takes 50 ns on a cache miss and 5 ns on a cache hit. While running a program, it is observed that 80% of the processor's read requests result in a cache hit. The average read access time is ___**14**_____ ns.

9. Consider a direct-mapped cache with 64 blocks and a block size of 16 bytes. Byte address 1208 will map to block number ____**11**_____ of the cache.

10. A cache memory system with capacity of *N* words and block size of *B* words is to be designed. If it is designed as a direct mapped cache, the length of the TAG field is 10 bits. If it is designed as an 8-way set associative cache, the length of the TAG field will be ___**13**_____ bits.

11. Temporal locality is -
    a) Recently referenced items are likely to be referenced again.
    b) Items neighbouring the recently referenced item are likely to be referenced.

12. Assuming all connections between registers are through bus only, for the micro routine of "ADD (R_1), R_2", in uni-bus environment, which of the following group of control signals can be activated at the same time -
    a) Z_{out}, PC_{out}
    b) MAR_{in}, MDR_{out}
    c) PC_{in}, Y_{in}

13. Role of Y_{in} signal in multi-data bus processor is-
    a) **Not available**.
    b) To handle the branch instruction.
    c) To access contiguous memory location.

14. µPC is used to keep track of –
    a) Instruction b) **Control word** c) Micro routine

15. We can reduce number of memory references in an efficient manner using –
    a) Early start
    b) Write through protocol with dirty bit
    c) Write back protocol with dirty bit

16. In direct mapping, which block replacement algorithm outperforms others:
    a) First In First Out
    b) Least Recently Used
    c) Last in First Out
    d) Cannot apply any algorithm

17. For the instructions, given below, if the last address is destination address and processor uses five pipeline stages (Fetch, Decode, Compute, Memory, Write), find :-

    ADD R_1, R_2, R_3

    SUB R_4, R_5, R_6

    MUL R_6, R_3, R_7

    a) Types of dependencies – **RAW**
    b) Number of NOP instructions required – **3**

18. I have word-addressable main memory with 10-bit address space using 2-bits for block size. I want to use a cache memory of 6-bit address using 2-way set-associative mapping. How many bits are required for tag and set field?

    Tag: ___**5**_____bits Set: ___**3**_____ bits