Low-Power High-Linearity CMOS R-2R Ladder DAC with Integrated Two-Stage Op-Amp Driver

Abstract

This paper presents a low-power, high-linearity 4-bit R-2R ladder Digital-to-Analog Converter (DAC) implemented in a 180 nm CMOS process. The DAC employs precision resistor matching and a two-stage operational amplifier to achieve accurate digital-to-analog conversion under low supply voltages. The first stage of the op-amp is a differential amplifier providing high common-mode rejection and gain, while the second stage is a common-source driver enabling large output swing and fast settling. The design targets sensor interface and mixed-signal SoC applications where low power and compact area are critical. Post-layout simulations in Cadence Virtuoso demonstrate an open-loop gain of over 60 dB, a phase margin above 60°, and INL/DNL errors below 0.5 LSB across the full operating range. The proposed architecture shows significant improvement in linearity and power efficiency compared with conventional resistor-string DACs, making it suitable for portable and battery-powered devices.

Keywords: CMOS DAC, R-2R ladder, Two-Stage Op-Amp, Low Power, 180 nm Technology, Mixed-Signal Circuit