FWC IDE ASSIGNMENT

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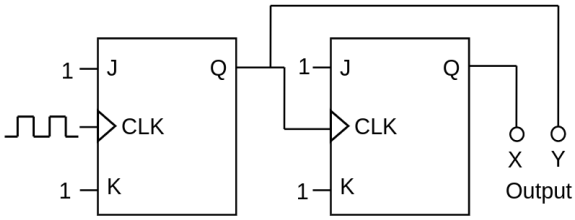
***Abstract*—This document contains the solution of the assignment provided as a part of assessment in the IDE part of the module 1 of FWC3**

Question. The circuit shown in the figure below uses ideal positive edge-triggered synchronous J-K flip flops with outputs X and Y. If the initial state of the output is X=0 and Y=0, just before the arrival of the first clock pulse, the state of the output just before the arrival of the second clock pulse is



Solution :

The output equation for a J-K flip flop is given as:

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

So if J=1 and K=1 then

$$Q_{n+1} = \bar{Q}_n$$

Since the 2nd J-K flip flop clock input comes from the output of the first flip flop so 2nd J-K flip flop will be triggered when output of 1st flip flop goes from low to high(as the flip flops are positive edge triggered).

The table below shows the output states of the flip flops.

Clock	J	K	$Q_0(n)$	$Q_1(n)$	$Q_0(n+1)$	$Q_1(n+1)$
1	1	1	0	0	1	1
2	1	1	1	1	1	0
3	1	1	1	0	0	1
4	1	1	0	1	0	0
5	1	1	0	0	1	1

From the different states we get to know that the next state of the flip-flop after the first clock pulse is **X=1**,**Y=1**. And the above circuit is behaving like a decreament counter.

Given below are the codes of IDE, Assembly and AVR-gcc respectively for the above problem implementation.

https://github.com/ParvChandola/FWC−3−Module−1/blob/main/Assignment%20IDE/IDE.ino

https://github.com/ParvChandola/FWC−3−Module−1/blob/main/Assignment%20IDE/assembly.asm

https://github.com/ParvChandola/FWC−3−Module−1/blob/main/Assignment%20IDE/AVRgcc.c

The connection are given in the table below.

Arduino	2	3	6	7	13	5V	GND
7474	2	12	5	9	CLK1,CLK2	1,4,10,13,14	7
7447	7	1				16	2,6,8