THESIS STAGE 3 PRESENTATION

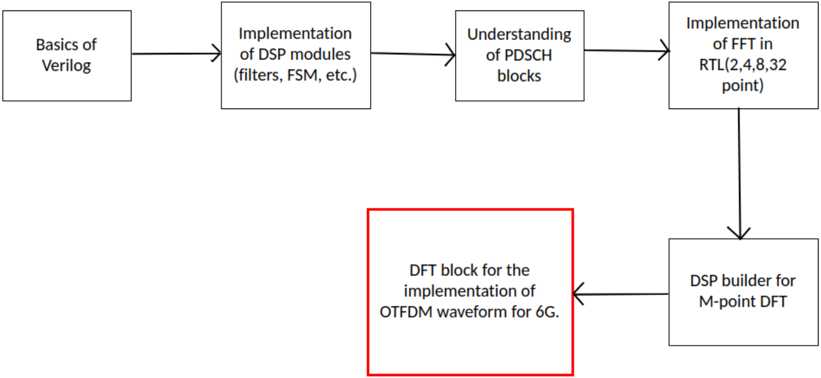
Indian Institute of Technology, Hyderabad.

December 4, 2023

Motivation

- Development of the transmitter for OTFDM waveform for 6G.
- Develop a good understanding of basic verilog circuits.
- Implementation of various signal processing blocks.
- Working with built-in IPs of various DSP modules to understand how they work.
- Implementation of 2,4,8,32 point FFT block in RTL.
- Currently working on DSP builder by intel to integrate the DFT block.

Workflow


Basics of Verilog
Implementation of DSP modules (filters, FSM, etc.)
Understanding of PDSCH blocks
Implementation of FFT in RTL(2,4,8,32 point)
DSP builder for M-point DFT
DFT block for the implementation of OTFDM waveform for 6G.

Contents

Verilog Basics

- Basics of verilog.
- Lecture series on Verilog
- Questions on HDL bits

Combinational Circuits

- Adders
  1. Half Adder
  2. Full Adder
  3. 8-bit and 16-bit ripple carry Adder
- Subtractors
  1. 16-bit subtractor
- Multipliers
  1. Unsigned 16-bit multiplier
  2. Signed 16-bit multiplier

Sequential Circuits

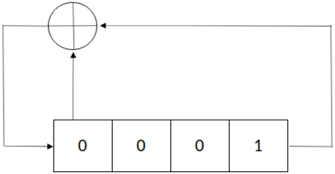
- Flip Flops
  1. D flip flop
  2. SR flip flop
  3. JK flip flop
- Counters
  1. Decade Counter

Sequential Circuits

PN sequence from LSFR

- 4-bit polynomial for generating the PN sequence

$$1 + x + x^4 \tag{1}$$



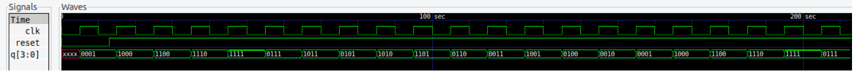


Figure: Waveform for the random sequence generated

Finite State Machine(FSM)

Sequence Detector

- A sequence detector will take a stream of input bits and and will the output bit as 1 if it detects the required sequence else zero.
- In the particular case the sequence is 1011.

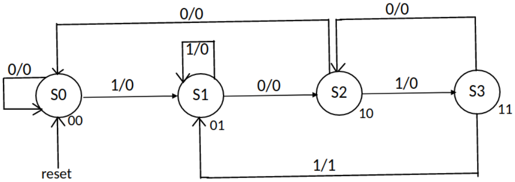


Figure: State transition diagram for the sequence detector

Output of Sequence detector

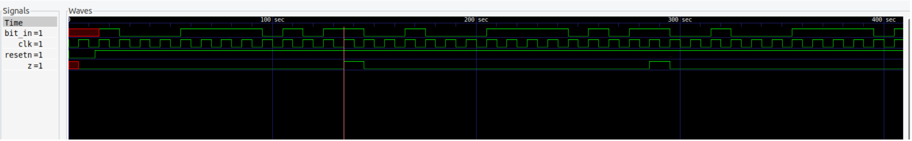
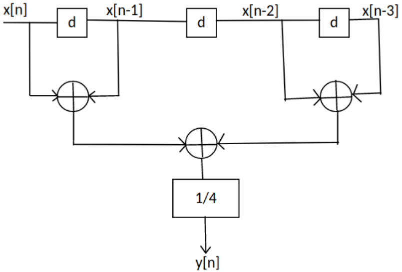


Figure: Waveform for the sequence detector

Moving Average Filter



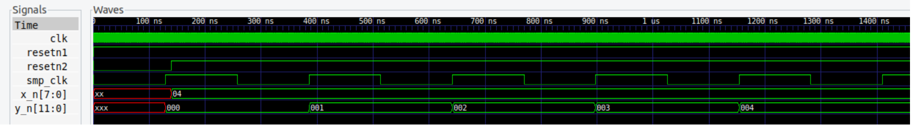
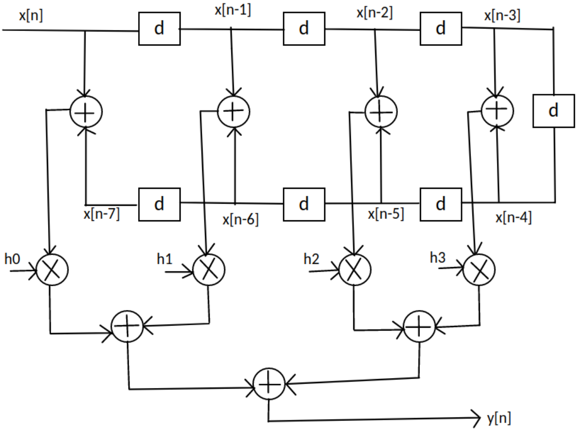


Figure: step response of the filter

8 Tap Filter



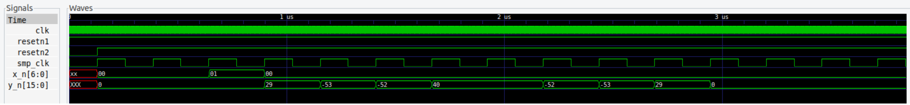


Figure: Implulse response of the filter

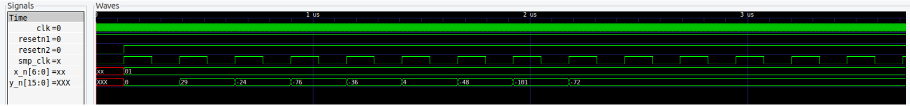


Figure: Step response of the filter

FIR Filter

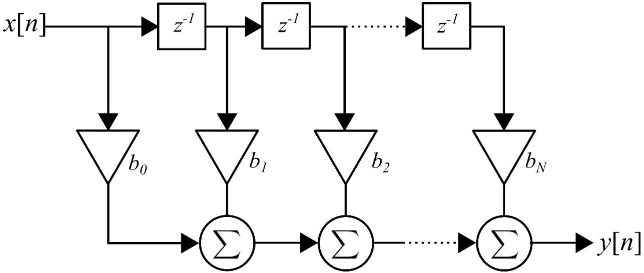
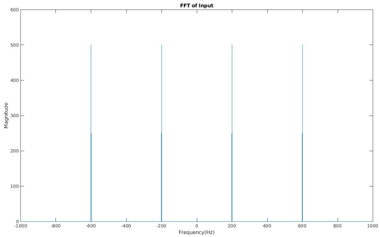
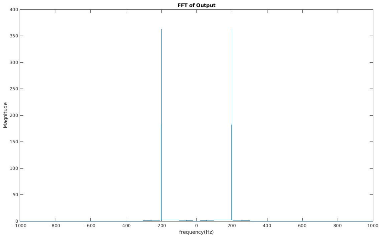


Figure: block diagram of FIR filter



(a) Input to filter



(b) Output of filter

Figure: Comparing the RTL output of input and output of a FIR filter

LDPC coding(bit-flipping algorithim)

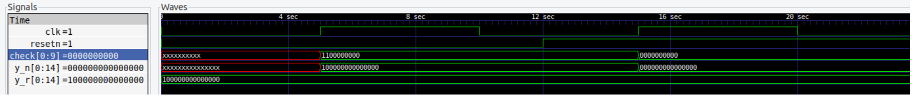


Figure: 1 bit error when all 0 transmitted

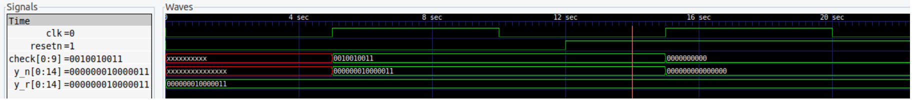


Figure: 3 bit error when all 0 transmitted

Fast Fourier Transform

The Fast Fourier Transform (FFT) is a widely used algorithm for efficiently computing the Discrete Fourier Transform (DFT) and its inverse.

- **Purpose**:FFT is used to analyze the frequency content of a signal. It transforms a time-domain signal into its frequency-domain representation, revealing the amplitude and phase information associated with different frequencies.
- **Algorithmic Efficiency**:The primary motivation behind FFT is to speed up the computation of the DFT. The standard DFT computation has a time complexity of O(N^2), where N is the number of data points. FFT algorithms, including the Cooley-Tukey algorithm, reduce this complexity to O(N log N), making it much faster for large datasets.

- **Divide-and-Conquer Strategy**:FFT achieves its efficiency through a divide-and-conquer approach. It recursively divides the DFT of a composite size N into smaller DFTs of size $N/2$, exploiting the periodicity properties of complex exponentials.
- **Applications**: FFT is used in various applications, including signal processing, audio and image analysis, communication systems, medical imaging, and scientific computing. It allows for efficient computation of convolutions, correlation, and filtering in the frequency domain.

8 point FFT

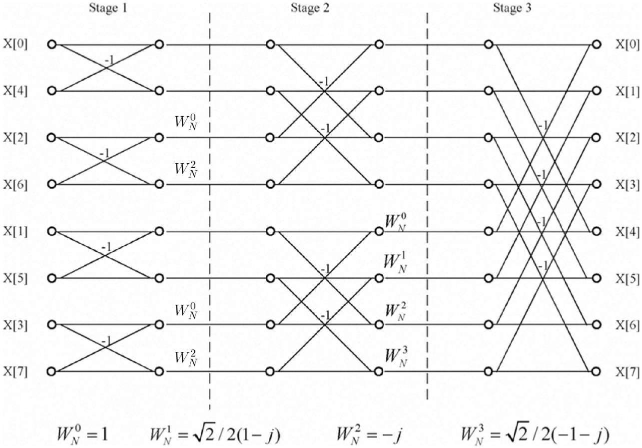


Figure: Butterfly structure of radix-2 8-point FFT

32 point FFT results

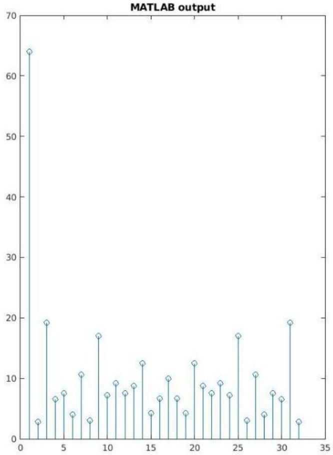


Figure: Comparision of the MATLAB and RTL output of 32 point FFT

OTFDM Waveform generation

- Orthogonal Frequency Division Multiplexing (OFDM) has been a fundamental technology in modern wireless communication systems, such as WLAN, 4G, and 5G, due to its spectral efficiency, multi-user capability, and ease of channel estimation. However, the traditional OFDM waveform has inherent limitations, including a high peak-to-average ratio (PAPR) and power inefficiency.
- We introduce Orthogonal Time Frequency Division Multiplexing (OTFDM) as a candidate for 6G mobile communication. OTFDM is designed to address the shortcomings of traditional OFDM and offer a waveform that enables simultaneous transmission of reference signals (RS) and data with low PAPR, high power efficiency, and reduced overhead.

- The OTFDM symbol is generated by the following set of operations: RS and Data/Control Information is Multiplexed into a single sequence and is fed to a DFT module followed by excess bandwidth spectrum shaping at subcarrier level further followed by IFFT and CP addition operation which generates a OTFDM symbol". By expanding the bandwidth and shaping the spectrum using a pulse shaping filter, the adverse effects of inter-symbol- interference (ISI) are minimized, in addition to reducing the PAPR. The design parameters of RS density, excess bandwidth, and DFT size can be carefully selected to eliminate the irreducible error floor caused by the channel's impulse response.

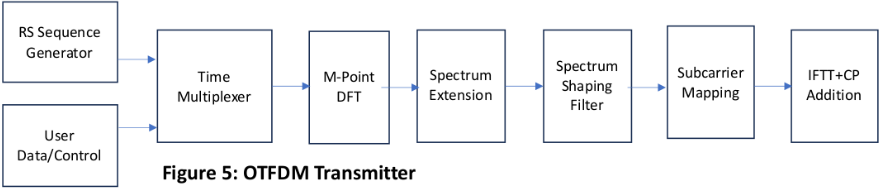


Figure 5: OTFDM Transmitter

DFT using DSP builder

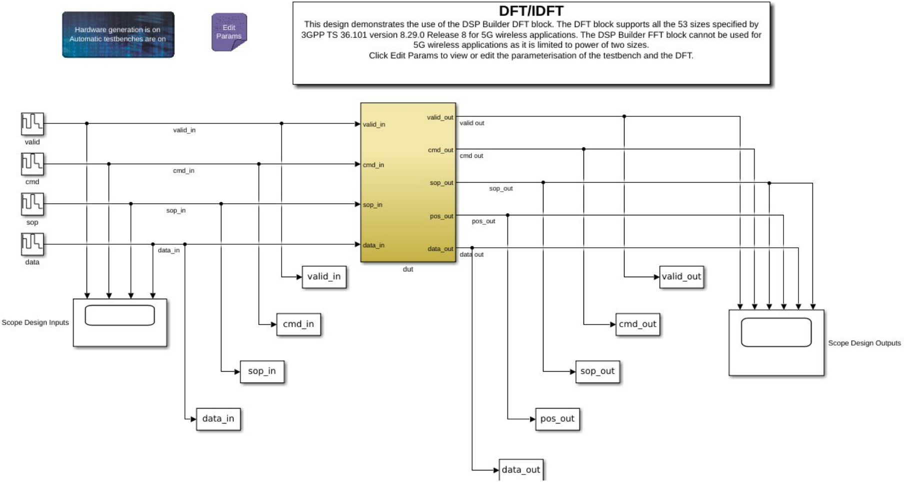


Figure: DSP builder for FFT implementation