University of Windsor

Winter 2015

0688564- RF Integrated Circuit Design

Course Project

Charge Pump Phase Locked Loop

Department of Electrical and Computer Engineering

Instructor: Dr R. Rashidzadeh

Ishita Gupta

104304978

Parvathi Shenoy Kasargod

104213203

ABSTRACT

In the given project, we use TSMC 65 nm technology to design a charge pump phase locked loop by using the block diagram given to us. Top to Down methodology is used and is implemented in Advance Design System (ADS).

The aim of this to project to design a charge pump phase locked loop by using the given specifications to us. Also a condition is given to use only one ideal current source.

Our aim will be to design a Charge Pump Phase Locked Loop with appropriate specifications and also making sure that the loop is locked at a given specified frequency.

CONTENTS

LIST OF FIGURES

GENERAL SPECIFICATIONS

Environment: Agilent Advanced Design System
Technology: TSMC CMOS 65nm
Supply Voltage: 1.0V
VCO Type: Differential Ring Oscillator
VCO Centre Frequency: 1.8GHz
Minimum Capture Range: 200MHz
Damping Factor: 0.65
Power Dissipation: 2mW
Overall Locking Range: 1.5GHz – 3GHz
Temperature Range: -50C to +85C

GENERAL DESCRIPTION

A PLL is a feedback system that includes a VCO, phase detector and low pass filter within its loop, Its purpose is to force the VCO to replicate and track the frequency and phase at the input when its lock. A simple block diagram of a typical charge pump phase lock loop is given below

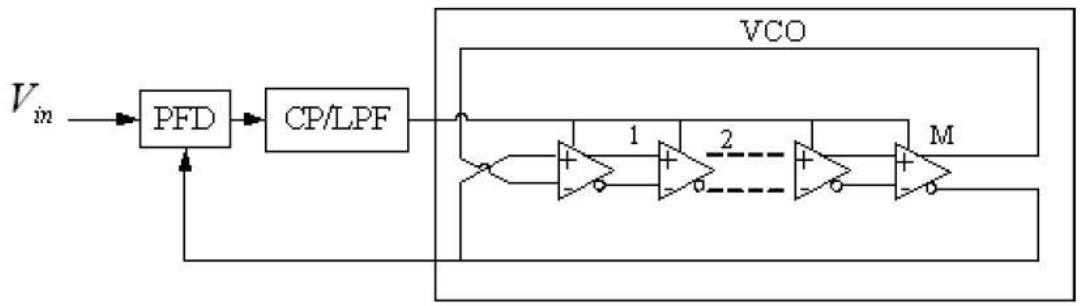

Figure 1: Conceptual Diagram of PLL

DESIGN IMPLEMENTATIONS

A. PHASE FERQUENCY DETECTOR

The circuit employs sequential logic to create three states and respond to the rising (or falling) edges of the two inputs. If initially $Q_A = Q_B = 0$, the rising transition on A leads to $Q_A = 1$, $Q_B = 0$. The circuit remains in this state until B goes high, at which point Q_A returns to zero. This behaviour is similar for the B input.

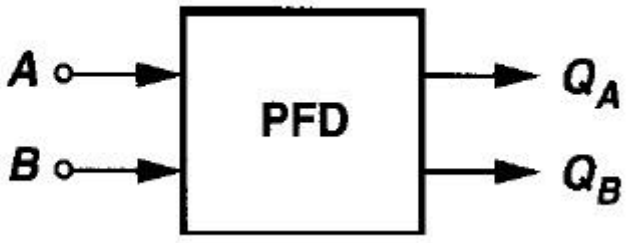

Figure 2: Basic diagram of Phase Frequency Detector

The two inputs have equal frequencies but a leads B. The output Q_A continues to produce pulses whose width is proportional to $\Phi_A - \Phi_B$ while Q_B remains at zero. If A has a higher frequency than B and Q_A generates pulses while Q_B produces pulses and Q_A remains quiet. Thus, the dc contents of Q_A and Q_B provide information about $\Phi_A - \Phi_B$ and $\omega_A - \omega_B$. The outputs Q_A and Q_B are called “UPbar” ad “DOWN” pulses respectively. This analysis of frequencies can been seen in Figure

From the building blocks we create phase frequency detector of the PLL. The phase frequency detector is constructed using D flip flop and a NAND gate. Two square input frequencies are fed into the two inputs of D flip flops as shown in the Figure 2. The outputs are in the form UP, DOWN and UPbar. But the output we are considering here are DOWN (Q_B) and UPbar (Q_A) and these inputs are fed into the charge pump.

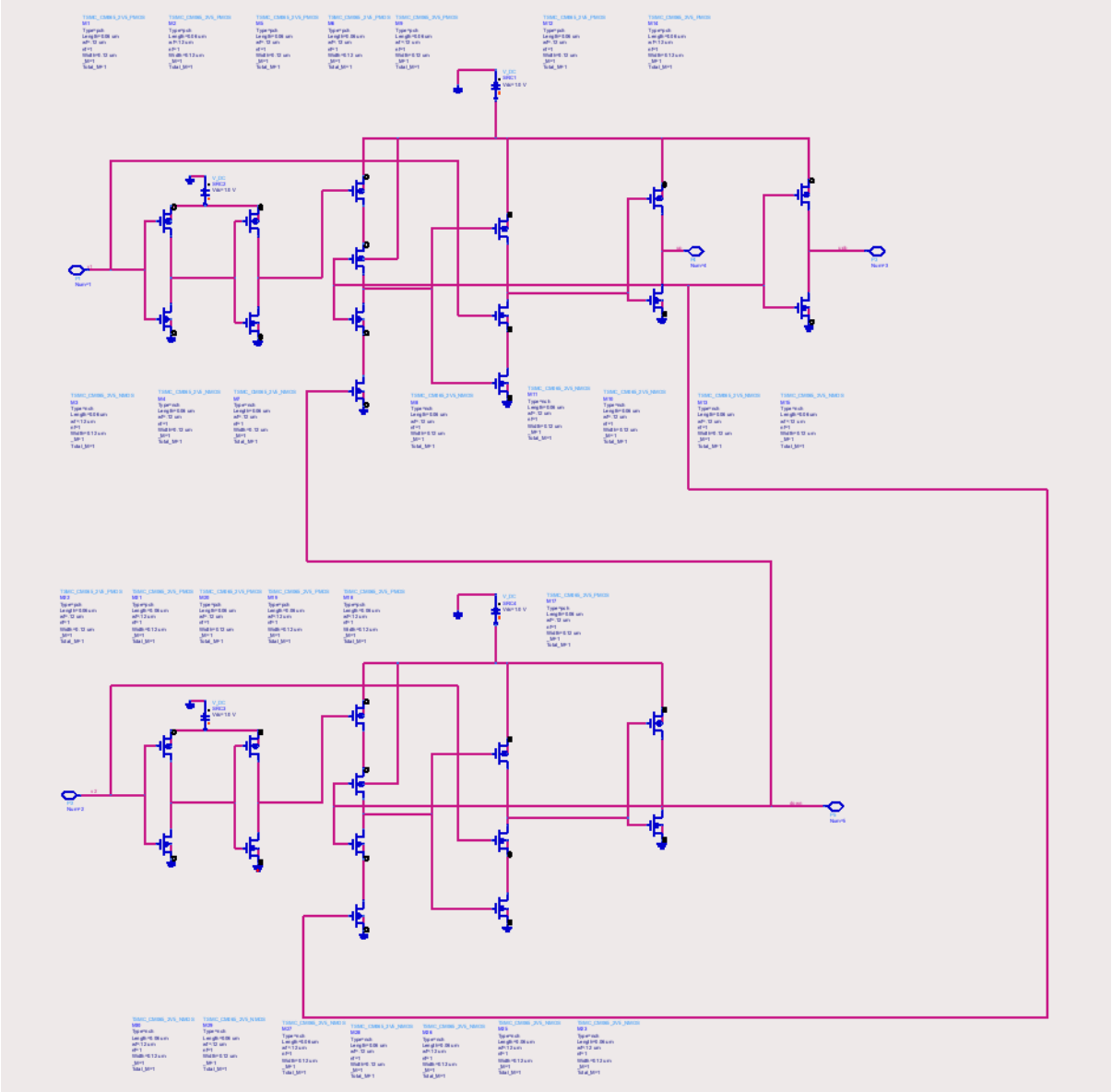

Figure 3: Phase Frequency Detector Design

B. CHARGE PUMP

A charge pump PLL, senses the transitions at the input and output, detects phase or frequency differences and activates the charge pump accordingly. When the loop is turned on ω_{out} may be far from ω_{in} and the PFD and the charge pump vary the control voltage such that ω_{out} approaches ω_{in} . When the input and output frequencies are sufficiently close, the PFD operates as a phase detector, performing phase lock. The loop locks when the phase difference drops to zero and the charge pump remains relatively idle.

For the requirement given to us we have to use one ideal current source for the charge pump. We use TSMC 65 nm technology to create the block of Charge Pump which is the second block in the Figure 1.

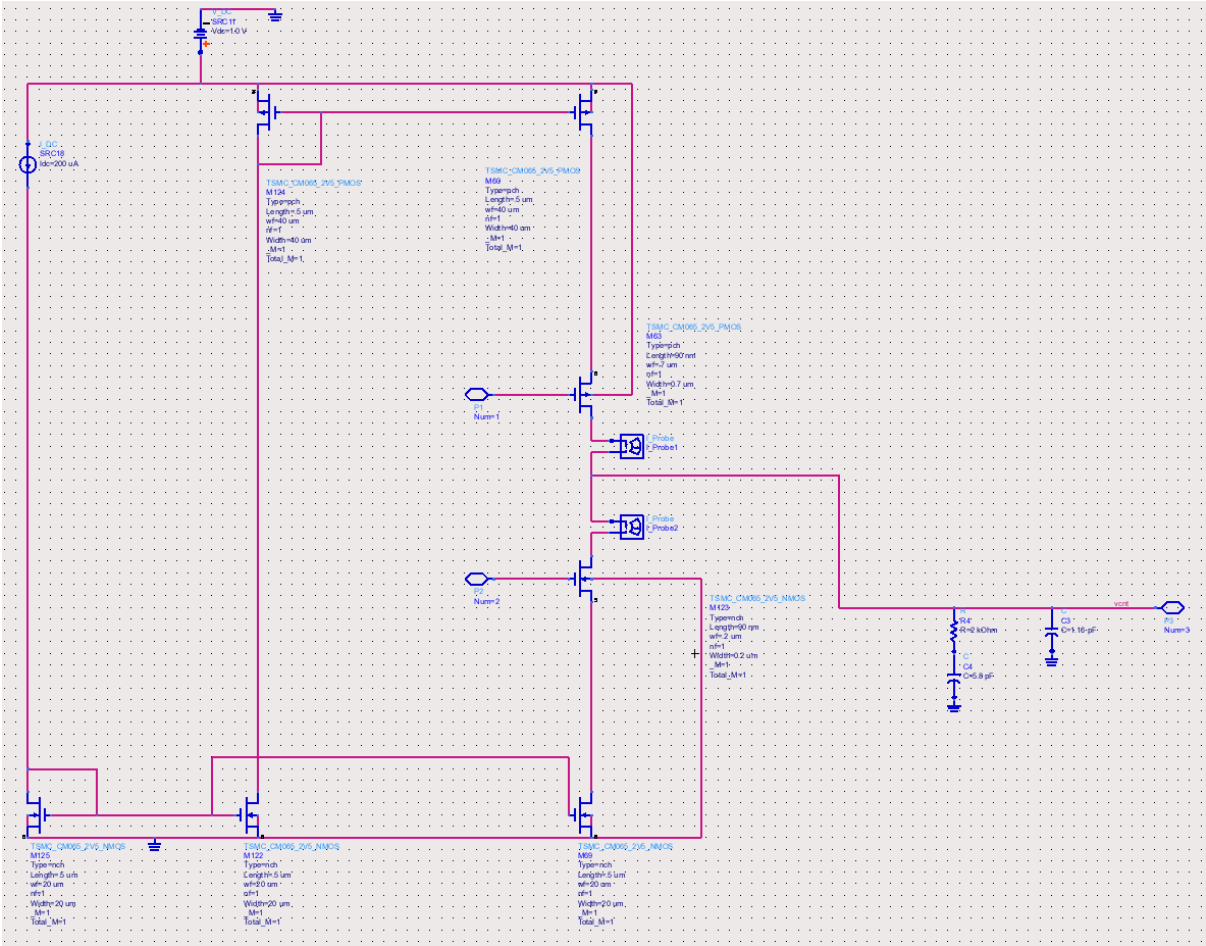

Figure 4: Charge Pump and Low Pass Filter Design

C. VOLTAGE CONTROLLED OSCILLATOR (VCO)

Voltage –Controlled Oscillator or VCO is an electronic oscillator designed to be controlled in oscillation frequency by a voltage point. The frequency of oscillation is varied by the applied DC voltage.

There are two key requirements for oscillation

1. Loop gain = 1
2. Phase Shift = 180 deg.

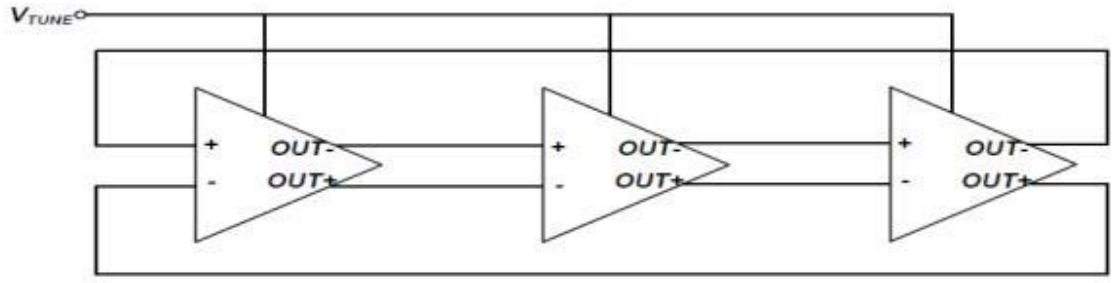

Figure 5: Functional Block of VCO.

The differential ring oscillator is widely used, since it has a differential output to reject common-mode noise, power supply noise and so on. At time the output of first stage changes to logic 1, when this logic propagates to the end, it creates logic 1 and the nth stage, which is fed back to the input of first stage creating logic 0.

In the given project we are using three delay cells and the VCO is created using transistors which is given in the figure 6.

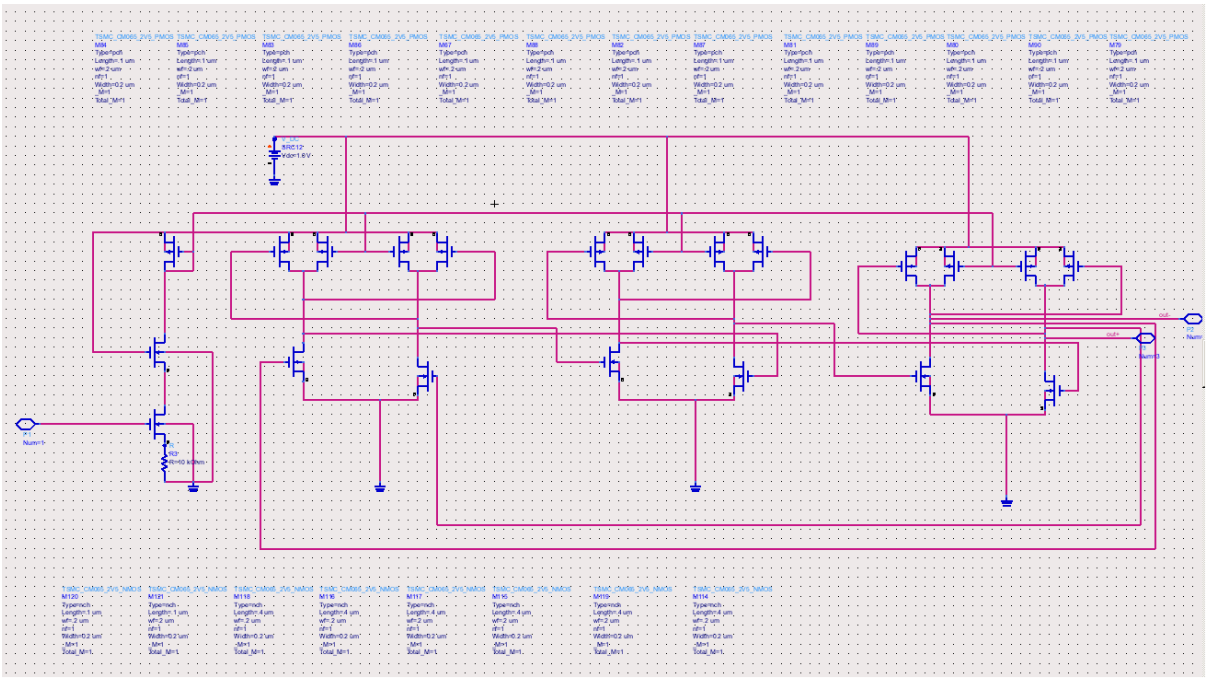

Figure 6: Voltage Controlled Oscillator Design

D. COMBINATION OF ALL BLOCKS OF PLL

After designing the individual blocks of charge pump phase lock loop. We combined them together and get the desired output. In order to reduce the design size, we create symbols of each block that is Phase frequency detector, Charge pump and Low pass filter and lastly the Voltage Controlled Oscillator. The combined circuit is given in the Figure 7

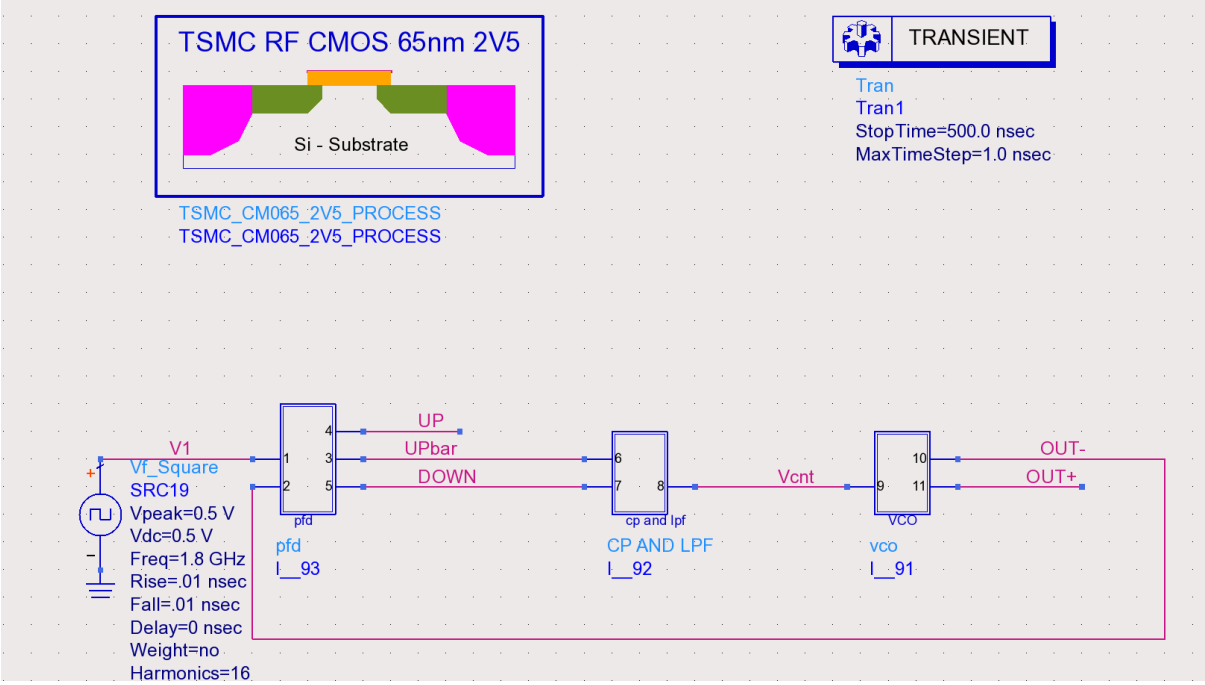

Figure 7: Charge Pump Phase Locked Loop Design

CALCULATIONS

For K_{VCO} :

$$\omega = \omega_o + V_{cnt} K_{VCO}$$

$$K_{VCO} = 1.76\ GHz/V$$

For Dumping Factor:

First, $\frac{I_p}{C_P}$ is supposed to be high so as to get shorter settling time, $I_p R_p$ has to be small so as to get perfect locking of loop

$$\xi = \frac{R_p}{2}\sqrt{\frac{I_p C_p K_{VCO}}{2\pi}}$$

Where $\xi = 0.65$

$$R_p\sqrt{I_p C_p} = 5.508\ X\ 10^{-4}$$

For the bias current not to be large, we set the bias current to be 200 µA, when I_p keeps a small value, Cp and R_p are also kept small

Hence the values of R_p, C_p and C_1 are as follows

R_p= 2 kOhm

C_p= 5.18pF

C_1= 1.16 pF

SIMULATION ANALYSIS

1. DC ANNOTATE SOLUTION OF PHASE FREQUENCY DETECTOR

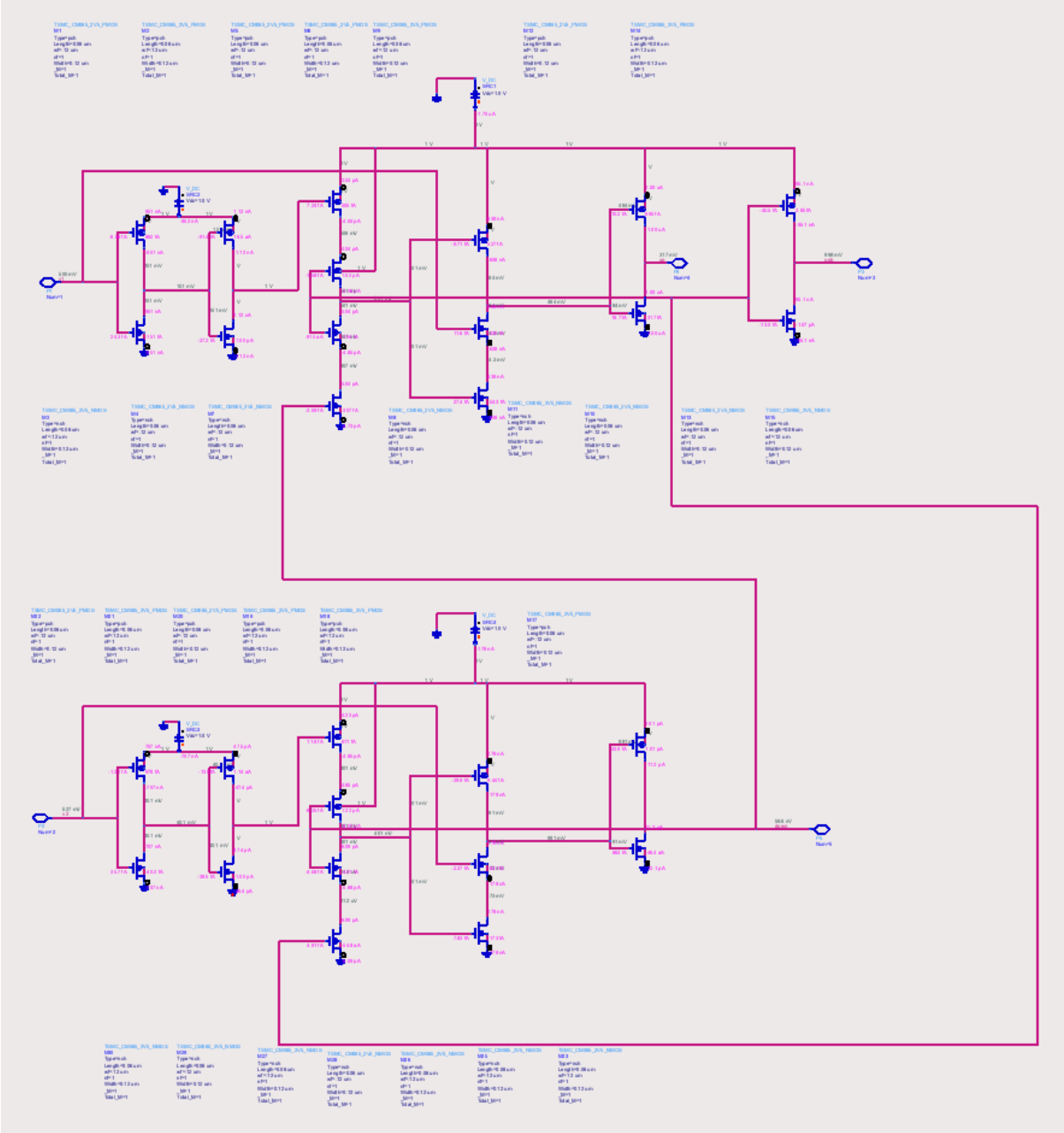

Figure 8

2. PHASE FREQUENCY DETECTOR OUTPUT

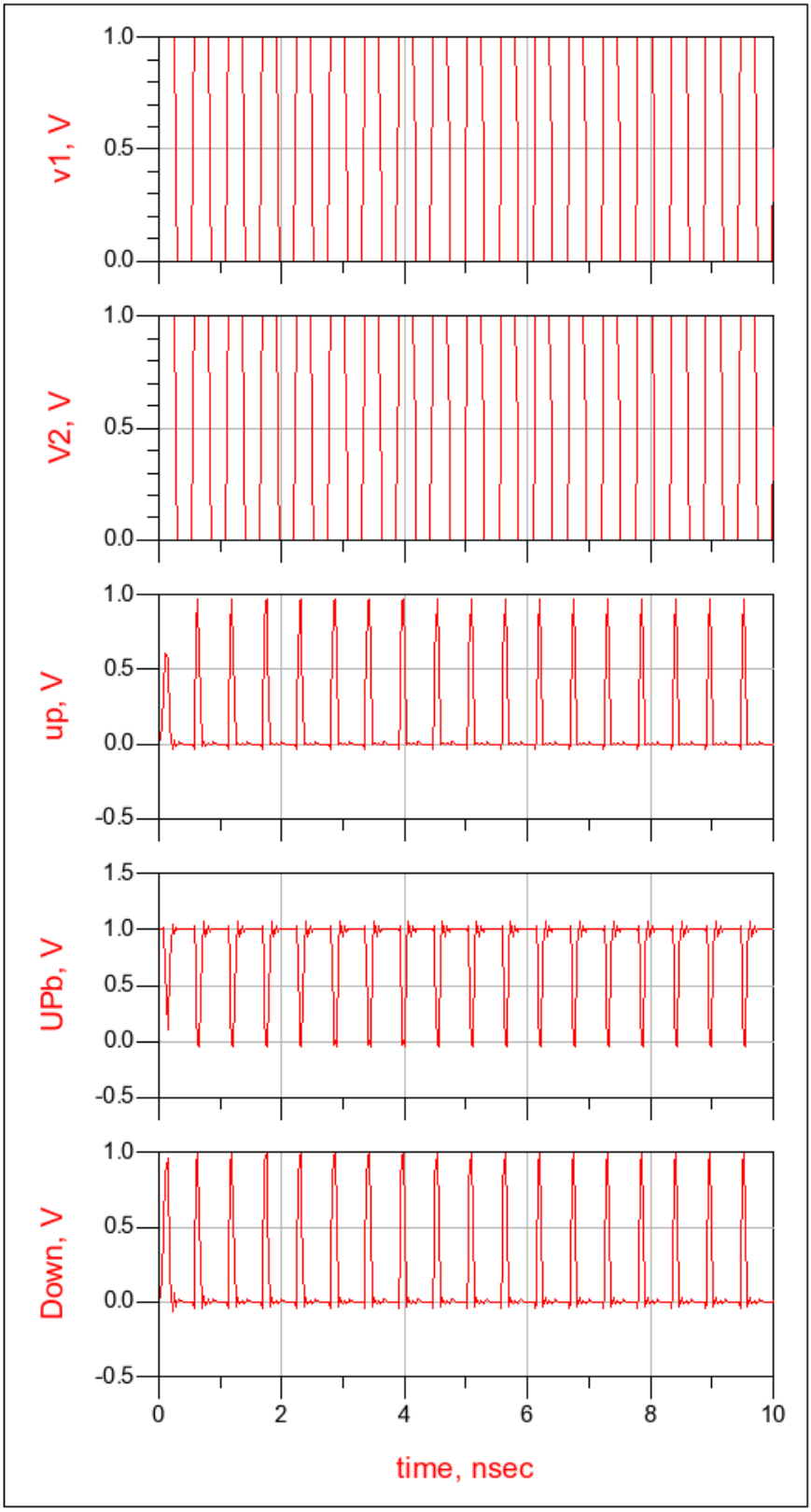

Figure 9

3. DC ANNOTATE SOLUTION OF CHARGE PUMP AND LOW PASS FILTER

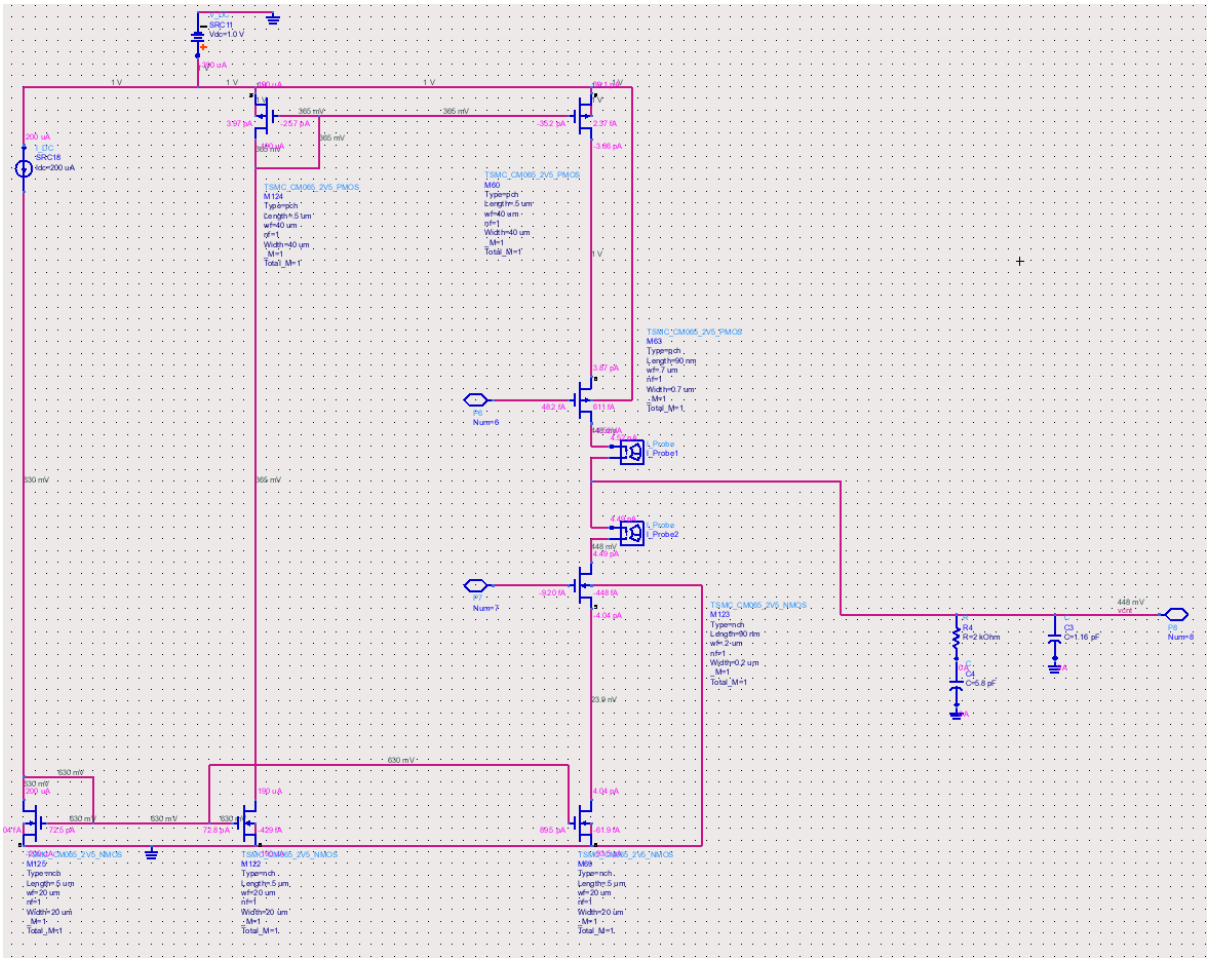

Figure 10

4. DC ANNOTATE SOLUTION OF VOLTAGE CONTROLLED OSCILLATOR

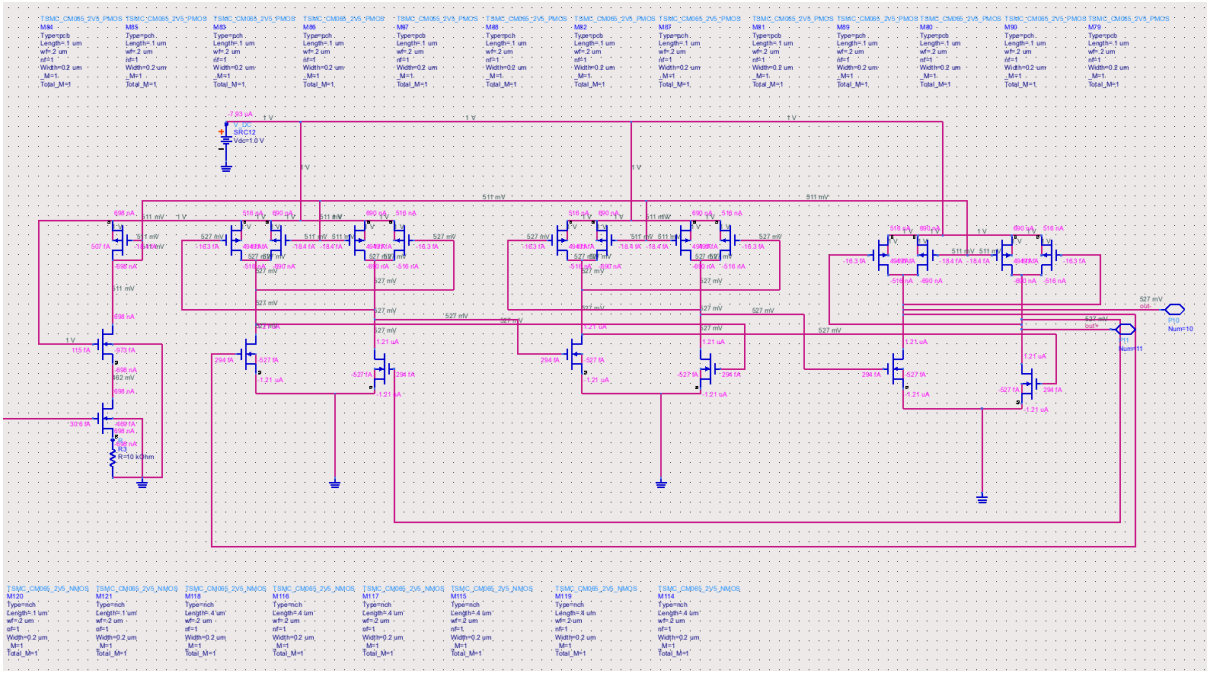

Figure 11

5. DC ANNOTATE SOLUTION OF CHARGE PUMP PHASE LOCKED LOOP

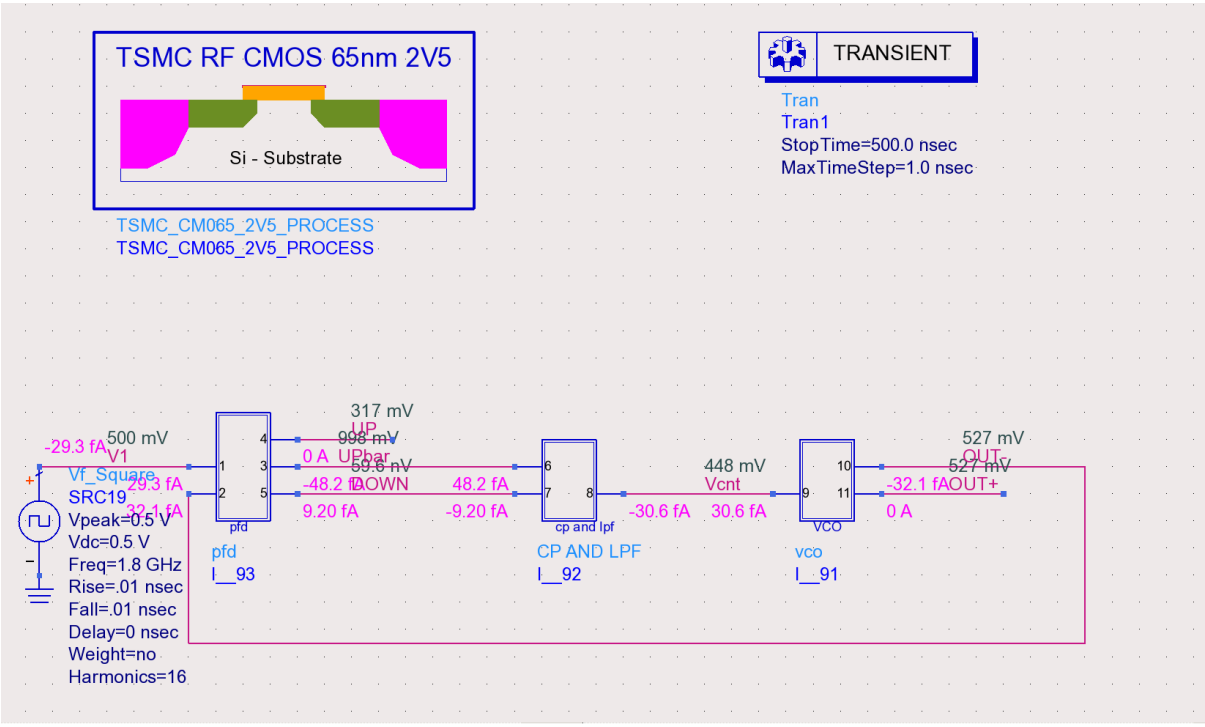

Figure 12

TRANSIENT ANALYSIS

I. Control Voltage and settling time at frequency 1.6 GHz of the system

Eqn freq=1/(indep(m3)-indep(m2))

time	freq
<invalid>sec	1.600 GHz

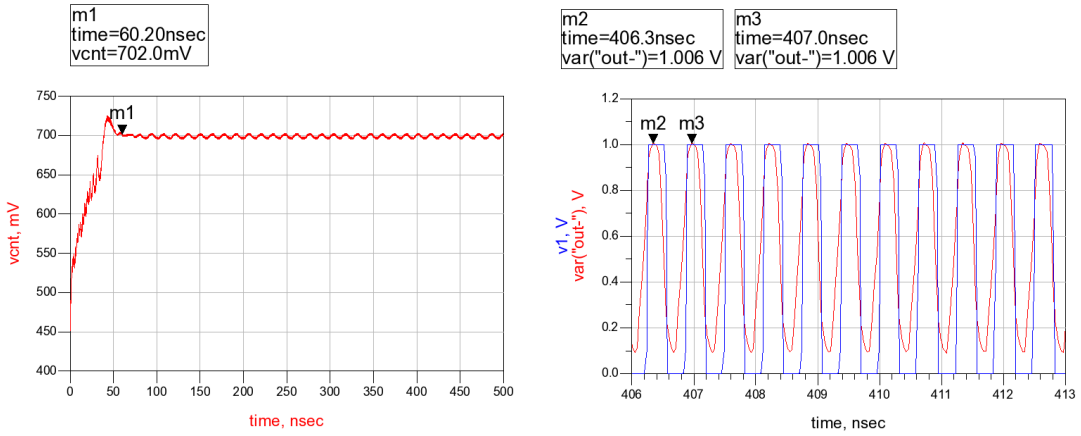

Figure 13

The phase is locked at the frequency of 1.600GHz

II. Control Voltage and settling time at frequency 1.8 GHz of the system

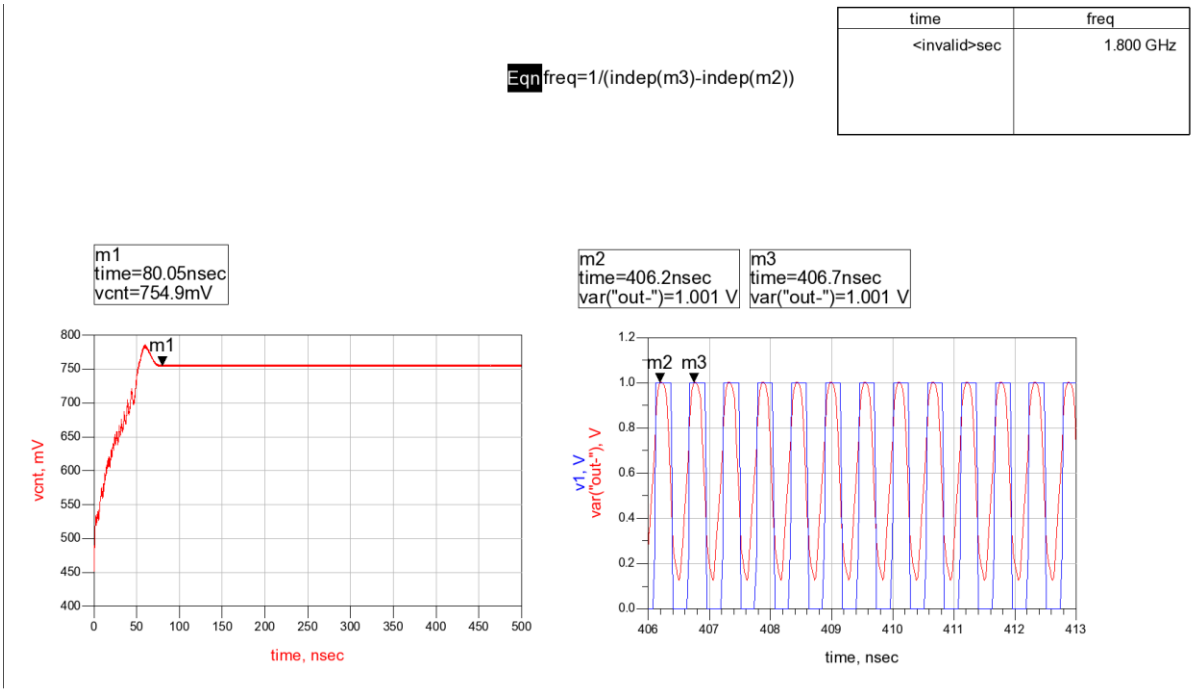

Figure 14

The phase is locked at the frequency of 1.800 GHz

III. Control Voltage and settling time at the frequency 2.0 GHz of the system

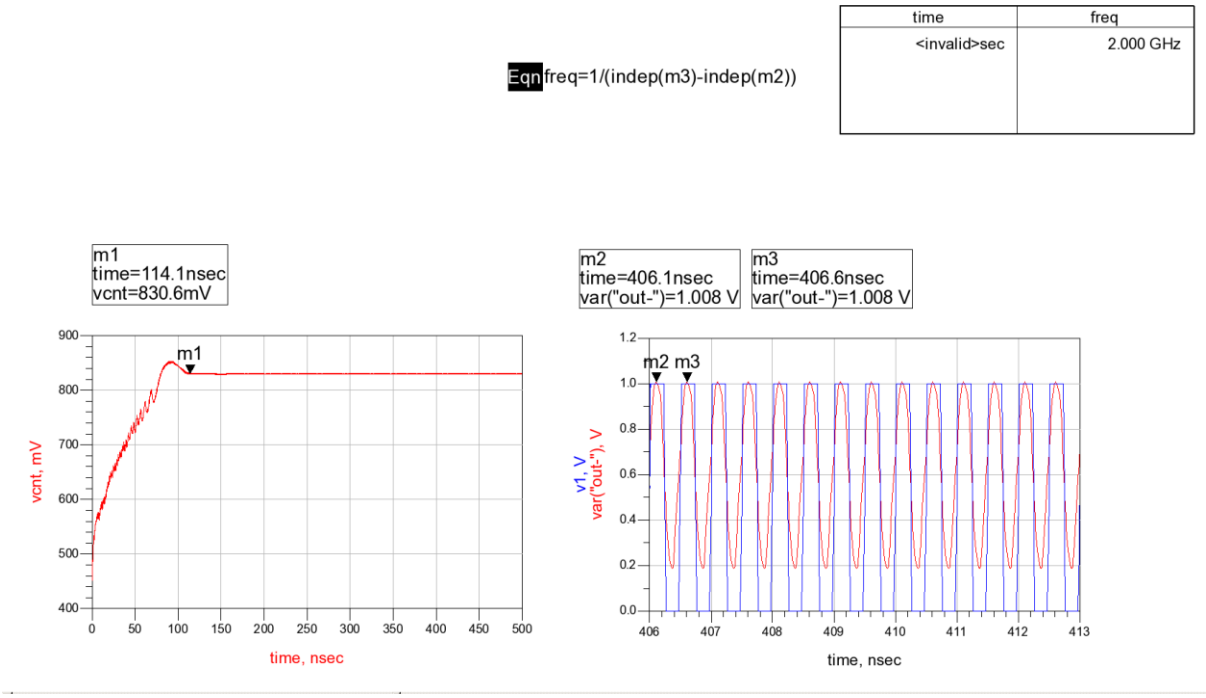

Figure 15

The phase is locked at the frequency of 2.0 GHz

PHASE NOISE OFFSET

For finding the phase noise offset from the palette we choose Harmonic Balance and Harmonic Noise Controller.

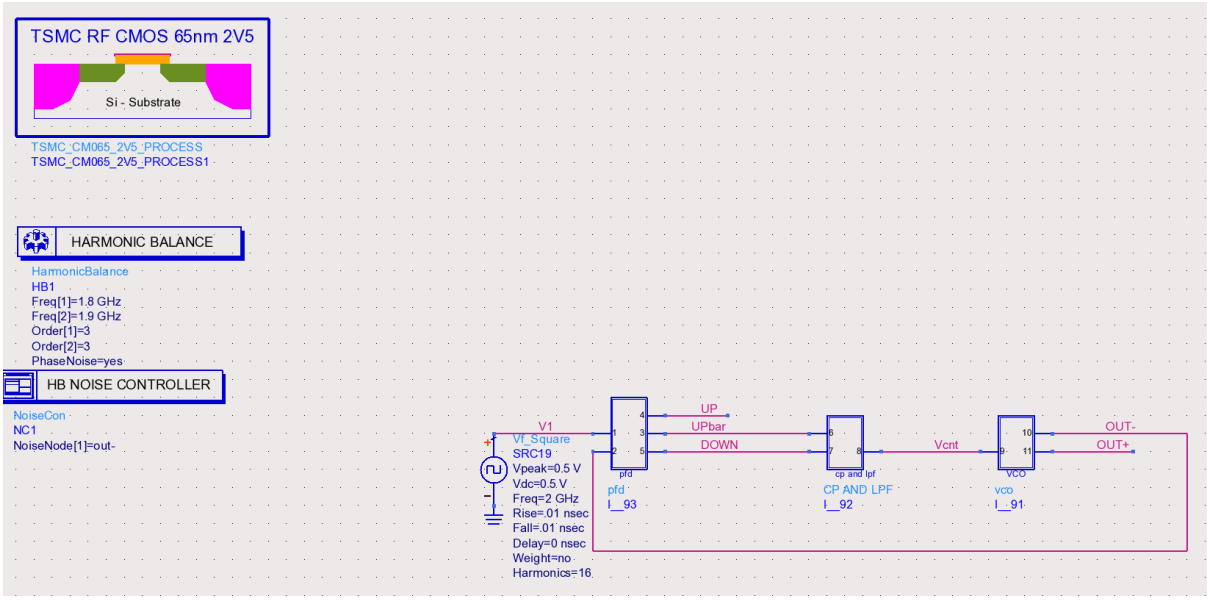

Figure 16: Phase Noise Offset Diagram

By simulating the above diagram we found out the phase noise offset to be at 83.851, the results are given below.

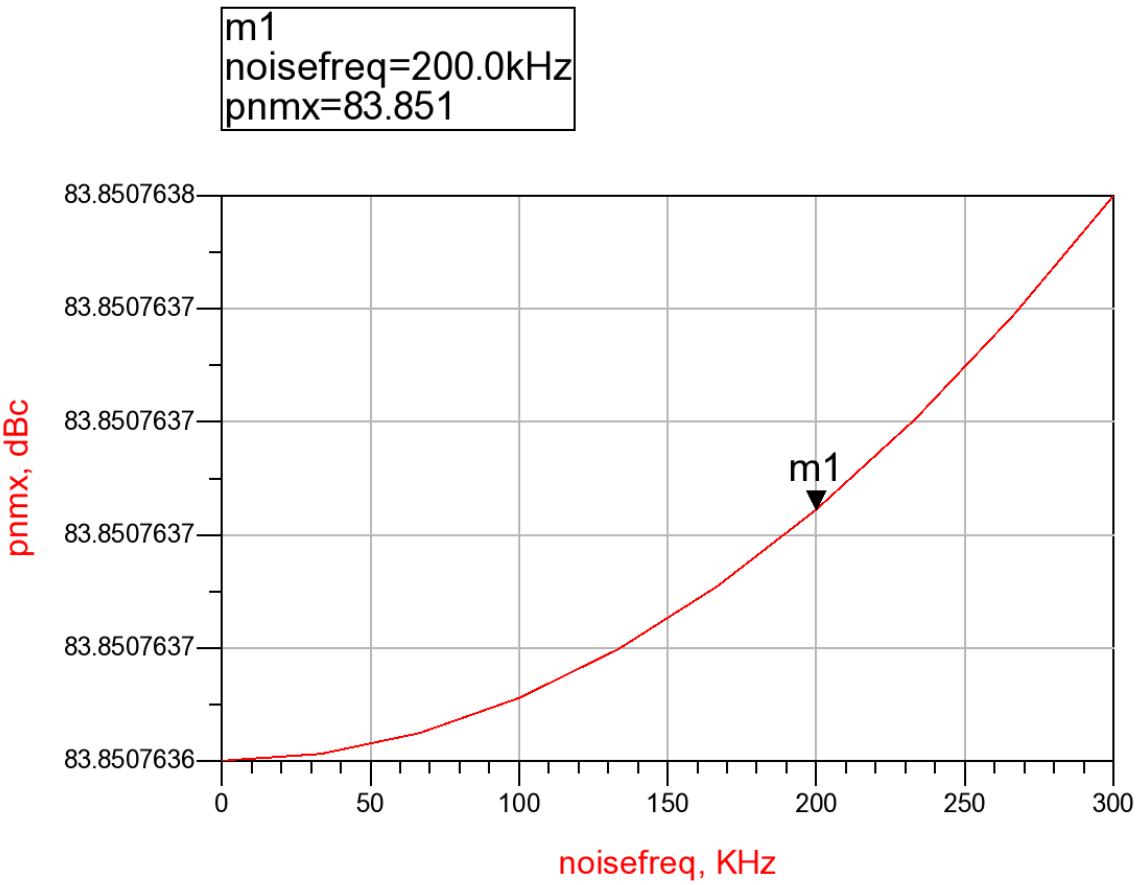

Figure 17: Phase Noise Offset Graph

POWER CONSUMPTION AND RMS JITTER

For power consumption and rms jitter we connect all the VDD sources of each individual block to a common VDD source and I_Probe as shown in the figure 18

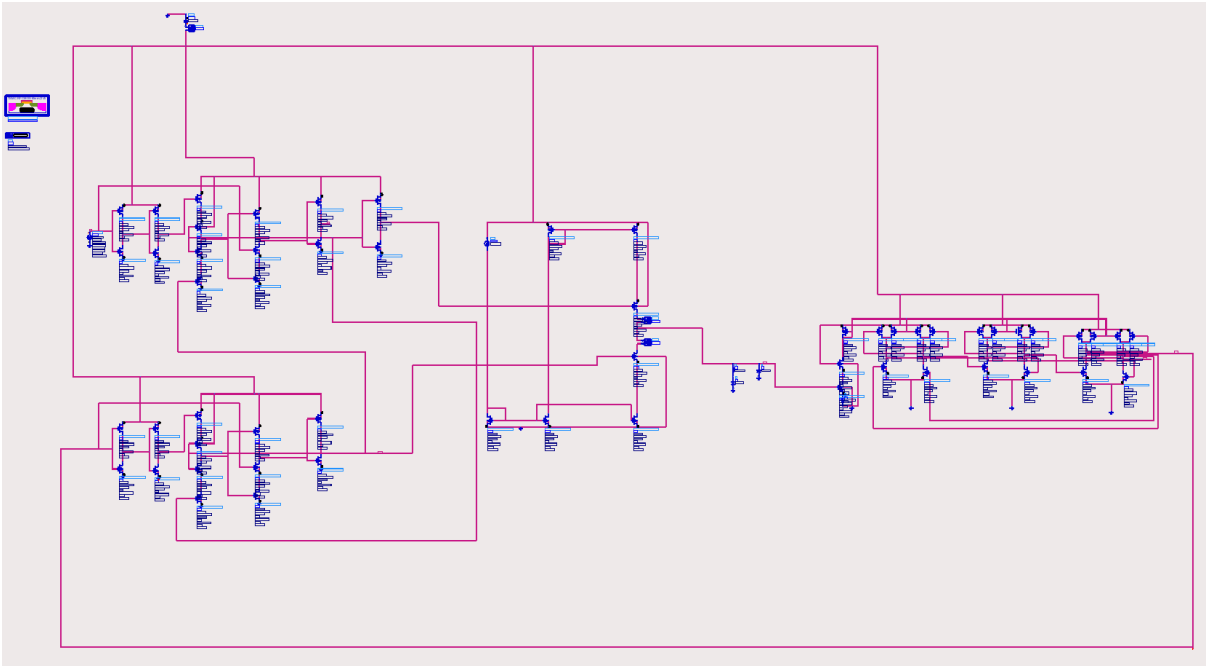

Figure 18: Power Consumption of PLL Design

When we simulate the above design, we write an equation in the Data Display space

$$Eqn\ q = integrate(I_{Probe\,3}.i, 400{,}455{,}1)/100$$

So the total power consumption of charge pump phase lock loop comes out to be 2 mV which is too low as the power consumption value given to us initially that is 6 mV.

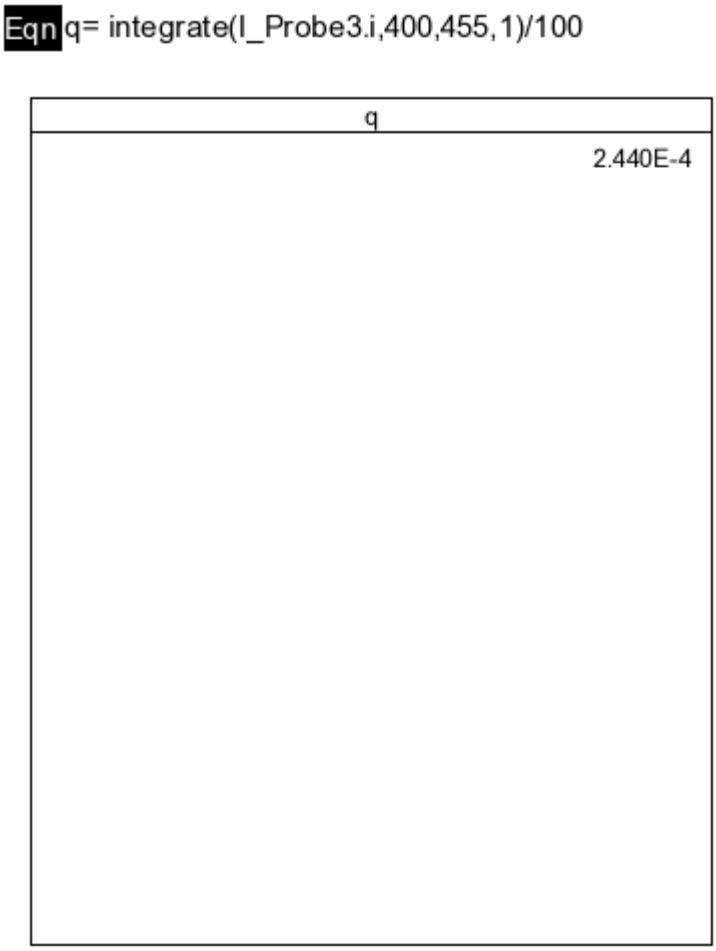

Figure 19: Power Consumption of the PLL system

For performing jitter analysis, we use simulate the main circuit with the transient response and then in Data Display, we choose front panel from tools and then selecting Eye diagram for the jitter. And the graph and the measurement results are shown in the given below figures

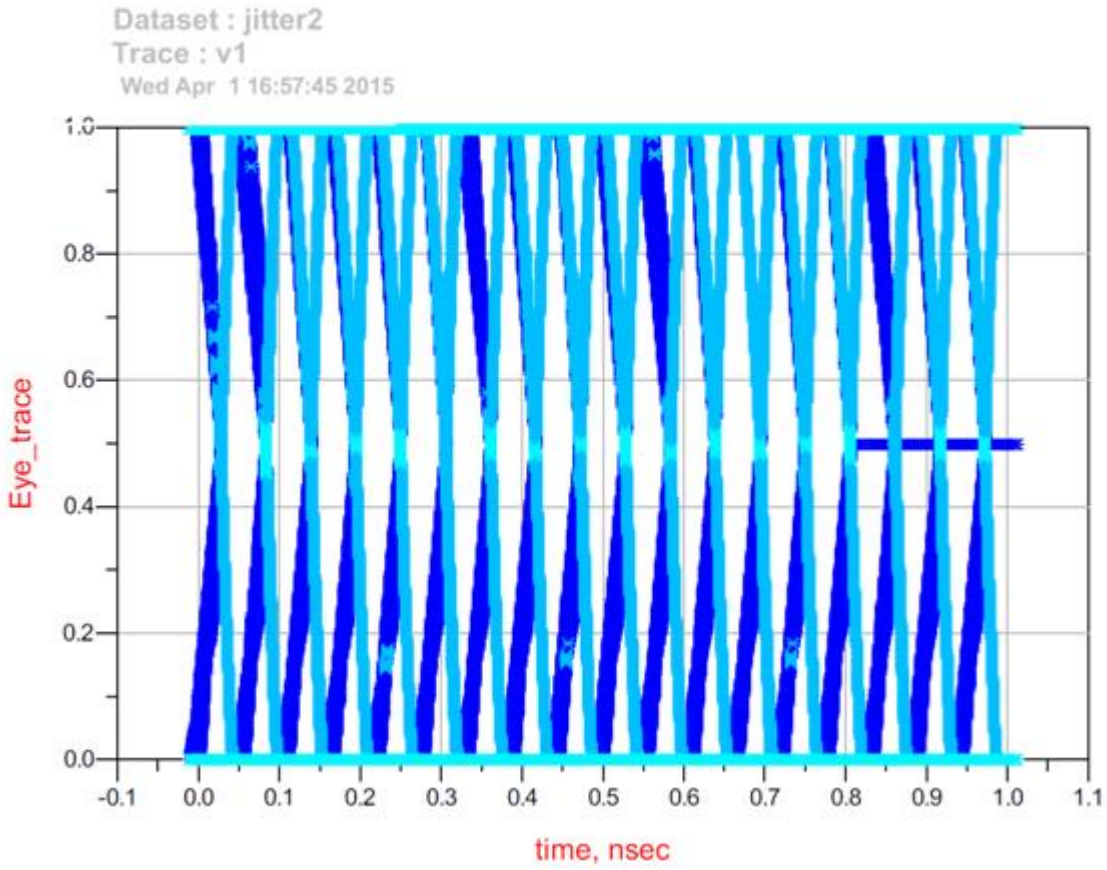

Figure 20: Jitter Analysis of the input Vin

Measurement Results

Eye Level One	FALSE
Eye Level Me...	FALSE
Eye Amplitude	FALSE
Eye Height	FALSE
Eye Height (...	FALSE
Eye Width	-2.2368e-10
Eye Opening...	FALSE
Eye Signal_to...	FALSE
Eye Duty Cyc...	FALSE
Eye Duty Cyc...	FALSE
Eye Rise Time	FALSE
Eye Fall Time	FALSE
Eye Jitter (PP)	6.1169632e-10
Eye Jitter (RMS)	1.9172197e-10

Figure 21: Measurement Results of the Jitter

CONCLUSION

In this project we implemented the charge pump phase locked loop with centre frequency 1.8 GHz. And also saw that at frequencies 1.6 GHz, 1.8GHz and 2.s0 GHz, the CPPLL is perfectly locking but presence of ripples in Vcnt is found at frequency 1.6 GHz. For achieving perfect locking we kept the lengths and widths of transistors as minimum as possible. Phase noise frequency is 83.851 and K_{VCO} is 1.76 GHz/V. Power Consumption is 2mV which is quite low as from the limit given to us that is 6 mV. And RMS jitter in picoseconds is 191psecs

REFERENCES

a. Dr R. Rashidzadeh, Lecture Notes, University of Windsor
b. Behzad Razavi, Design of Analog CMOS Integrated Circuit Design
c. Ryan Perigny, Area Efficient Improvement of CMOS Charge Pump Circuits, Oregon State University, June 2001
d. Yogendra Pratap Singh, Dr. R.K Chauhan, Fast Pump circuits for PLL using 50nm CMOS technology, International Journal of Advance Research in Computer & Communication Engineering , July 2013
e. Prof. R. H. Talwekar, Prof. (Dr.) S.S Limaye, A High Speed Low Power Consumption Positive edge Triggered D Flip-Flop for High Speed Phase Frequency Detector in 180nm CMOS Technology, International Journal of VLSI Design & Communication Systems (VLSICS), October 2012