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Advanced Analog Integrated Circuit Design

Project: Single Ended Two Stage Operational Amplifier

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Design of a Single-ended two stage Operational Amplifier

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Project Description: **Signal processing applications like Continuous-time Delta-Sigma ADCs require op-amps with high gain and linearity. Typically analog signal processing employs fully-differential op-amps. However, in this project a single-ended two stage op-amp has to be designed which satisfies the given specifications using TSMC 180-nm mixed-mode CMOS technology with a VDD=1.8 V supply voltage.**

I. INTRODUCTION

The two stage circuit architecture of the operational amplifier has historically been the most popular approach to Op-amp design. Major operation of an operational amplifier is used to amplify low amplitude signals ,add or subtract voltages or currents and generally used in active filtering. It must have high gain ,high input resistance and low output resistance depending on the input and output signals. The two stage operational amplifiers generally utilizes an differential amplifier , gain stage and an optional output buffer stage as shown in Fig.1 .The input differential amplifier block forms the input of the op-amp and provides a good overall gain and also improves noise performance .The second stage is a common source stage which provides maximum output swings.

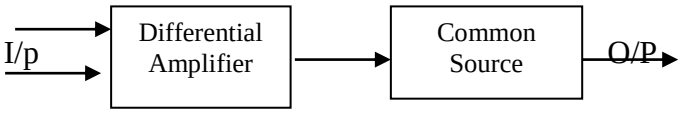

Fig.1-General Block diagram

II. CLASSIC TWO STAGE OPERATIONAL AMPLIFIER

The differential amplifier is made up of transistors M1,M2,M3,M4 as shown in the Fig-2. Where M1 is the inverting input and M2 is the non inverting input .The gain of this stage is trans-conductance of M2 multiplied by the total output resistance seen at the drain of M2 as explained in section III of Design strategy below .The current mirror topology in the differential amplifier circuit M3 performs the differential to single ended output conversion.

The main aim of the second stage is to increase the gain of the amplifier. Here mainly current sink load is utilized , M6,M7 as it provides a very good output swing. Whereas the other topologies like the telescopic is not taken into consideration as it provides very poor output swing. M5 and M8 acts as a simple biasing circuit.

C_C is also known as the dominant pole compensation capacitor which controls the occurrence of the first pole frequency and also used to ensure stability during feedback application. The reason for the inclusion of the resistor resistor is to realize a left-half-plane zero at frequencies around or slightly above resulting in lead-compensation [2].Selecting a value of C_C plays a very crucial role, if we select C_C with a larger value, then the second pole is larger and is unaffected but moves the first pole to the lower frequency.

A. Design Architectures

There are several topologies available for the design of operational amplifier .Firstly let us discuss about telescopic operational amplifier .In spite telescopic being a low power and a low noise amplifier, the gain that can be achieved with a single stage is around 40db .Thus to achieve a gain of 60 db two stages have to be combined in cascade. However two stages bring poles one close to each other which will require a need of compensation network there by reducing the design flexibility. Moreover it has a very small output swing and we require a large output swing of 500V/microsecond for our design of operational amplifier. So this topology cannot be recommended as per the specifications given for our project.

Secondly, lets discuss about folded cascode amplifier. In spite of having a better frequency response and high PSSR ratio. The major drawback of these amplifiers is that they have two extra current legs thereby having more power dissipation .For the construction it requires more number of devices there by increasing the noise ratio.

As a result of the above stated problems we can make use of a simple two stage operational amplifier which will provide a high output swing and an intermediate frequency response with a good design flexibility .Since our design specification does not put any limitations on negative PSSR and power consumption we can make use of a simple two stage operational amplifier in our design..

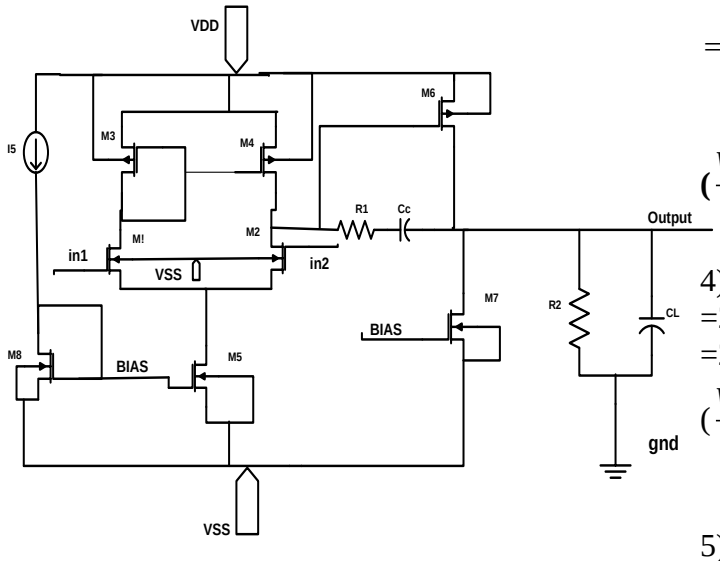

Fig-2 Topology of single ended two stage Op-Amp[1]

III. DESIGN STARTEGY[5]

This section includes two parts firstly architecture design and secondly the component design.

Fig-3 gives the schematic diagram of the architecture design.

In this project the architecture which is available is used and design is carried out according to the need of the specification..

A. Component design

1)Phase Margin $=84.29-\tan^{-1}(\frac{GBW}{P2})$

With the phase margin given as 63 degree and unity gain frequency greater than 100MHz

We get $C_c=.256C_L$

Assume C_L=1pF

We get Cc=.256PF . So let us assume Cc=.4PF.

2)Slew rate= $\frac{I_5}{C_C}$

With slew rate given as 500 V/microsecond

I_5 =200 micro A .

3)

$S3=(I_5/K_3'(Vdd-Vin(max)|Vth03(max)+Vt1(min)|)^2$

$$=\frac{200*10^{-6}}{77.84*10^{-6}[1.8-1.6-.464+.433]^2}$$

$$(\frac{W}{L})_3=(\frac{W}{L})_4=120$$

4) $gm_1=GB*C_C$

$=2*pi*100*10^{-6}*.4p$

$=2.512*10-16$

$$(\frac{W}{L})_1=(\frac{W}{L})_2=\frac{(2.512*10^{-16})^2}{288*10^{-6}*100*10^{-6}}=69.7=69$$

5) $V_{dsat}>=V_{inmin}-Vss-\sqrt{\frac{I_5}{B_1}}-V_{th1}$

$V_{in(min)}=V_{gs1}+V_{od}$

$=V_{gs1}+V_{gs5}-V_{th5}$

$=609.3*10^{-3}+563.7*10^{-3}-486.4*10^{-3}$

$=.6866$

$$V_{dsat}>.8-\sqrt{\frac{250*10^{-6}}{300*175}}-.59$$

V_{dsat}=.209

$$(\frac{W}{L})_5=\frac{2*I_5}{K'_5*V_{DS5sat}^{\ 2}}$$

$$\frac{2*200*10^{-6}}{288*10^{-6}*.209^2}$$

$$(\frac{W}{L})_5 = 124$$

6) $g_{m6}=10*g_{m1}$

$=10*2.512*10^{-16}=2.512*10^{-15}$

$G_{m4}=\sqrt{2*37*10^{-6}*112*200*10^{-6}}$

$G_{m4} = 1.43*10^{-16}$

$$(\frac{W}{L})_6=(\frac{W}{L})_4*(\frac{gm_6}{gm_4})$$

$$(\frac{W}{L})_6 = 104$$

7) $I_6=\dfrac{(\frac{W}{L})_6}{(\frac{W}{L})_4} = 290.3*10^{-6}$

$$(\frac{W}{L})7=(\frac{I_6}{I_5})*(\frac{W}{L})_5=35$$

It is seen from Fig-3 that the ideal current source of 200 micro Amp as shown in Fig -2 is replaced by a current mirror .We are making use of Wilsons current mirror in our circuit as it requires limited amount of resources does not require additional bias voltages or resistors which are more commonly used in cascaded or restively degenerated mirrors.The low impedance of the circuit makes it possible for the bias to operate at higher frequency .provides good linearity in the bias current operation.

The test bench for the architecture was created as shown in Fig-4 which is an open loop operational amplifier

It can be seen from the Fig-5 that the design of the operational amplifier has a gain of 62.35 dB , phase of 64.56 degree, Unity gain frequency of 188.74MHz .A load capacitor of 1PF and a resistor of 5K ohm is used as per the given specification. Thus satisfying all the required requirements of the operational amplifier design.

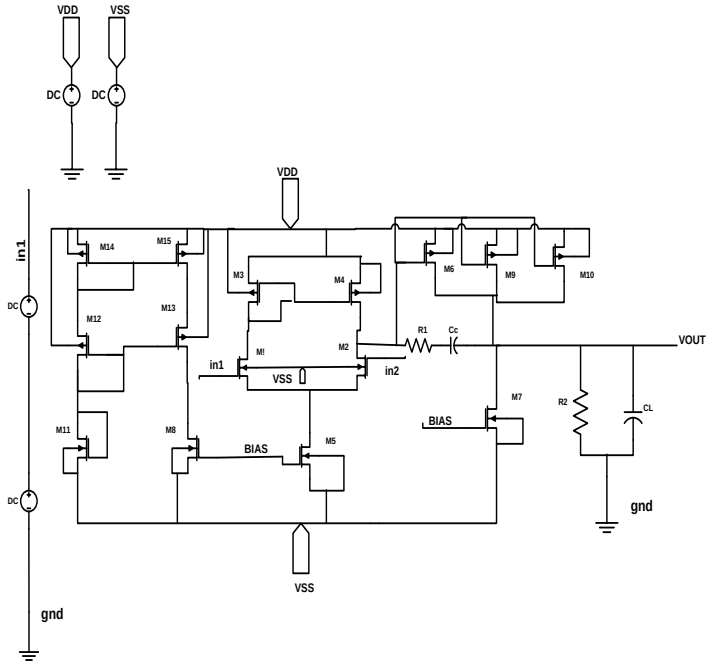

Fig-3 Architecture design

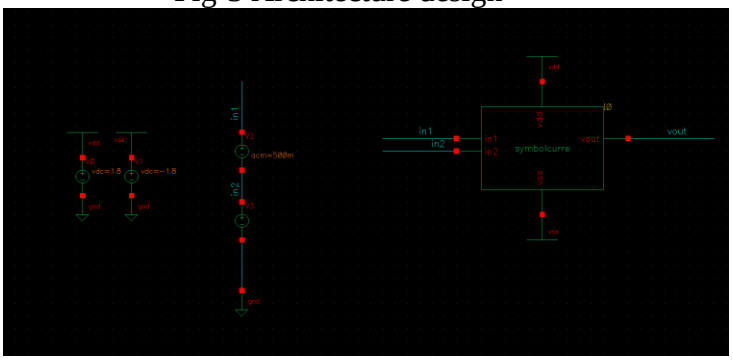

Fig-4 Test bench of open circuit operational amplifier

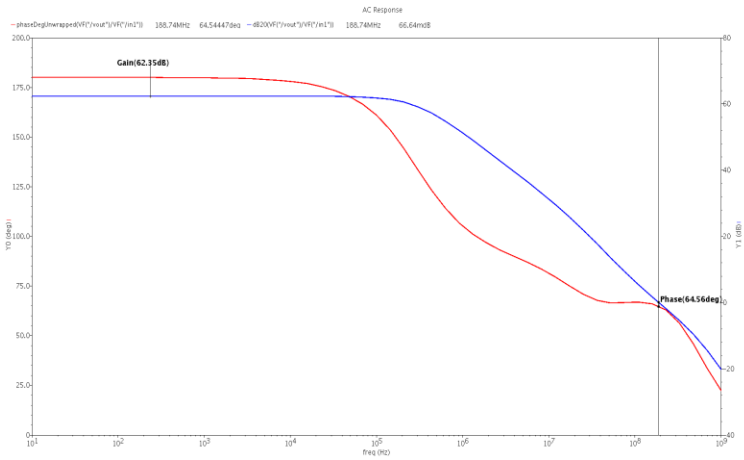

Fig-5 Phase and gain

IV. CALCULATIONS

A. *Slew Rate*

It is defined as the maximum rate of change of output voltage per unit time [3] expressed in volts per micro second. The test bench for the calculation of slew rate is shown in the Fig- 6. Here the non-inverting terminal is applied with a input voltage of 1.6V . A pulse raise and fall time of 1 nano seconds is specified at the input. Inverting terminal will act like a feedback from the output. Fig-6 shows the differential slope technique for the calculation of slew rate . Fig-7 gives the exact value of the slew rate which is 500V/microsecond

Slew rate= $\frac{I_5}{C_C}$

Where I_5 is assumed as 200micro Amp

C_C is .4PF

Hence the theoretical slew rate is 500 V/Microsecond .

From the above procedure we can find that the slew rate obtained both theoretical and practice is similar.

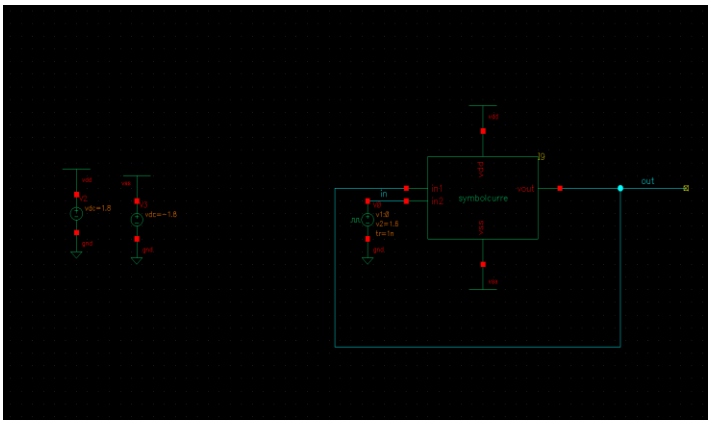

Fig- 6 Test bench for slew rate

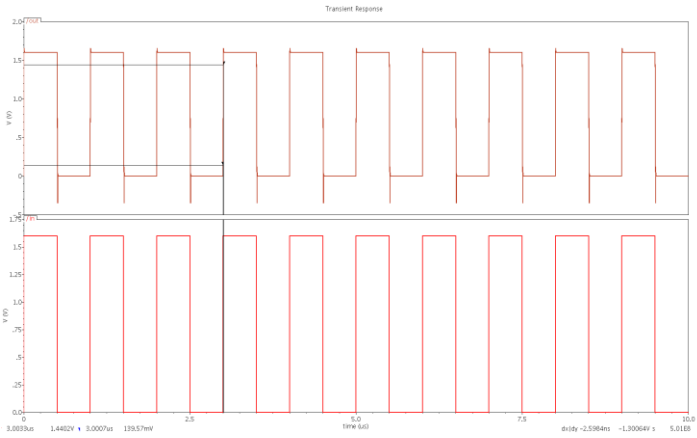

Fig –6 Differential analysis for calculation of slew rate

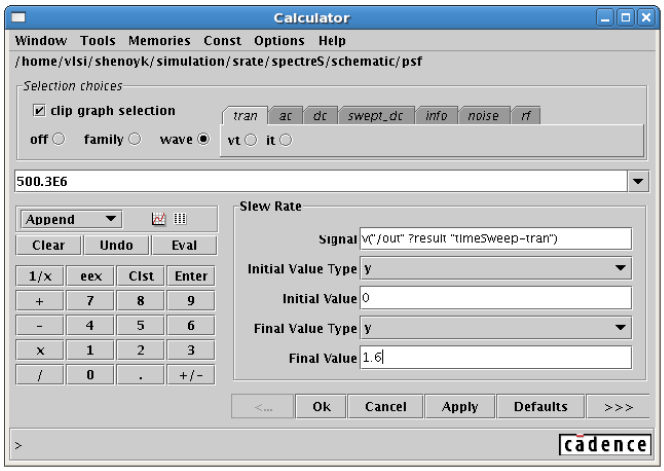

Fig-7 Slew rate found to be 500.3 Volts/microsecond

B. *CMRR*

CMRR measures how output changes when common mode input is applied. Fig-8 shows test bench of CMRR. Two similar voltage sources are connected to the two terminals of opamp in unity gain configuration. Then CMRR can be calculated as Vcm divided by Vout. It is found that CMRR is 73.52dB from Fig-9.

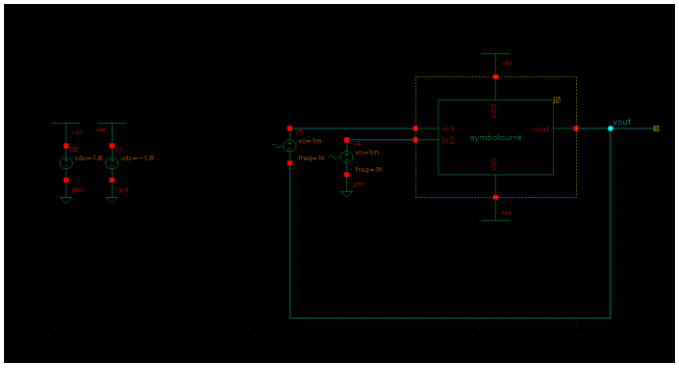

Fig-8 Test bench for CMRR

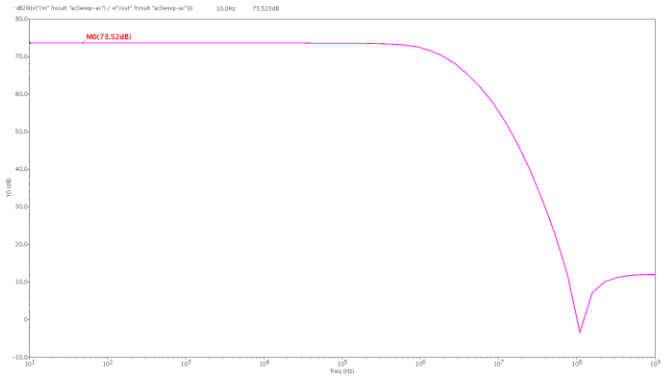

Fig-9 Plot of CMRR(73.52 db)

C. PSSR Positive

Power supply rejection ratio is defined as the amount of noise from the supply that the device can reject .The test bench for this circuit is shown in the Fig-10.For the calculation of PSSR+ place a small sinusoidal voltage in series with Vdd .Then calculate Vdd/Vout .It is found from Fig-11 that PSSR+ is 67.5 dB .

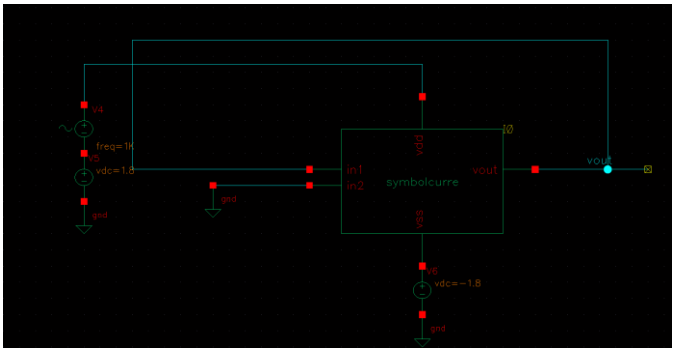

Fig- 10 Test bench of PSSR positive

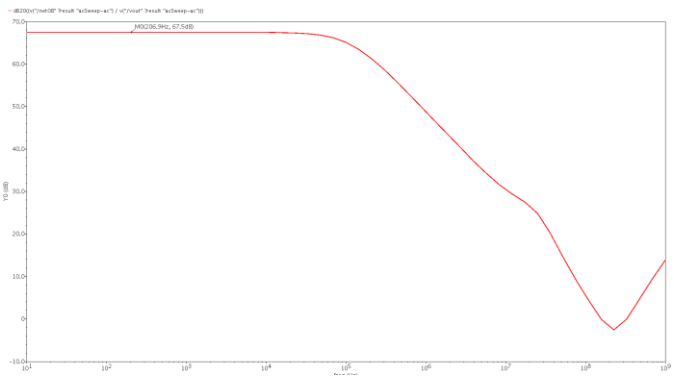

Fig- 11 Plot of PSSR positive 67.5 dB

D. PSSR Negative

Test bench for PSSR- calculation is shown in Fig - 12. .For the calculation of PSSR- place a small sinusoidal voltage in series with Vss,then calculate VSS/Vout . From the Fig-13 PSSR- is calculated as 76.9 dB.

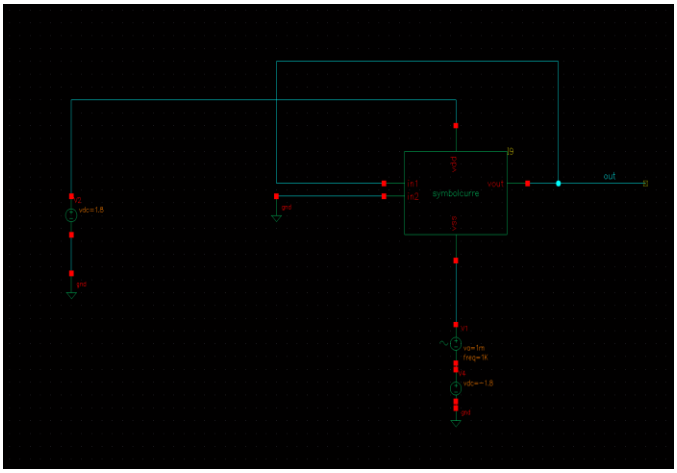

Fig-12 Test bench for PSSR negative

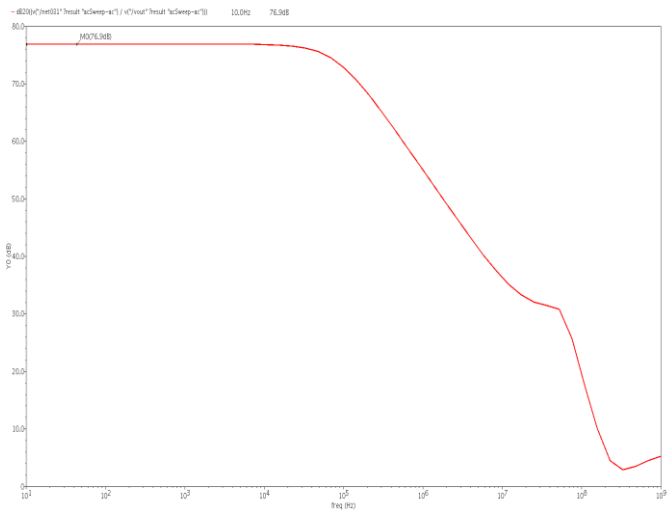

Fig-13 Plot of PSSR negative 76.9 dB

E. Power Consumption

Test bench for power consumption along with DC operating point is as shown in the Fig -14 The power consumed by the circuit can be represented as

$=V_{dd}*I_{dd}+V_{ss}*I_{ss}$

$=1.8*-1.064*10^{-3}+-1.8*731.8*10^{-6}$

=3.23Milli Watt is the total power consumed by the circuit.

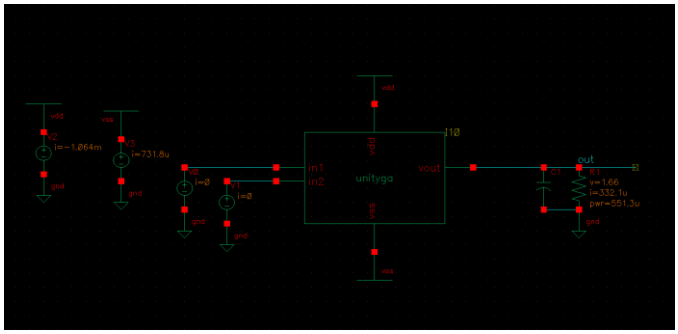

Fig –14 Power consumption

F. Operational amplifier as a Unity gain Amplifier

The closed loop transient analysis is performed on the operational amplifier as shown in the test bench Fig-15.We can clearly see that output exactly follows the input without oscillations as shown in Fig-16 .So the transient analysis tells that the operational amplifier is stable in unity gain configuration.

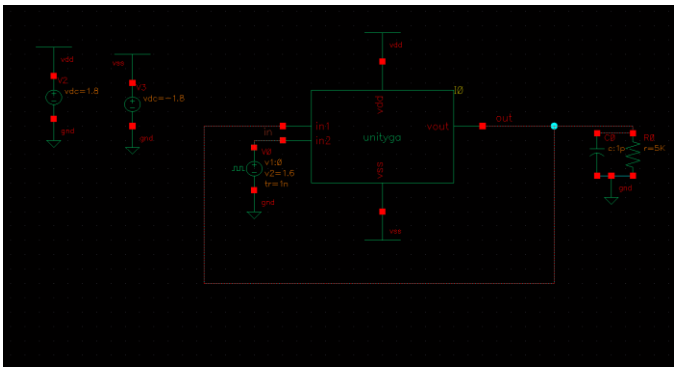

Fig-15 Amplifier in unity gain

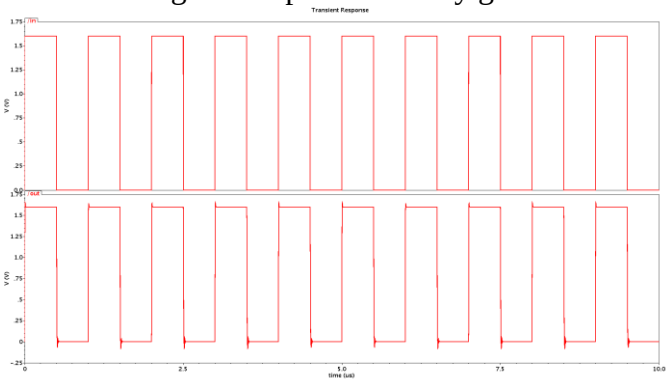

Fig – 16 Unity gain transient response

G. Transistor Parameters g_m, I_d , V_{od}

Table-1 shows the values of g_m, I_d , V_{od} .The name of the transistors is similar to the circuit as shown in the Fig-17

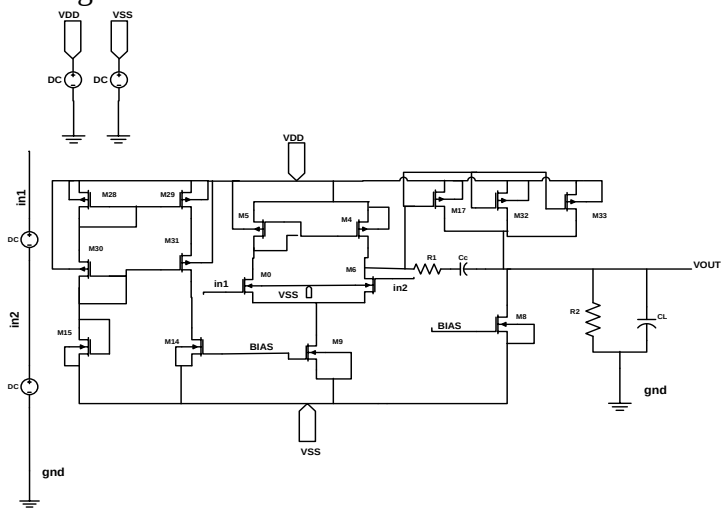

Fig-17 Reference transistor values for table 1

Transitors	gm (S)	id (A)	vgs (V)	vth (V)	Vod(V)
M0	1.59E-03	1.04E-04	7.56E-01	6.97E-01	5.91E-02
M4	1.11E-03	-1.04E-04	-5.94E-01	-4.47E-01	-1.47E-01
M5	1.11E-03	-1.04E-04	-5.94E-01	-4.47E-01	-1.47E-01
M6	1.59E-03	-1.04E-04	7.56E-01	6.97E-01	5.91E-02
M8	1.57E-03	1.25E-04	5.36E-01	5.07E-01	2.90E-02
M9	3.26E-03	2.08E-04	5.36E-01	4.86E-01	5.03E-02
M14	3.15E-03	-1.99E-04	5.36E-01	4.86E-01	5.01E-02
M15	3.15E-03	-1.99E-04	5.36E-01	4.86E-01	5.01E-02
M17	1.95E-03	-1.52E-04	-5.94E-01	-5.09E-01	-8.48E-02
M28	3.90E-04	-1.99E-04	-1.323	-4.38E-01	-8.85E-01
M29	3.90E-04	-1.99E-04	-1.323	-4.38E-01	-8.85E-01
M30	3.54E-04	-1.99E-04	-1.74	-7.78E-01	-9.63E-01
M31	3.54E-04	-1.99E-04	-1.74	-7.78E-01	-9.63E-01
M32	1.95E-03	-1.52E-04	-5.94E-01	-5.09E-01	-8.48E-02
M33	1.95E-03	-1.52E-04	-5.94E-01	-5.09E-01	-8.48E-02

Table-1 Transistor parameters

V. *BAISING CIRCUITS*

Fig-18 shows the circuit of the biasing currents, the ideal current source is replaced by an Wilson current mirrors as shown in the Fig-19 .It is seen that the ideal current source of 208micro amps(theoretical 200 micro amps) is replaced by a current mirror circuit .Which provides the same current biasing ,for the entire operational amplifier. Table-2 shows the theoretical and practical ratios of the transistors used in the design of the operational amplifier.

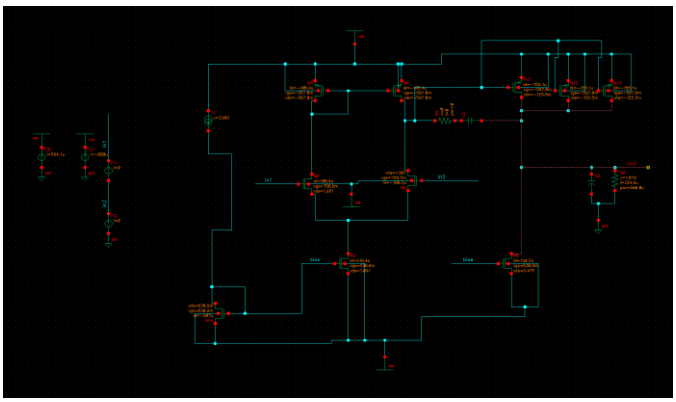

Fig-18 DC operating points of the ideal current

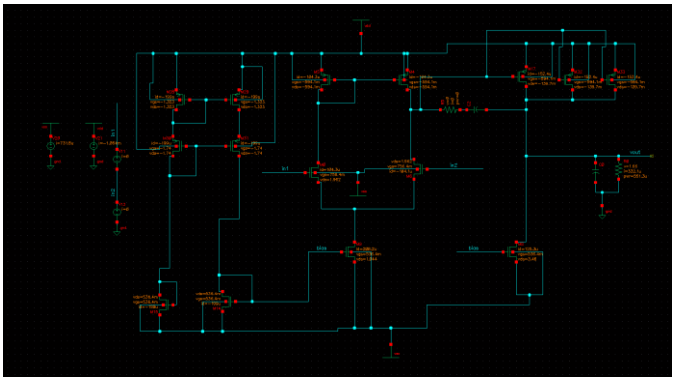

Fig -19 DC operating points with current mirror

transistor	W	L	Ratio practicle	RatioTheoretical
M1	150u	2.5u	60	69
M2	150u	2.5u	60	69
M3	240u	2u	120	120
M4	240u	2u	120	120
M5	62u	500n	124	124
M6	49u	180n	272.2	104
M7	6u	180n	33.3	33.3

Table-2 Theoretical and practical ratio of amplifiers

VI. CONCLUSION

The single ended two stage operational amplifier has been designed using a Wilson current mirror for biasing which provides a current of 208 micro Amps. .A gain of 62.35 dB ,phase of 64.56 degree and a unity gain frequency of 188.74 MHz has been achieved as per the project requirement .

VII. REFERENCES

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