AN-1339
APPLICATION NOTE

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ADF7023-J AD_15d4g Firmware Download Module

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INTRODUCTION

This application note describes the AD_15d4g firmware download module for the ADF7023-J transceiver IC. The AD_15d4g firmware download module adds the following features to the ADF7023-J:

- IEEE 802.15.4g physical layer (PHY) header formatting
- IEEE 802.15.4g data whitening
- Tx/Rx rolling data buffer
- 1 byte to 1000 byte Tx preamble
- ARIB STD T108 clear channel assessment (CCA)
- Rx antenna diversity

Figure 1 shows a block diagram of the ADF7023-J low power, 902 MHz to 958 MHz transceiver IC. The transceiver contains a custom microcontroller (MCU) core with a mask ROM, which implements packet handling functions and translates radio commands into internal control sequences. An additional 2 kB of program RAM (PRAM) is available and serves as program code memory. PRAM enables the addition of radio controller commands to provide modified or extended functionality. The AD_15d4g firmware download module described in this application note is based on program code downloaded into this PRAM.

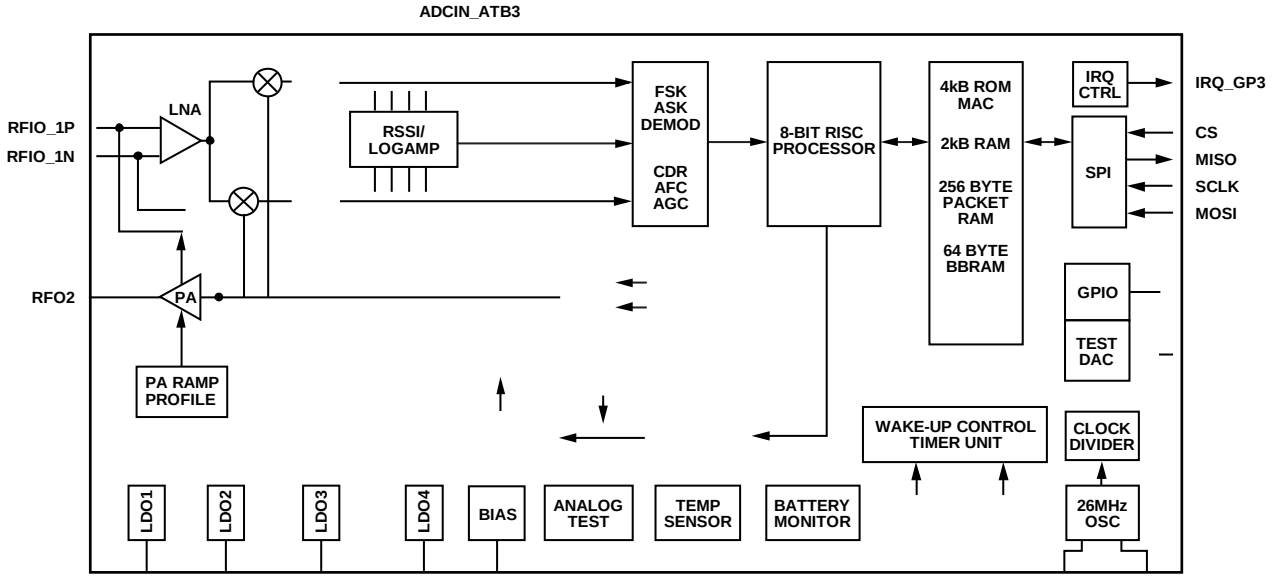
The PRAM block is volatile memory and must be reloaded each time the transceiver wakes up from sleep state. The PRAM locations can be accessed sequentially through the serial peripheral interface (SPI) interface. The details of the code download mechanism are explained in the Code Download Sequence section.

The firmware download binary is **rom_ram_7023_2_2_AD_15d4g_R4p3.dat** and is available from Analog Devices, Inc., at ftp://ftp.analog.com/pub/RFL/FirmwareModules.

The revision (Revision 4.3) may change as new features are added.

The AD_15d4g firmware download module remaps several of the ADF7023-J registers and commands and extends the data sheet state diagram. See the Register Remapping section for more information.

Note that throughout this application note, multifunction pins, such as the ADCIN_ATB3 pin, are referred to either by the entire pin name or by a single function of the pin, for example, ATB3, when only that function is relevant.



[1]GPIO REFERS TO PIN 17, PIN 18, PIN 19, PIN 20, PIN 25, AND PIN 27.

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REVISION HISTORY

3/15—Revision 0: Initial Version

REGISTER REMAPPING

The firmware extends the ADF7023-J data sheet state diagram to include the 15d4g state, as outlined in Figure 2, and extends the firmware states, as defined in Table 3.

When the firmware module is downloaded and the 15d4g state is entered, some of the battery backup random access memory (BBRAM) registers take on new meaning, and some are rendered redundant. The remapped BBRAM registers are defined in Table 1. The command list is expanded, as defined in Table 2. The INTERRUPT_MASK_0 register and the INTERRUPT_SOURCE_0 register are also remapped while in the 15d4g state, as defined in Table 29 and Table 30.

Packet RAM locations 0x20 to 0xFF are available for packet data in the 15d4g state. Bytes 0x00 to 0x1F are allocated for use by the on-chip processor and must not be used for packet data.

When 15d4g state is exited, all normal data sheet functionality is restored. Note, however, that the reused settings must be reprogrammed appropriately according to the data sheet.

Table 1. BBRAM Reuse During 15d4g State

Address (Hex)	Normal Operation	Operation in 15d4g State	Comment
0x100	INTERRUPT_MASK_0	INTERRUPT_MASK_0	Interrupts remapped in 15d4g state
0x101	INTERRUPT_MASK_1	INTERRUPT_MASK_1	
0x102	NUMBER_OF_WAKEUPS_0	Reserved	Do not overwrite in 15d4g state
0x103	NUMBER_OF_WAKEUPS_1	BB_CCA_CFG_0	
0x104	NUMBER_OF_WAKEUPS_IRQ_THRESHOLD_0	BB_CCA_CFG_1	
0x105	NUMBER_OF_WAKEUPS_IRQ_THRESHOLD_1	BB_CCA_THRESHOLD	
0x106	RX_DWELL_TIME	Reserved	Do not overwrite in 15d4g state
0x107	PARMTIME_DIVIDER	PARMTIME_DIVIDER	Not used in 15d4g state
0x108	SWM_RSSI_THRESH	SWM_RSSI_THRESH	Not used in 15d4g state
0x109	CHANNEL_FREQ_0	CHANNEL_FREQ_0	
0x10A	CHANNEL_FREQ_1	CHANNEL_FREQ_1	
0x10B	CHANNEL_FREQ_2	CHANNEL_FREQ_2	
0x10C	RADIO_CFG_0	RADIO_CFG_0	
0x10D	RADIO_CFG_1	RADIO_CFG_1	
0x10E	RADIO_CFG_2	RADIO_CFG_2	
0x10F	RADIO_CFG_3	RADIO_CFG_3	
0x110	RADIO_CFG_4	RADIO_CFG_4	
0x111	RADIO_CFG_5	RADIO_CFG_5	
0x112	RADIO_CFG_6	RADIO_CFG_6	
0x113	RADIO_CFG_7	RADIO_CFG_7	
0x114	RADIO_CFG_8	RADIO_CFG_8	
0x115	RADIO_CFG_9	RADIO_CFG_9	
0x116	RADIO_CFG_10	RADIO_CFG_10	
0x117	RADIO_CFG_11	RADIO_CFG_11	
0x118	IMAGE_REJECT_CAL_PHASE	IMAGE_REJECT_CAL_PHASE	
0x119	IMAGE_REJECT_CAL_AMPLITUDE	IMAGE_REJECT_CAL_AMPLITUDE	
0x11A	MODE_CONTROL	MODE_CONTROL	
0x11B	PREAMBLE_MATCH	PREAMBLE_MATCH	
0x11C	SYMBOL_MODE	SYMBOL_MODE	
0x11D	PREAMBLE_LEN	PREAMBLE_LEN	
0x11E	CRC_POLY_0	CRC_POLY_0	
0x11F	CRC_POLY_1	CRC_POLY_1	
0x120	SYNC_CONTROL	SYNC_CONTROL	
0x121	SYNC_BYTE_0	SYNC_BYTE_0	
0x122	SYNC_BYTE_1	SYNC_BYTE_1	
0x123	SYNC_BYTE_2	SYNC_BYTE_2	
0x124	TX_BASE_ADR	TX_BASE_ADR	
0x125	RX_BASE_ADR	RX_BASE_ADR	
0x126	PACKET_LENGTH_CONTROL	PACKET_LENGTH_CONTROL	

Address (Hex)	Normal Operation	Operation in 15d4g State	Comment
0x127	PACKET_LENGTH_MAX	PACKET_LENGTH_MAX	
0x128	STATIC_REG_FIX	RESERVED	Set to 0 for 15d4g state
0x129	ADDRESS_MATCH_OFFSET	BB_RX_ANTENNA_DIVERSITY_CFG	
0x12A	ADDRESS_LENGTH	BB_TX_ANTENNA_CFG	
0x12B	Address matching	BB_ANTENNA0_RSSI	
0x12C	Address matching	BB_ANTENNA1_RSSI	
0x12D	Address matching	BB_THRESHOLD_DIFF_RSSI	
0x12E	Address matching	BB_NB_PREAMBLE_BYTES_LOW	
0x12F	Address matching	BB_NB_PREAMBLE_BYTES_HIGH	
0x130	Address matching	BB_SFD_LOW	
0x131	Address matching	BB_SFD_HIGH	
0x132	Address matching	BB_PHR_LOW	Controlled by firmware in 15d4g state
0x133	Address matching	BB_PHR_HIGH	Controlled by firmware in 15d4g state
0x134	Address matching	BB_RX_BUFFER_SIGNAL	
0x135	Address matching	BB_RX_BUFFER_SIZE	
0x136	Address matching	BB_TX_BUFFER_SIGNAL	
0x137	Address matching	BB_TX_BUFFER_SIZE	
0x138	RSSI_WAIT_TIME	Reserved	Set to 0x00 for 15d4g state
0x139	TESTMODES	BB_TESTMODES	
0x13A	TRANSITION_CLOCK_DIV	Reserved	Set to 0x01 for 15d4g state
0x13B	Reserved	BB_VCO_BAND_READBACK	
0x13C	Reserved	BB_VCO_AMP_READBACK	
0x13D	Reserved	Reserved	
0x13E	RX_SYNTH_LOCK_TIME	RX_SYNTH_LOCK_TIME	
0x13F	TX_SYNTH_LOCK_TIME	TX_SYNTH_LOCK_TIME	
0x01F	Packet data	PHY_RX_STATUS	Packet RAM used in 15d4g state

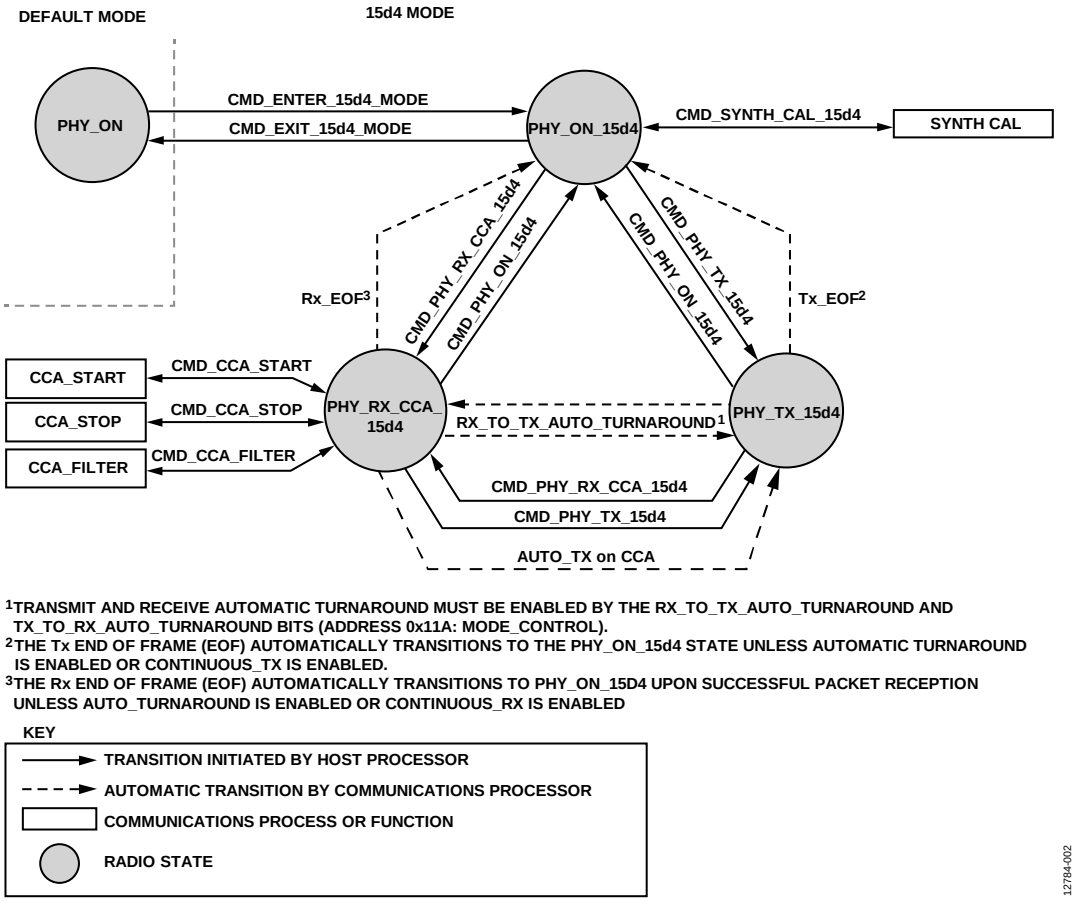

Figure 2. 15d4g State Diagram

Table 2. Commands and States Included in the Firmware Download

Command/Bit	Command Code	Present State	Next State
CMD_ENTER_15d4_MODE	0xC1	PHY_ON	PHY_ON_15d4
CMD_EXIT_15d4_MODE	0xB1	PHY_ON_15d4	PHY_ON
CMD_PHY_RX_CCA_15d4	0xB2	PHY_ON_15d4, PHY_TX_15d4, PHY_RX_CCA_15d4	PHY_RX_CCA_15d4
CMD_PHY_TX_15d4	0xB5	PHY_ON_15d4, PHY_RX_CCA_15d4	PHY_TX_15d4
CMD_PHY_ON_15d4	0xB1	PHY_RX_CCA_15d4, PHY_TX_15d4	PHY_ON_15d4
CMD_SYNTH_CAL_15d4	0xEE	PHY_ON_15d4	PHY_ON_15d4
CMD_CCA_START	0xB7	PHY_RX_CCA_15d4	PHY_RX_CCA_15d4
CMD_CCA_STOP	0xB8	PHY_RX_CCA_15d4	PHY_RX_CCA_15d4
CMD_CCA_FILTER	0xB9	PHY_RX_CCA_15d4	PHY_RX_CCA_15d4
CMD_CONFIG_DEV	0xBB	PHY_ON_15d4	PHY_ON_15d4

Table 3. FW_STATE Description

Value	State	Description
0x18	PHY_ON_15d4	The device is ready to operate in 15d4 mode, and PHY_RX_CCA_15d4 and PHY_TX_15d4 states can be entered.
0x1A	PHY_RX_CCA_15d4	The device is in 15d4 receive mode where valid 15d4 packets can be received, CCA and antenna diversity can be enabled. After reception of a valid packet, the device can return to the PHY_ON_15d4 state, can remain in the PHY_RX_CCA_15d4 state, or can transition to the PHY_TX_15d4 state depending on the user settings.
0x1C	PHY_TX_15d4	The device is in 15d4 transmit mode, where it automatically transmits the transmit packet stored in packet RAM. After transmission of the packet, the device can return to the PHY_ON_15d4 state, can remain in the PHY_TX_15d4 state, or can transition to the PHY_RX_CCA_15d4 state depending on the user settings.

REGISTER MAP EXTENSION

Table 4. Registers for Use with AD_15d4g Firmware Download

Address (Hex)	Register	Description
C)27(C)13.70(A)503 ref20.253)TI	2.33.7230_CFG_w 99.1(.0224)-11(0..3(9.1(0.o)	6(4(Configuration Word 2 6(48.42)49(i)- ref127(64.6 663.24 0.48 0.481 re27(64.6 663.24 0.48 0. 0.4

REGISTER DESCRIPTIONS

Table 5. Address 0x103: BB_CCA_CFG_0

Bits	Name	Access	Description
7	CCA_STATUS	R/W	Indicates if channel is clear (0) or busy (1).
[6:5]	CCA_FILTER_BW	R/W	CCA_FILTER_BW sets the intermediate frequency (IF) filter bandwidth for CCA RSSI. 00: 100 kHz. 01: 150 kHz. 10: 200 kHz. 11: 300 kHz.
4	CCA_AUTO_TX	R/W	1: remain in the PHY_RX_CCA_15d4 state (manual Tx) on CCA. This is for use with CCA infinity mode. 0: automatic Tx on CCA. This is for use with CCA timer mode.
[3:1]	CCA_TIMER	R/W	CCA_TIMER selects one of eight timer options. 000: 160 µs. 001: 320 µs. 010: 640 µs. 011: 1280 µs. 100: 1920 µs. 101: 2560 µs. 110: 9960 µs. 111: infinity mode.
0	CCA_BYPASS_UPDATE	R/W	Debug mode only. For normal use, set to 0. 0: CCA data is updated every byte (normal use). 1: CCA data is not updated every byte (debug mode only, causes the CCA_STATUS bit to be frozen).

Table 6. Address 0x104: BB_CCA_CFG_1

Bits	Name	Access	Description
7	CCA_LIVE_STATUS	R/W	Live indication if channel is clear (0) or busy (1).
6	ENABLE_IFBW_SWITCH_ON_PREAMBLE	R/W	1: changes bandwidth when preamble is detected. 0: keep bandwidth when preamble is detected.
5	ENABLE_IFBW_AUTO_SWITCH	R/W	1: changes bandwidth when CMD_CCA_START is issued. 0: keep default bandwidth when CMD_CCA_START is issued.
4	WAIT_FOR_HOST_EOCCA	R/W	Debug mode only. For normal use, set to 0. 1: wait for host at end of CCA timer after CCA trigger (debug mode only). 0: continue to update CCA registers on CCA timer timeout (normal use).
[3:0]	Reserved	R/W	Set to 0.

Table 7. Address 0x105: BB_CCA_THRESHOLD

Bits	Name	Access	Description
[7:0]	CCA_THRESHOLD	R/W	This is an 8-bit number representing the CCA RSSI threshold in dBm. CCA_THRESHOLD = RSSI (dBm) + 107

Table 8. Address 0x129: BB_RX_ANTENNA_DIVERSITY_CFG

Bits	Name	Access	Description
[7:6]	RX_ANTENNA_DIVERSITY_CFG_PATH_ANT_0	R/W	Maps the Rx Antenna 0 path to the ATB pins Bit 7 = ATB1/ATB3, 0 = low, 1 = high Bit 6 = ATB2/ATB4, 0 = low, 1 = high
[5:4]	RX_ANTENNA_DIVERSITY_CFG_PATH_ANT_1	R/W	Maps the Rx Antenna 1 path to the ATB pins Bit 5 = ATB1/ATB3, 0 = low, 1 = high Bit 4 = ATB2/ATB4, 0 = low, 1 = high
3	RX_ATB_LEVEL	R/W	1: select to use 1.8 V drivers (ATB3 and ATB4) 0: select to use V_{DD} drivers (ATB1 and ATB2)
2	Reserved	R/W	Set to 0
1	ANTENNA_SELECTED	R/W	If the ANTENNA_DIVERSITY_ENABLE bit = 1, this bit reports the antenna selected by the diversity algorithm: 0 = Antenna 0 1 = Antenna 1 If the ANTENNA_DIVERSITY_ENABLE bit = 0, this bit selects the receive antenna: 0 = Antenna 0 (using the RX_ANTENNA_DIVERSITY_CFG_PATH_ANT_0 bit mapping 1 = Antenna 1 (using the RX_ANTENNA_DIVERSITY_CFG_PATH_ANT_1 bit mapping)
0	ANTENNA_DIVERSITY_ENABLE	R/W	1 = enable antenna diversity algorithm (and autoselect the Rx antenna) 0 = disable antenna diversity algorithm (and manually select the Rx antenna)

Table 9. Address 0x12A: BB_TX_ANTENNA_CFG

Bits	Name	Access	Description
[7:6]	TX_ANTENNA_CFG_PATH_ANT_0	R/W	Maps the Tx Antenna 0 path to the ATB bits Bit 7 = ATB1/ATB3, 0 = low, 1 = high Bit 6 = ATB2/ATB4, 0 = low, 1 = high
[5:4]	TX_ANTENNA_CFG_PATH_ANT_1	R/W	Maps the Tx Antenna 1 path to ATB bits Bit 5 = ATB1/ATB3, 0 = low, 1 = high Bit 4 = ATB2/ATB4, 0 = low, 1 = high
3	TX_ATB_LEVEL	R/W	1: selects to use 1.8 V drivers (ATB3 and ATB4) 0: selects to use V_{DD} drivers (ATB1 and ATB2)
2	Reserved	R/W	Set to 0
1	TX_ANTENNA	R/W	This bit selects the transmit antenna 0 = Antenna 0 (using the TX_ANTENNA_DIVERSITY_CFG_PATH_ANT_0 bit mapping) 1= Antenna 1 (using the TX_ANTENNA_DIVERSITY_CFG_PATH_ANT_1 bit mapping)
0	Reserved	R/W	Set to 0

Table 10. Address 0x12B: BB_ANTENNA0_RSSI

Bits	Name	Access	Description
[7:0]	ANTENNA0_RSSI_READBACK	R/W	This register contains the RSSI value measured on Antenna 0: RSSI (dBm) = ANTENNA0_RSSI_READBACK – 107

Table 11. Address 0x12C: BB_ANTENNA1_RSSI

Bits	Name	Access	Description
[7:0]	ANTENNA1_RSSI_READBACK	R/W	This register contains the RSSI value measured on Antenna 1: RSSI (dBm) = ANTENNA1_RSSI_READBACK – 107

Table 12. Address 0x12D: BB_THRESHOLD_DIFF_RSSI

Bits	Name	Access	Description
[7:0]	THRESHOLD_DIFF_RSSI	R/W	Difference between the CCA_THRESHOLD and the most recent RSSI value evaluated

Table 13. Address 0x12E: BB_NB_PREAMBLE_BYTES_LOW

Bits	Name	Access	Description
[7:0]	NB_PREAMBLE_BYTES_LOW	R/W	Bits[7:0]of the NB_PREAMBLE_BYTES word

Table 14. Address 0x12F: BB_NB_PREAMBLE_BYTES_HIGH

Bits	Name	Access	Description
[7:0]	NB_PREAMBLE_BYTES_HIGH	R/W	Bits[15:8] of the NB_PREAMBLE_BYTES word. Note that valid values are within the range, 4 ≤ the NB_PREAMBLE_BYTES word ≤ 1000

Table 15. Address 0x130: BB_SFD_LOW

Bits	Name	Access	Description
[7:0]	BB_SFD_LOW	R/W	Bits[7:0] of the SFD word (see Table 34)

Table 16. Address 0x131: BB_SFD_HIGH

Bits	Name	Access	Description
[7:0]	BB_SFD_HIGH	R/W	Bits[15:8] of the SFD word. For supported SFD values, see Table 34.

The values in Address 0x132 (the BB_PHR_LOW register) are read only. In receive mode, the values are copied in by the AD_15d4g firmware download module from a received packet. In transmit mode, the required PHR value for a transmit must be written to the TX_BASE_ADR register and the firmware reflects those values back in Address 0x132.

Table 17. Address 0x132: BB_PHR_LOW

Bits	Name	Access	Description
7	MODE_SWITCH	R	Indicates if the packet is a mode switch packet.
[6:5]	Reserved	R	Set to 0.
4	FCS	R	0 = 32-bit frame check sequence (FCS); 1 = 16-bit FCS. Note that only a 16-bit FCS is automatically handled by the ADF7023-J. A 32-bit FCS must be calculated by the user. For a 32-bit FCS Tx, the user must calculate the FCS and add to the end of the payload. For a 32-bit FCS Rx, the user must calculate the cyclic redundancy check (CRC) and compare with the last four bytes received into the packet RAM. In a 32-bit FCS Rx, a CRC correct interrupt is never generated. The INTERRUPT_RX_EOF interrupt signifies the end of packet reception.
3	Whitening	R	1 = PHY service data unit (PSDU) whitened.
[2:0]	PSDU_LENGTH_HI	R	Bits[10:8] of the PSDU_LENGTH[10:0] word.

The values in Address 0x133 (the BB_PHR_HIGH register) are read only. In receive mode, the values are copied in by the AD_15d4g firmware download module from a received packet. In transmit mode, the required PHR value for a transmit must be written to the TX_BASE_ADR register and the firmware reflects those values back in Address 0x133.

Table 18. Address 0x133: BB_PHR_HIGH

Bits	Name	Access	Description
[7:0]	PSDU_LENGTH_LO	R	Bits[7:0] of the PSDU_LENGTH[10:0] word. Note that valid values are within the range, 2 < the PSDU_LENGTH[10:0] word < 2048

Table 19. Address 0x134: BB_RX_BUFFER_SIGNAL

Bits	Name	Access	Description
[7:0]	RX_BUFFER_SIGNAL	R/W	The rolling buffer fills from the RX_BASE_ADR register with data. When the buffer reaches location, RX_BASE_ADR + RX_BUFFER_SIGNAL, the INTERRUPT_BUFFER_ALMOST_FULL interrupt is generated. Note that the contents of RX_BUFFER_SIGNAL must be greater than 2.

Table 20. Address 0x135: BB_RX_BUFFER_SIZE

Bits	Name	Access	Description
[7:0]	RX_BUFFER_SIZE	R/W	This is the maximum size of the Rx buffer. When the location, RX_BASE_ADR + RX_BUFFER_SIZE, is filled with data, an INTERRUPT_BUFFER_FULL interrupt is generated, and the buffer loops back to location RX_BASE_ADR and continues to fill from there. Note that RX_BUFFER_SIZE must have a value greater than 2 and that, for a 16-bit FCS case, a 2-byte overflow area is required after the RX_BUFFER_SIZE register.

Table 21. Address 0x136: BB_TX_BUFFER_SIGNAL

Bits	Name	Access	Description
[7:0]	TX_BUFFER_SIGNAL	R/W	The rolling buffer sends from the TX_BASE_ADR register with data. When the buffer reaches and sends from location, TX_BASE_ADR + TX_BUFFER_SIGNAL, an INTERRUPT_BUFFER_ALMOST_FULL interrupt is generated. Note that TX_BUFFER_SIGNAL must have a value greater than 2.

Table 22. Address 0x137: BB_TX_BUFFER_SIZE

Bits	Name	Access	Description
[7:0]	TX_BUFFER_SIZE	R/W	This is the maximum size of the Tx buffer. When the data from location, TX_BASE_ADR + TX_BUFFER_SIZE, is sent, an INTERRUPT_BUFFER_FULL interrupt is generated, and the buffer loops back to location TX_BASE_ADR and continues to send from there. Note that TX_BUFFER_SIZE must have a value greater than 2.

Table 23. Address 0x138: Reserved

Bits	Name	Access	Description
[7:0]	Reserved	R/W	Set to 0

Table 24. Address 0x139: BB_TESTMODES

Bits	Name	Access	Description
[7:2]	Reserved	R/W	Set to 0
1	BIT_CONTINUOUS_TX	R/W	1: device remains in the PHY_TX_15d4 state after packet transmission 0: device returns to the PHY_ON_15d4 state after packet transmission
0	BIT_CONTINUOUS_RX	R/W	1: device remains in the PHY_RX_CCA_15d4 state after packet reception 0: device returns to the PHY_ON_15d4 state after packet reception

Table 25. Address 0x13A: Reserved

Bits	Name	Access	Description
[7:1]	Reserved	R/W	Set to 0
0	Reserved	R/W	Set to 1

Table 26. Address 0x13B: BB_VCO_BAND_READBACK

Bits	Name	Access	Description
[7:0]	VCO_BAND_READBACK	R/W	Stores the VCO band calibration results after synthesizer calibration, for fast Tx/Rx transitions

Table 27. Address 0x13C: BB_VCO_AMPL_READBACK

Bits	Name	Access	Description
[7:0]	VCO_AMPL_READBACK	R/W	Stores the VCO amplitude calibration results after synthesizer calibration, for fast Tx/Rx transitions

Table 28. Address 0x01F: PHY_RX_STATUS

Bits	Name	Access	Description
[7:2]	Reserved	R	Reserved
1	SFD_RX_STATUS	R	1: SFD detected 0: SFD not detected
0	PREAMBLE_RX_STATUS	R	1: preamble detected 0: preamble not detected

INTERRUPT MASK AND SOURCE CONFIGURATIONS

Table 29. Address 0x100: INTERRUPT_MASK_0

Bit	Name	Access	Description
7	INTERRUPT_CCA	R/W	In timer mode, interrupt after CCA period has expired. (The CCA_STATUS flag indicates if the channel is busy or clear.) In infinity mode, interrupt when the channel is clear. 1: interrupt enabled; 0: interrupt disabled.
6	INTERRUPT_BUFFER_FULL	R/W	Interrupt when the Rx or Tx buffer is full. 1: interrupt enabled; 0: interrupt disabled.
5	INTERRUPT_BUFFER_ALMOST_FULL	R/W	Interrupt when the Rx or Tx buffer is almost full. 1: interrupt enabled; 0: interrupt disabled.
4	INTERRUPT_RX_EOF	R/W	Interrupt when a packet has finished receiving. 1: interrupt enabled; 0: interrupt disabled.
3	INTERRUPT_TX_EOF	R/W	Interrupt when a packet has finished transmitting. 1: interrupt enabled; 0: interrupt disabled.
2	INTERRUPT_CRC_CORRECT	R/W	Interrupt when a received packet has the correct CRC. 1: interrupt enabled; 0: interrupt disabled.
1	INTERRUPT_PHR_DETECT	R/W	Interrupt when PHR has been detected in the received packet. The interrupt is generated when SFD is detected, but is delayed and issued at the end of PHR reception. 1: interrupt enabled; 0: interrupt disabled.
0	INTERRUPT_PREAMBLE_DETECT	R/W	Interrupt when a qualified preamble is in the received packet. 1: interrupt enabled; 0: interrupt disabled.

Table 30. Address 0x336: INTERRUPT_SOURCE_0

Bit	Name	Access	Reset	Description
7	INTERRUPT_CCA	R/W	0	In timer mode, after CCA period has expired, a CCA interrupt is asserted. In infinity mode, the INTERRUPT_CCA interrupt is asserted only when the channel is clear.
6	INTERRUPT_BUFFER_FULL	R/W	0	Asserted when the Rx or Tx buffer is full (Rx or Tx buffer size is reached).
5	INTERRUPT_BUFFER_ALMOST_FULL	R/W	0	Asserted when the Rx or Tx buffer is almost full (Rx or Tx buffer signal is reached).
4	INTERRUPT_RX_EOF	R/W	0	Asserted when a packet has finished receiving.
3	INTERRUPT_TX_EOF	R/W	0	Asserted when a packet has finished transmitting.
2	INTERRUPT_CRC_CORRECT	R/W	0	Asserted when a received packet has the correct CRC.
1	INTERRUPT_PHR_DETECT	R/W	0	Asserted when PHR is detected in the received packet.
0	INTERRUPT_PREAMBLE_DETECT	R/W	0	Asserted when a qualified preamble is detected in the received packet.

ANTENNA SIGNAL PATH CONTROL

FAST Tx/Rx TRANSITIONS

The AD_15d4g firmware download module supports fast transitions from the PHY_ON_15d4 state to the PHY_TX_15d4 state and the PHY_RX_CCA_15d4 state. The fast transitions are achieved by the following sequence:

1. Issue the CMD_SYNTH_CAL_15d4 command (Command 0xEE) while in the PHY_ON_15d4 state. A synthesizer calibration is performed at the programmed channel frequency, and the results are stored in the BB_VCO_BAND_READBACK register (Address 0x13B) and the BB_VCO_AMP_READBACK register (Address 0x13C).
2. Enable synthesizer calibration overwrite by setting VCO_OVRW_EN (Address 0x3CD) to 0x3.

The CMD_PHY_RX_CCA_15d4 command and the CMD_PHY_TX_15d4 command complete in a shorter time after this sequence, because a synthesizer calibration is no longer performed.

Note that it is good practice to periodically perform a full synthesizer calibration. A full synthesizer calibration maintains optimum RF performance across fluctuations in operating temperature or battery voltage.

ANTENNA DIVERSITY

In addition to propagation loss, channel impairments, such as multipath and signal fading, can degrade the performance and robustness of a wireless communication link.

The propagation of an electromagnetic wave is subject to impairments such as reflections, refractions, and scattering along its path, as illustrated in Figure 3. At the input to a receiver, multiple copies of the transmitted signal can arrive at slightly different times and have varying amplitudes. These multipath signals superimpose and result in constructive or destructive interference in the composite signal seen at the input to the receiver.

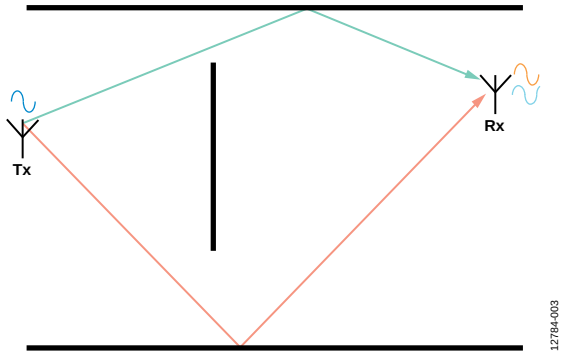

Figure 3. Multipath Propagation

To combat this issue, antenna diversity techniques can be used to improve the performance of the radio link. By measuring the signal quality from two antennas that are physically separate, the antenna with the highest quality signal can be directed to the input of the receiver. By physically separating the antennas, the probability that both antennas suffer the same fading characteristics at the same time is significantly reduced.

The technique employed by the ADF7023-J firmware download is a switched diversity technique. In receive mode, an external RF switch (for example, a double pole, double throw (DPDT) switch) is used to select a signal from one of two antennas, as shown in Figure 4. The ATB1 and ATB2 pins provide logic control of the RF diversity switch from the ADF7023-J. The ADF7023-J also offers the flexibility to assign any combination of logic states (00, 01, 10, 11) to the switch control pins, ATB1 and ATB2. This configurable polarity scheme supports control of a wide range of RF switch topologies. The maximum logic output level from the ATB1 and ATB2 pins is V_{DD}. If 1.8 V logic levels are required, use the ATB3 and ATB4 pins. See the Antenna Signal Path Control section for more details on the configuration of these pins.

The ADF7023-J evaluates the quality of the received signal from either antenna by the use of a dual qualification process: by qualifying the existence of a valid preamble sequence (101010…) and by measuring the power level (RSSI). This two-level qualification process ensures high quality signal integrity at the input to the receiver and ensures sufficient signal-to-noise ratio (SNR) for packet reception.

After a packet is received, if continuous Rx is enabled (Address 0x139, Bit 0 = 1), the ADF7023-J remains in receive mode with the algorithm continuing to evaluate signal quality from both paths. If continuous Rx is not enabled, the ADF7023-J returns to the PHY_ON_15d4 state after packet reception.

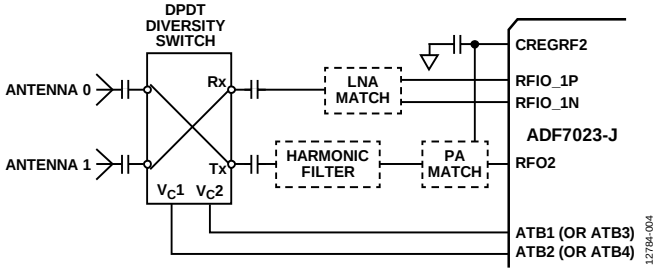

Figure 4. Typical Antenna Diversity Hardware

The diversity algorithm is most effective at input power levels close to the sensitivity level of the receiver. In such conditions, if antenna diversity is not used, the packet error rate (PER) performance of the receiver can be significantly degraded due to multipath and signal fading loss. With diversity enabled, the likelihood of fading occurring on both antennas at the same time is significantly diminished and the ADF7023-J firmware automatically selects an antenna with the highest SNR.

ANTENNA DIVERSITY ALGORITHM

Antenna diversity is enabled by setting Bit 0 of the BB_RX_ANTENNA_DIVERSITY_CFG register (Address 0x129) to 1.

Upon entering the PHY_RX_CCA_15d4 state with antenna diversity enabled, the signal on each antenna is evaluated, switching between antennas with a fixed search timer period.

The algorithm operates as follows:

- The ADF7023-J performs both preamble qualification and RSSI measurement on both antennas. During preamble qualification, the received bit stream is correlated against a fixed number of 10 preamble bit pairs in the ADF7023-J.
- RSSI measurement is also performed during this search period.
- After the antenna search period has expired, the same preamble qualification and RSSI measurement is performed on the second antenna.
- When a valid preamble sequence is detected on both antennas, the antenna with the largest RSSI reading is used for reception.
- When a valid preamble sequence is detected only on one antenna, this antenna is selected for reception of the packet.
- If the preamble sequence is not qualified on either antenna, the algorithm continues to switch between both antennas at the search period rate.

After completing packet reception, if the BIT_CONTINUOUS_RX bit, Bit 0 of the BB_TESTMODES register (Address 0x139), = 1, the device returns to the PHY_RX_CCA_15d4 antenna search state and the diversity algorithm continues to evaluate both antennas. Note that as the device transitions back to the PHY_RX_CCA_15d4 state, the interrupts are not automatically cleared (see Figure 5).

If the BIT_CONTINUOUS_RX bit = 0, the device returns to the PHY_ON_15d4 state at the end of packet reception, and the identification of the antenna selected can be read back from the value in Bit 1 of the BB_RX_ANTENNA_DIVERSITY_CFG register.

The Antenna RSSI values can be read back from Address 0x12B (Antenna 0) and Address 0x12C (Antenna 1) (see Figure 6).

The mapping of the control bits to configure the antenna paths is programmable in Bits[7:6] and Bits[5:4] of the BB_RX_ANTENNA_DIVERSITY_CFG register (Address 0x129).

These control bits appear at the ATB1 and ATB2 pins as V_{DD} logic levels, or at the ATB3 and ATB4 pins as 1.8 V logic levels. Select between V_{DD} or 1.8 V levels using the RX_ATB_LEVEL bit, Bit 3 of the BB_RX_ANTENNA_DIVERSITY_CFG register (Address 0x129).

See the Antenna Signal Path Control section for more details.

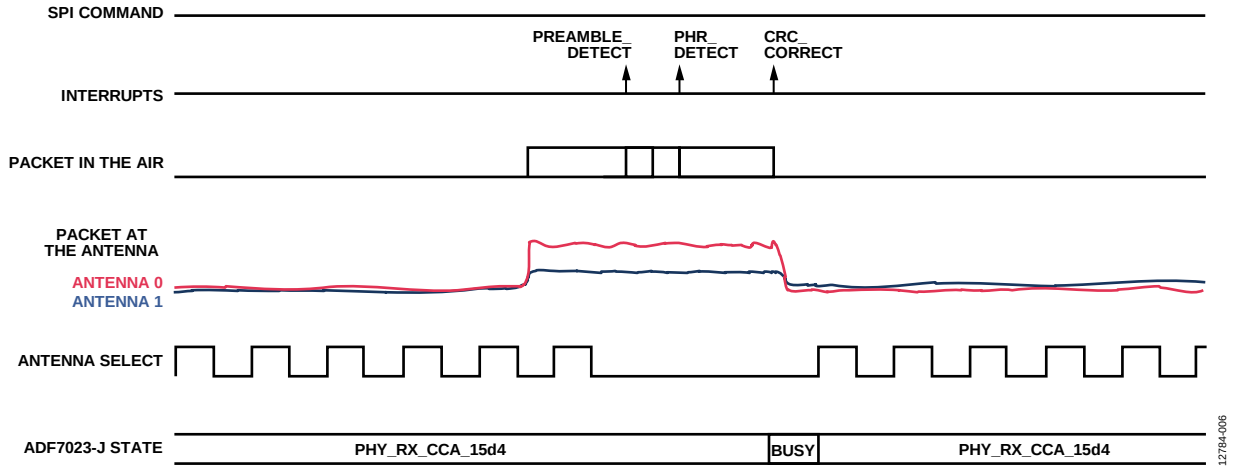

Figure 5. Antenna Diversity Timing with Continuous Rx

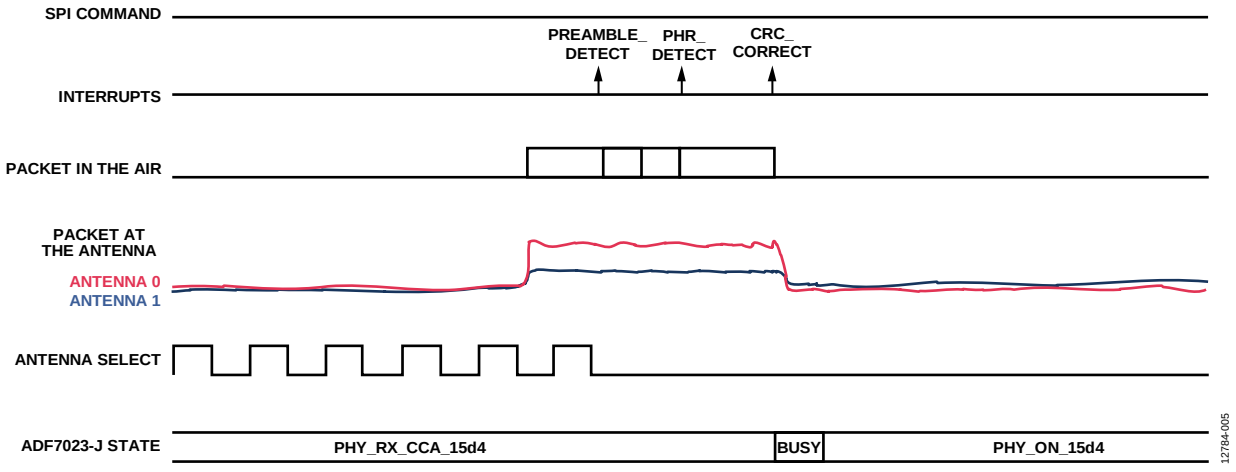

Figure 6. Antenna Diversity Timing, the BIT_CONTINUOUS_RX Bit = 0

PERFORMANCE IN A FADING ENVIRONMENT

The performance of this algorithm was measured under the following conditions:

- Preamble length = 10 bytes
- Payload length = 12 bytes
- Data rate = 100 kbps
- Modulation index = 1
- Rayleigh fading
- Fading pitch = 4 Hz
- Correlation between antennas: 0% and 100% (100% correlation is equivalent to the single antenna case in a fading environment)

Under these conditions, a diversity gain of >9 dB was achieved at the 1% PER point (see Figure 7).

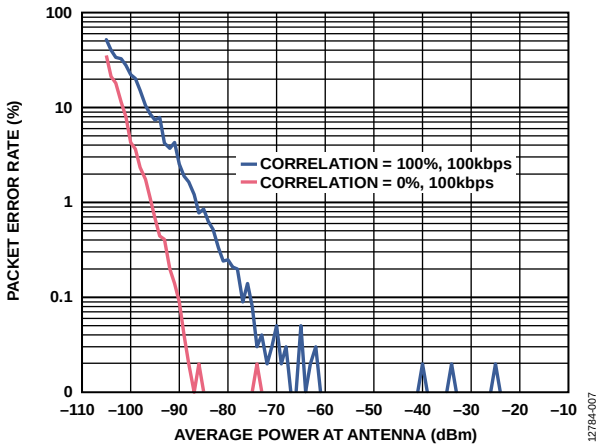

Figure 7. Performance Results: Antenna Diversity Gain in a Fading Environment

CLEAR CHANNEL ASSESSMENT

For clear channel assessment, the CCA threshold is programmed into the BB_CCA_THRESHOLD register (Address 0x105). If the measured RSSI is above this threshold, the channel is busy. If the measured RSSI is below this threshold, the channel is clear.

Evaluation of CCA and RSSI is automatically activated upon entering the PHY_RX_CCA_15d4 state. Multiple times per byte, the RSSI value is evaluated, and the CCA_LIVE_STATUS flag is updated to busy or clear. Thus, after entering the PHY_RX_CCA_15d4 state, the RSSI value and a live CCA status are always updated unless updates are turned off with the CCA_BYPASS_UPDATE bit (Bit 0 of Address 0x103).

Note that there is a time lag until the first RSSI value is updated upon first entering the PHY_RX_CCA_15d4 state. Until the first RSSI value is updated, the previously measured RSSI value is retained. To clear the previously measured RSSI value, the BB_ANTENNA0_RSSI and BB_ANTENNA1_RSSI registers can be zeroed before entering the PHY_RX_CCA_15d4 state.

The ADF7023-J firmware download module can support CCA and antenna diversity at the same time.

When antenna diversity is enabled, the RSSI value on the current antenna is evaluated multiple times every byte, while the value on the alternate antenna is held at its last measured value. When the antenna switches, the RSSI on the deselected antenna is held, and the RSSI on the currently selected antenna is updated. The CCA_LIVE_STATUS bit is updated continuously to signify if the measured RSSI is above or below the CCA threshold. Any excursion above the CCA threshold sets the CCA_STATUS bit to busy.

When antenna diversity is not enabled, only the RSSI on the current antenna is evaluated and compared with the CCA threshold to determine if the channel is busy or clear, and update the CCA_STATUS flag accordingly.

There are two distinct modes of operation: timer mode and infinity mode. These modes are discussed in the CCA Timer Mode section and the CCA Infinity Mode section.

CCA TIMER MODE

CCA timer mode is used with automatic Tx (the BB_CCA_CFG_0 register, Bit 4 = 0), and is initiated by the CMD_CCA_START command.

In timer mode, the CCA evaluation period is programmable in CCA_TIMER in the BB_CCA_CFG_0 register. This is a timer in µs, as defined in Table 33.

In timer mode, the timer is initiated and the evaluation period is started by the CMD_CCA_START command. When the timer times out, or the timer is interrupted by an incoming packet, the CCA interrupt is generated (if it is enabled). Note that there is an internal overhead on the timer mode, which means the CCA evaluation period is somewhat less than the CCA timer value. In particular, for the 160 µs timer, under certain conditions, the CCA evaluation time is less than 128 µs. Therefore, it is recommended that, if Timer 000 is used, users perform their own characterization tests to ensure performance, per TELEC requirements.

Table 33. CCA Timer Mode Times

Timer Option	Evaluation Period Time (µs)
000	160
001	320
010	640
011	1280
100	1920
101	2560
110	9960

The CCA_STATUS bit is automatically cleared at the beginning of every evaluation period (channel free). If the CCA_LIVE_STATUS bit goes high (becomes busy) at any stage during the evaluation period, the CCA_STATUS flag is automatically updated to busy.

CCA timer mode is used with automatic Tx (the BB_CCA_CFG_0 register, Bit 4 = 0) only. If the channel is clear, and automatic Tx is enabled, the device transitions automatically to the PHY_TX_15d4 state (see Figure 8).

If the channel is busy and the timer times out, a CCA interrupt is generated, and the device remains in the PHY_RX_CCA_15d4 state, with the CCA_STATUS bit set to busy (see Figure 9).

It is important to note that the RSSI value is continuously updated and evaluated during each byte period. Therefore, in antenna diversity mode, to ensure that both antennas are evaluated before making a CCA judgment, the CCA timer must be ≥4 bytes.

During CCA timer mode, incoming packets can be received.

If an SFD is detected on the best antenna, any running CCA timer is terminated and the CCA interrupt is asserted after SFD detection. The CCA_STATUS bit is set to busy. The packet continues to be received normally (see Figure 10).

If the CCA timer times out during the preamble or SFD of an incoming packet, that packet is lost and the CCA interrupt is generated (see Figure 11).

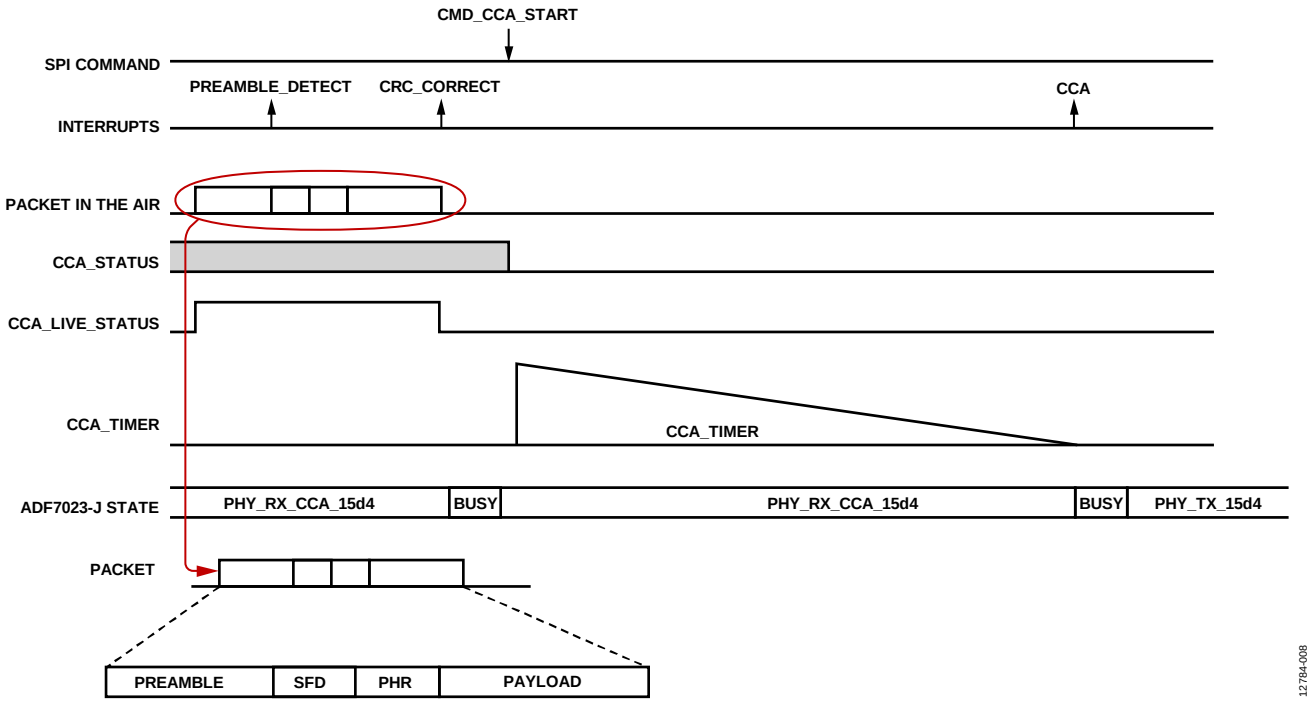

Figure 8. CCA Timer Mode, Channel Clear, Automatic Tx

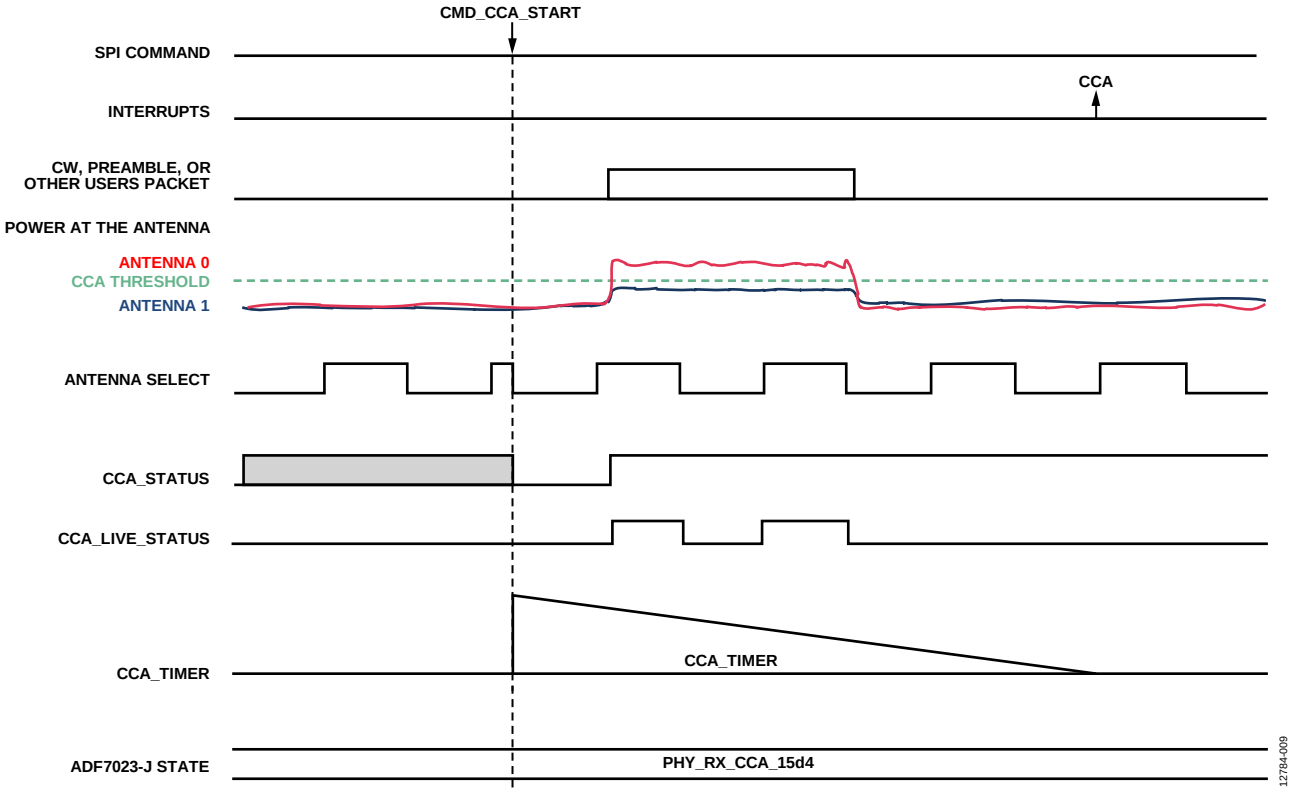

Figure 9. CCA Timer Mode, Antenna Diversity Enabled, Channel Busy

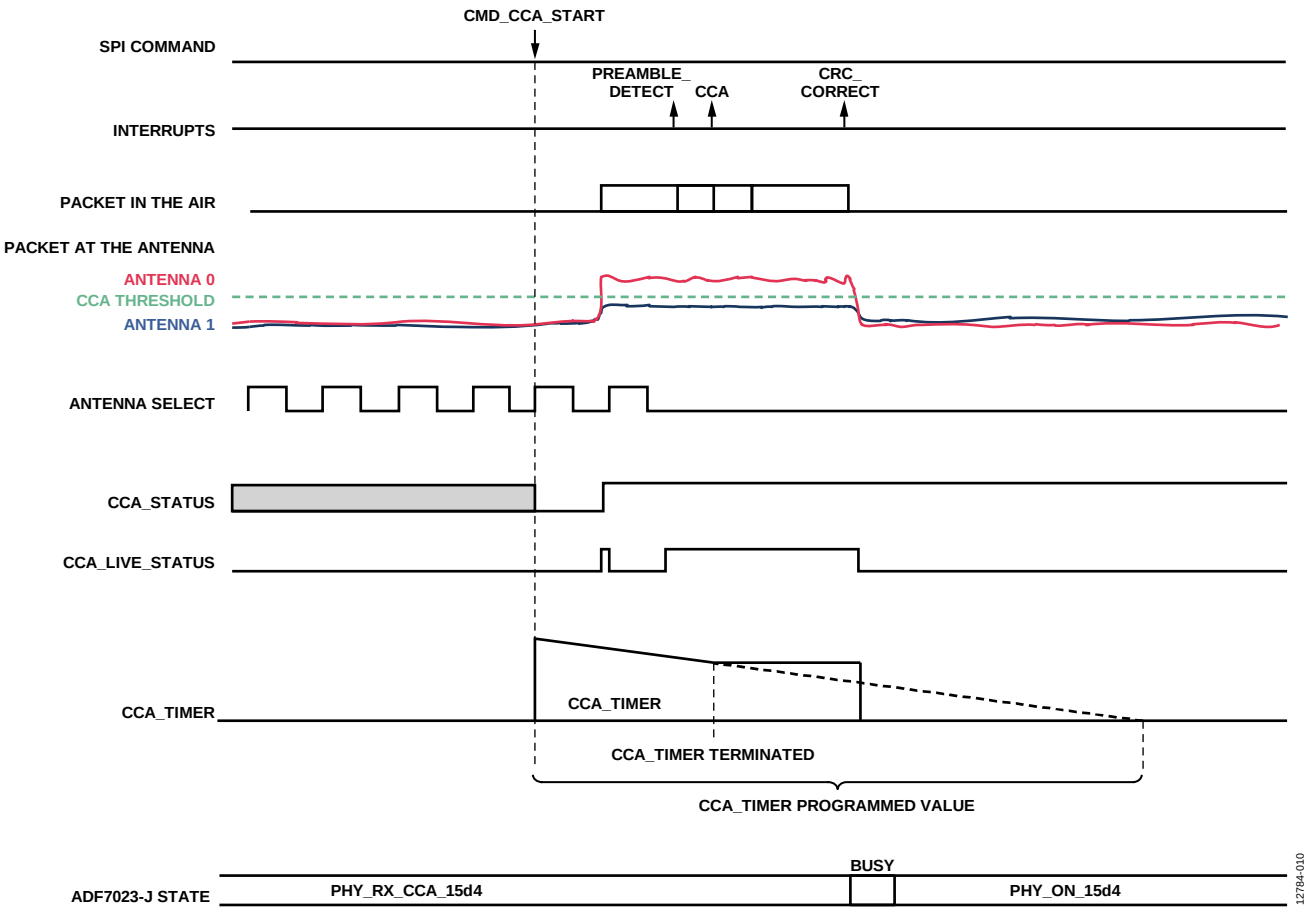

Figure 10. Packet Reception During CCA Timer Mode

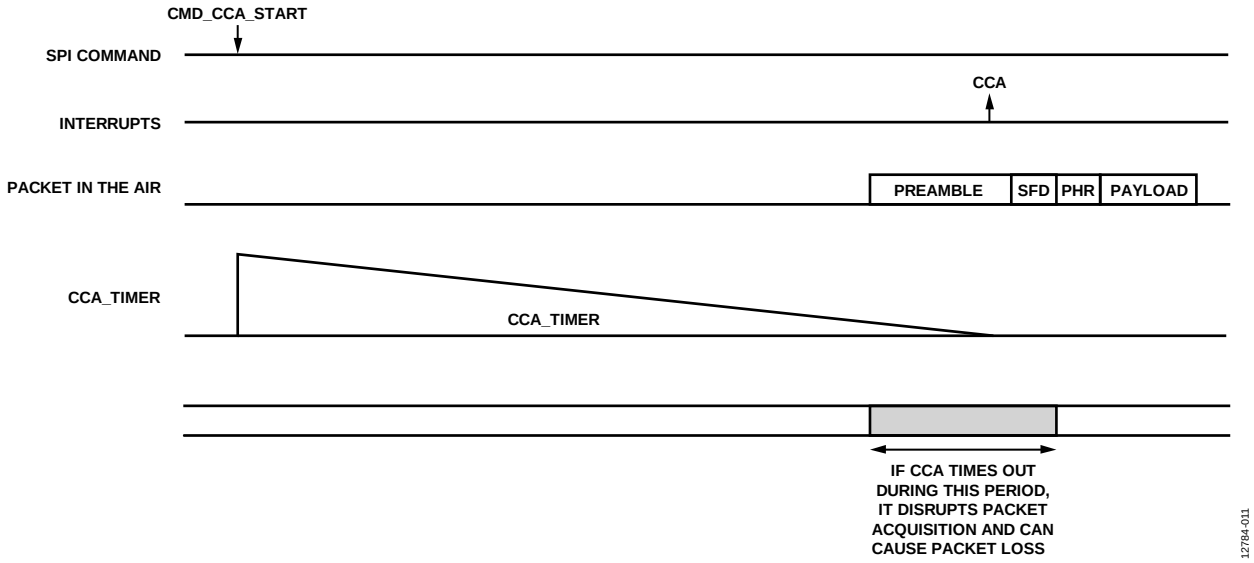

Figure 11. CCA Timer Timeout During Packet Reception

Issuing Commands During Packet Reception

Take care when issuing the CMD_CCA_START command because there are certain conditions under which issuing the command, coincident with the start of preamble on an incoming packet, causes that packet to be lost. Minimizing this risk is discussed in the Potential Packet Loss When Issuing Commands section.

Dynamic IF Filter Bandwidth Setting During CCA Timer Mode

The functionality of the intermediate frequency (IF) filter bandwidth for Rx during CCA timer mode is discussed in this section.

Upon entering the PHY_RX_CCA_15d4 state, the receiver baseband filter bandwidth is selected from the BBRAM (Bits[7:6] of Address 0x115).

In CCA timer mode, the receiver baseband filter can be automatically changed for CCA RSSI by setting the ENABLE_IFBW_AUTO_SWITCH bit (Bit 5 of the CCA_CFG_1 register, Address 0x104) to 1. Then, the filter bandwidth automatically switches to the CCA_FILTER_BW bit setting (Bits[6:5] of the BB_CCA_CFG_0 register, Address 0x103) when the CMD_CCA_START command (Command 0xB7) is issued.

Note that the IF of the receiver can toggle between 200 kHz and 300 kHz depending on the selected filter bandwidth.

The IF filter bandwidth of the receiver is switched back to its original BBRAM setting (Bits[7:6] of Address 0x115) on the occurrence of one of the following events:

- If the CCA timer times out
- Upon issuing the CMD_CCA_STOP command
- Upon issuing the CMD_PHY_RX_CCA_15d4 command
- Upon an incoming packet preamble detection if the ENABLE_IFBW_SWITCH_ON_PREAMBLE bit = 1

Upon an incoming packet preamble detection, if the ENABLE_IFBW_SWITCH_ON_PREAMBLE bit = 1, the receiver baseband filter switches back to its original value for packet reception (see Figure 12).

Upon an incoming packet preamble detection, if the ENABLE_IFBW_SWITCH_ON_PREAMBLE bit = 0, the receiver baseband filter bandwidth is retained at its current value for the duration of the packet reception, and switches back at the end of packet reception.

False Preamble Detection During CCA Timer Mode

If a false preamble is detected while in CCA timer mode and the ENABLE_IFBW_SWITCH_ON_PREAMBLE bit = 1, the receiver switches back to its original value for packet reception (as specified in the IFBW bits (Bits[7:6] of Address 0x115)).

If SFD is subsequently not detected, this is a false preamble detection, and the firmware takes the following action:

- If the ENABLE_IFBW_AUTO_SWITCH bit = 1, the ADF7023-J sets the IF filter bandwidth to the CCA_FILTER_BW bit setting (Bits[6:5] of the BB_CCA_CFG_0 register, Address 0x103) as soon as SFD is not detected.
- If the ENABLE_IFBW_AUTO_SWITCH bit = 0, the ADF7023-J sets the IF filter bandwidth to the original IFBW bit setting for packet reception, as specified in the IFBW bits (Bits[7:6] of Address 0x115) as soon as SFD is not detected.

If a false preamble is detected while in CCA timer mode, and the ENABLE_IFBW_SWITCH_ON_PREAMBLE bit = 0, the receiver does not switch back during preamble.

If SFD is subsequently not detected, this is a false preamble detection, and the firmware takes the following action:

- If the ENABLE_IFBW_AUTO_SWITCH bit = 1, the ADF7023-J sets the IF filter bandwidth to the CCA_FILTER_BW bit setting (Bits[6:5] of Address 0x103) as soon as SFD is not detected.
- If the ENABLE_IFBW_AUTO_SWITCH bit = 0, the ADF7023-J sets the IF filter bandwidth to the original IFBW value for packet reception, as specified in the IFBW bit (Bits[7:6] of Address 0x115) as soon as SFD is not detected.

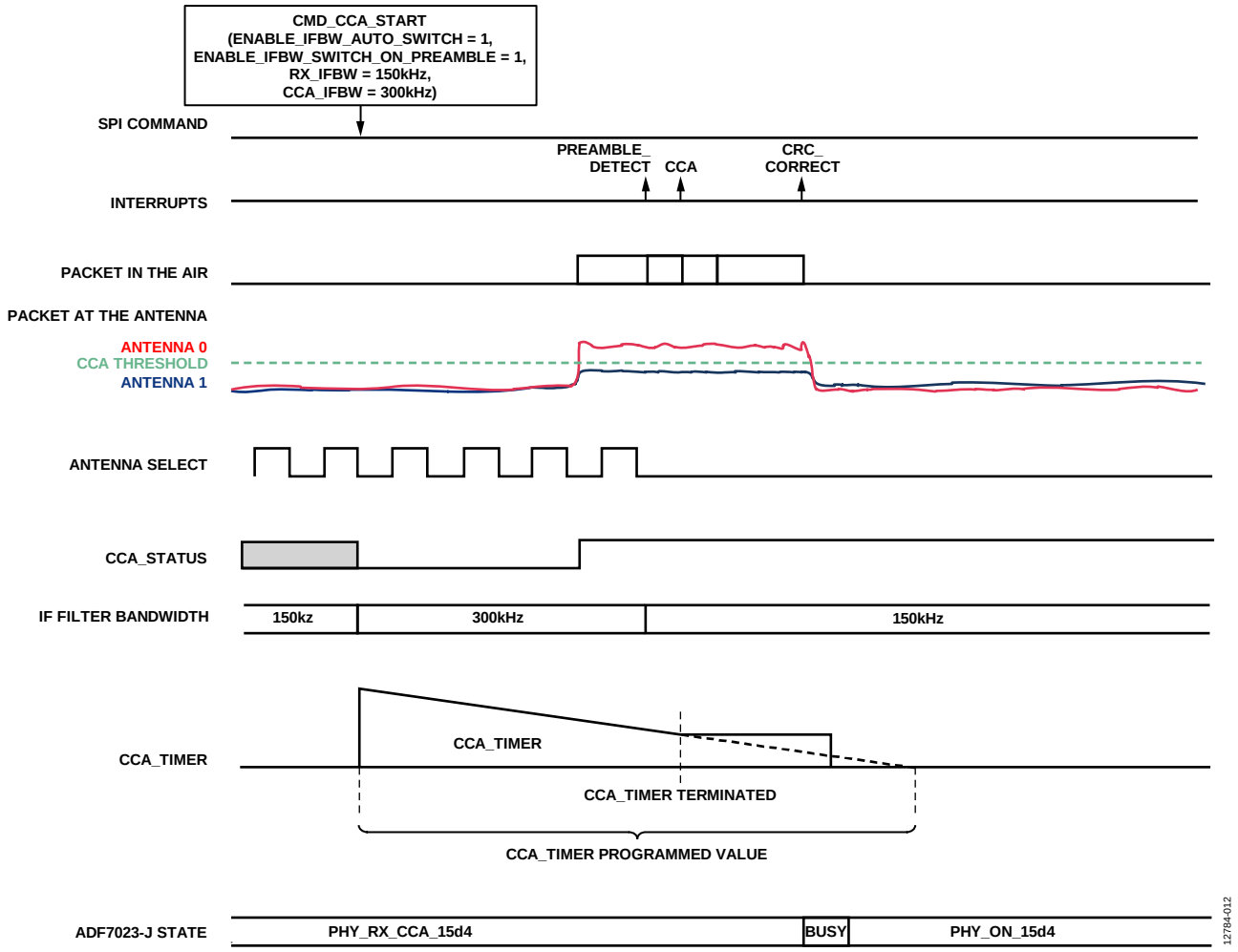

Figure 12. IF Bandwidth Automatic Switching

CCA INFINITY MODE

CCA infinity mode is used with manual Tx (the BB_CCA_CFG_0 register, Bit 4 = 1).

Setting CCA_TIMER to 7 (binary code 111), initiates infinity mode. To select a wider IF filter for CCA during infinity mode, the CMD_CCA_FILTER command must be issued before setting CCA_TIMER to 7. Therefore, when transitioning from the PHY_ON_15d4 state, set the timer value to a value other than infinity. Upon entering Rx, the CMD_CCA_FILTER command can be issued, followed by setting the timer value to infinity. The operation of the IF bandwidth switching for infinity mode is discussed in the Dynamic IF Filter Bandwidth Setting During CCA Infinity Mode section.

As soon as infinity mode is initiated, the ADF7023-J continues to evaluate the channel until the channel is clear (see Figure 13 and Figure 14).

In infinity mode, the ADF7023-J only generates a CCA interrupt when the channel is clear for a minimum of 128 µs. If the channel is clear, the device generates an INTERRUPT_CCA interrupt, stays in the PHY_RX_CCA_15d4 state, and reverts the IF filter back to its default value while still evaluating CCA RSSI and updating the CCA_LIVE_STATUS flag.

Note that if the channel remains clear, and the CCA interrupt is cleared, it is reasserted after another 128 µs evaluation period. To avoid reasserting the channels, the CCA interrupt can be masked, or infinity mode can be exited, by setting CCA_TIMER to a value other than 7 before clearing the interrupt.

Infinity mode is used with manual Tx, so automatic Tx must be disabled for infinity mode.

If infinity mode is used with antenna diversity enabled, both antennas must be clear before the channel is considered clear and the interrupt is generated. In this case, the CCA time increases to a minimum of 250 µs (see Figure 15).

During CCA infinity mode, any incoming packet can be received. If continuous Rx is enabled, the device returns to the PHY_RX_CCA_15d4 state with infinity mode still enabled. However, if the ENABLE_IFBW_SWITCH_ON_PREAMBLE bit is enabled (1), the CCA filter bandwidth reverts to its default Rx value on preamble detection. If continuous Rx is enabled, the filter bandwidth is reverted to the CCA filter bandwidth by reissuing the CMD_CCA_FILTER command.

If continuous Rx is not enabled, the device returns to the PHY_ON_15d4 state upon packet reception.

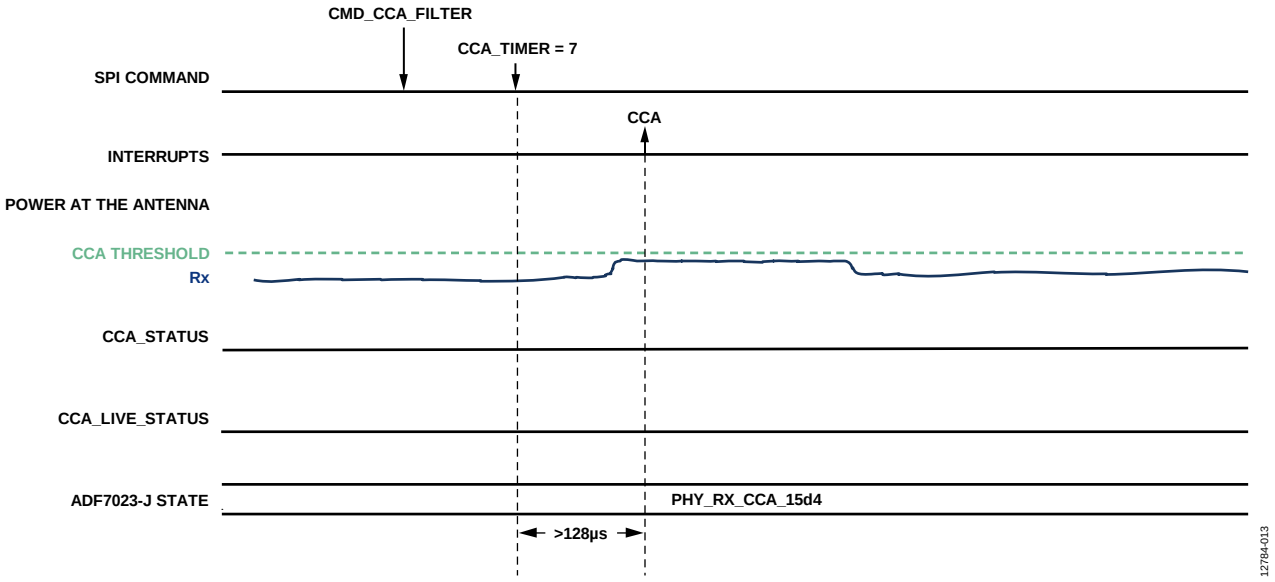

Figure 13. CCA Infinity Mode, Channel Clear on Entering

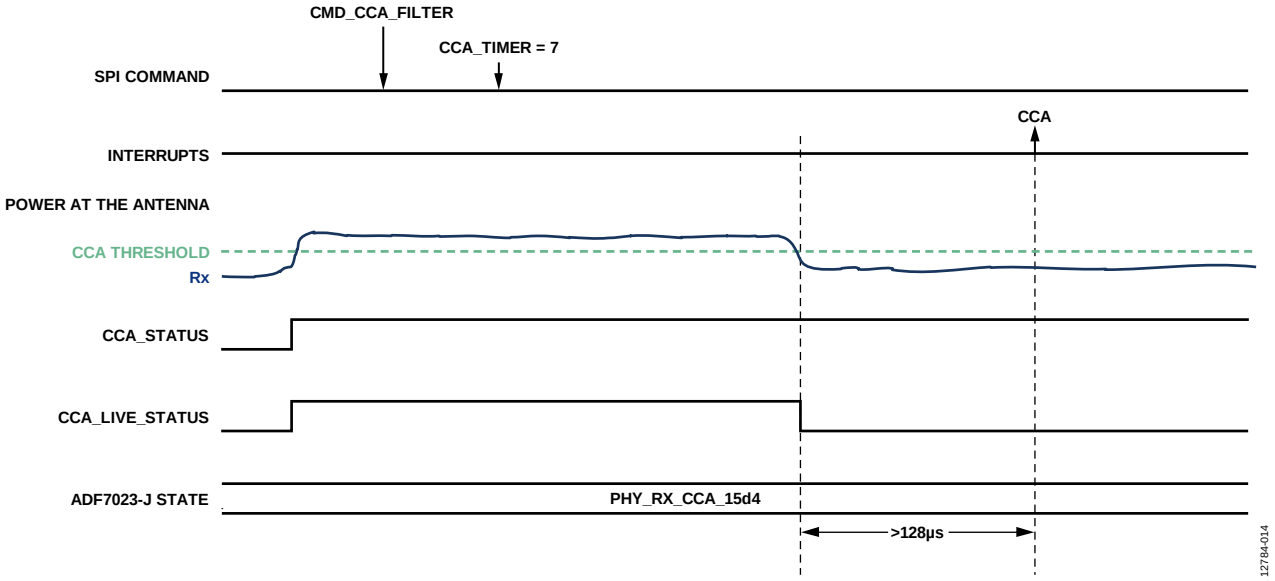

Figure 14. CCA Infinity Mode, Channel Becomes Clear

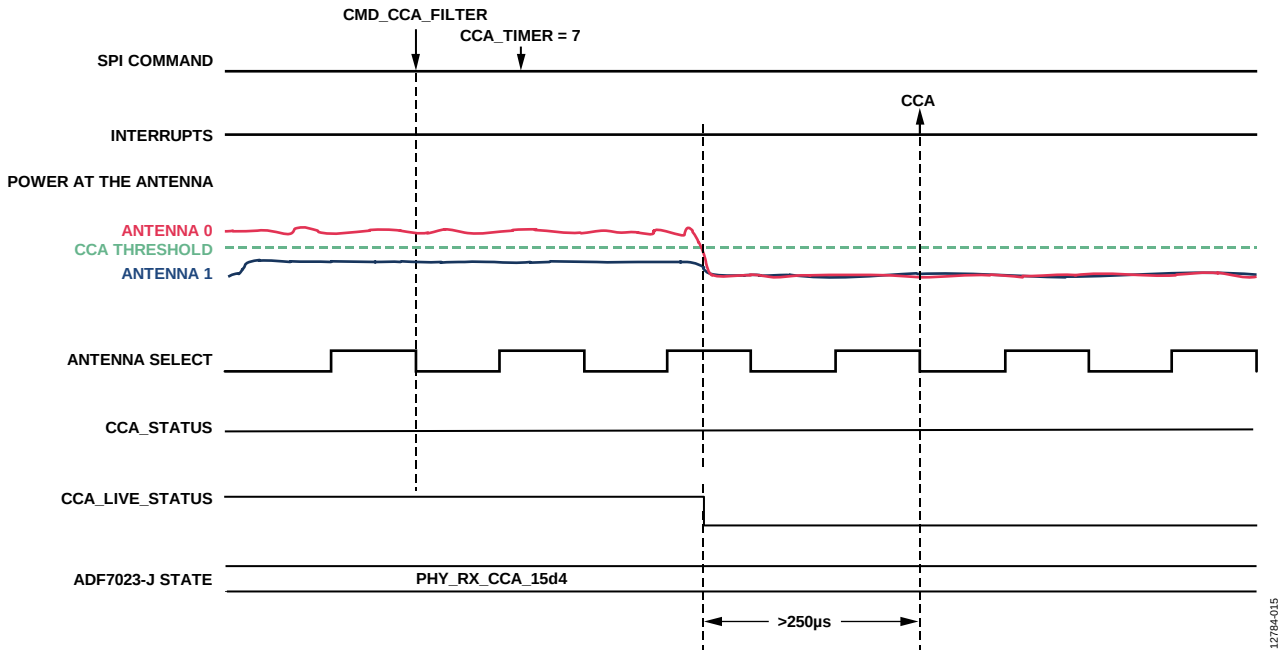

Figure 15. CCA Infinity Mode with Antenna Diversity

Dynamic IF Filter Bandwidth Setting During CCA Infinity Mode

Upon entering the PHY_RX_CCA_15d4 state, the receiver baseband filter bandwidth is selected from the BBRAM (Bits[7:6] of Address 0x115).

Setting CCA_TIMER to 7 (binary code 111), initiates infinity mode. To select a wider IF filter for CCA during infinity mode, the CMD_CCA_FILTER command (Command 0xB9) must be issued before setting CCA_TIMER to 7.

After the user issues the CMD_CCA_FILTER command (Command 0xB9), the bandwidth is automatically adjusted to the desired setting in Bits[6:5] of BBRAM Address 0x103 and Rx is restarted to allow synchronization of the antenna search period with the new setting (Figure 16).

Take care when issuing the CMD_CCA_FILTER command because there are certain conditions under which issuing the command, coincident with the start of preamble on an incoming packet, causes that packet to be lost. To minimize this risk, see the Potential Packet Loss When Issuing Commands section for more information.

Note that the IF of the receiver can toggle between 200 kHz and 300 kHz depending on selected filter bandwidth.

The IF filter bandwidth of the receiver is reverted back to its original BBRAM setting (Bits[7:6] Address 0x115) under of the following conditions:

- Upon issuing the CMD_CCA_STOP command (Command 0xB8)
- Upon issuing the CMD_PHY_RX_CCA_15d4 command (Command 0xB2)
- Upon an incoming packet preamble detection if the ENABLE_IFBW_SWITCH_ON_PREAMBLE bit = 1

Upon an incoming packet preamble detection, if the ENABLE_IFBW_SWITCH_ON_PREAMBLE bit = 1, the receiver baseband filter switches back to its original value for Rx.

If the ENABLE_IFBW_SWITCH_ON_PREAMBLE bit = 0 , the receiver baseband filter bandwidth is retained at its current CCA value for the duration of the packet reception.

False Preamble Detection During CCA Infinity Mode

Note that a false preamble detection reverts the filter back to its default Rx value. By enabling the preamble detect interrupt, this condition can be alerted to the user. The filter returns to the desired CCA filter value by reissuing the CMD_CCA_FILTER command.

Alternatively, Bit 0 in the PHY_RX_STATUS register (Address 0x01F) can be monitored to alert when a preamble has been detected and revert the filter to its previous CCA value if no SFD interrupt is received.

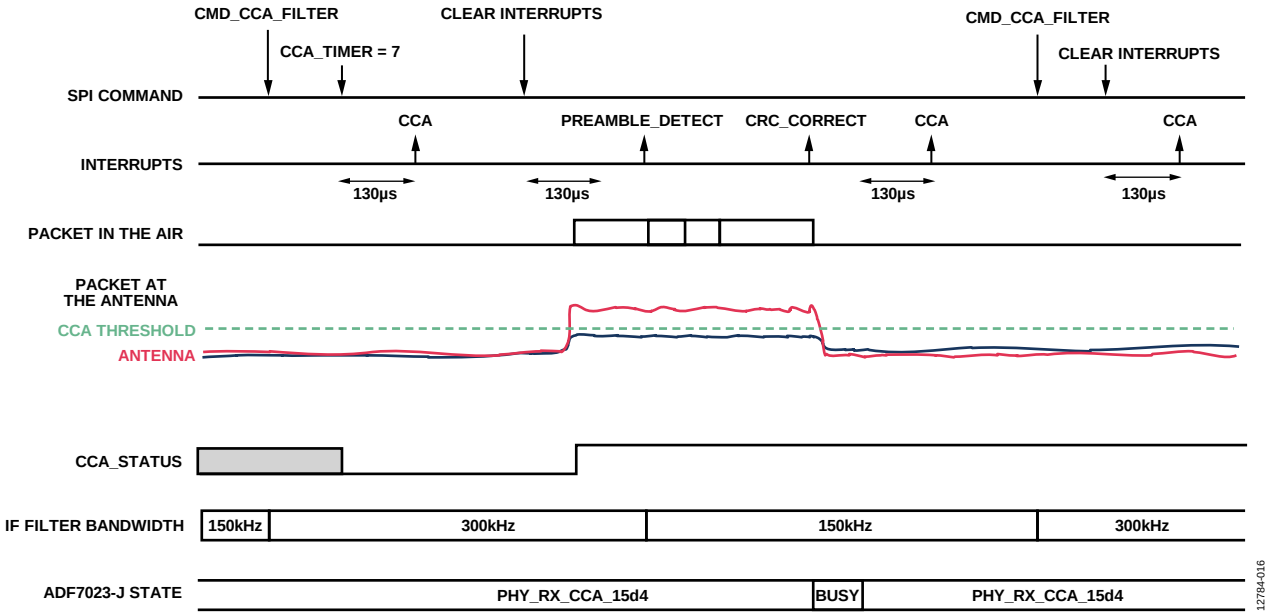

Figure 16. Dynamic CCA Filter Bandwidth with Rx, and CCA Infinity Mode

COMMAND ACCESS DURING THE PHY_RX_CCA_15d4 STATE

The ADF7023-J is controlled through commands, and command access is described in the ADF7023-J data sheet. The ADF7023-J data sheet also describes the use of the status word to ensure the communications processor is ready to accept a new command.

POTENTIAL PACKET LOSS WHEN ISSUING COMMANDS

Take care when issuing commands in the PHY_RX_CCA_15d4 state while waiting for an incoming packet because of the asynchronous timing of the incoming packets.

There are certain conditions under which issuing a command, coincident with the start of preamble on an incoming packet, causes that packet to be lost. Commands involved are the following:

- CMD_PHY_RX_CCA_15d4
- CMD_PHY_TX_15d4
- CMD_PHY_ON_15d4
- CMD_CCA_START
- CMD_CCA_FILTER

To minimize this risk of losing an incoming packet, a PHY_RX_STATUS byte (Address 0x01F) is offered (see Figure 17). Bit 0 of this byte highlights when a preamble is detected, and Bit 1 indicates when the SFD is detected.

Upon entering the PHY_RX_CCA_15d4 state, Bit 0 and Bit 1 of the PHY_RX_STATUS register (Address 0x01F), are set to 0. Upon preamble detection, Bit 0 is set to 1. Upon SFD detection, Bit 1 is set to 1. At the end of packet reception, both bits are set back to 0 (see Figure 18). If a false preamble is detected (for example, a qualified preamble without a subsequent SFD), these bits are set to 0 and the search for a preamble continues.

Any commands that restart Rx reset these bits to 0.

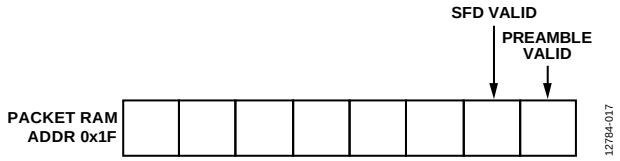

Figure 17. PHY_RX_STATUS Register

Packet loss can be minimized by monitoring the PHY_RX_STATUS register and issuing commands only when the PHY_RX_STATUS register = 0.

However, monitoring the PHY_RX_STATUS register method, there is still a condition under which packet loss is possible where a preamble may have started in the air, but is not yet detected by the device.

The two extremes of this condition are outlined in Figure 19 and Figure 20. The worst case scenario occurs at the latest possible preamble qualification time during antenna diversity, which is 8 bytes into the 10-byte preamble (see Figure 19). In this scenario, if a command (for example, the CMD_CCA_START command) occurs during the first eight bytes of preamble, it disrupts the preamble acquisition and may cause packet loss. The best case scenario occurs at the earliest possible preamble qualification time, which is three bytes into preamble (see Figure 20). In this case, if the CMD_CCA_START command occurs during the first three bytes of preamble, there may be packet loss.

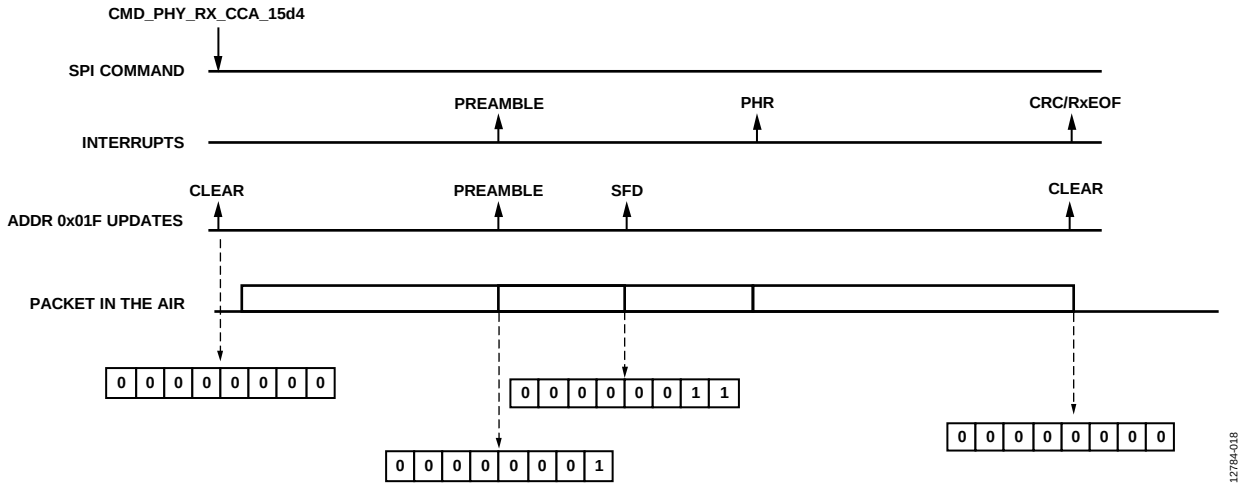

Figure 18. PHY_RX_STATUS Register Update on Packet Receptiona2b392tC Attached Bottom Box 282 0 36.002349 0 7 21 070

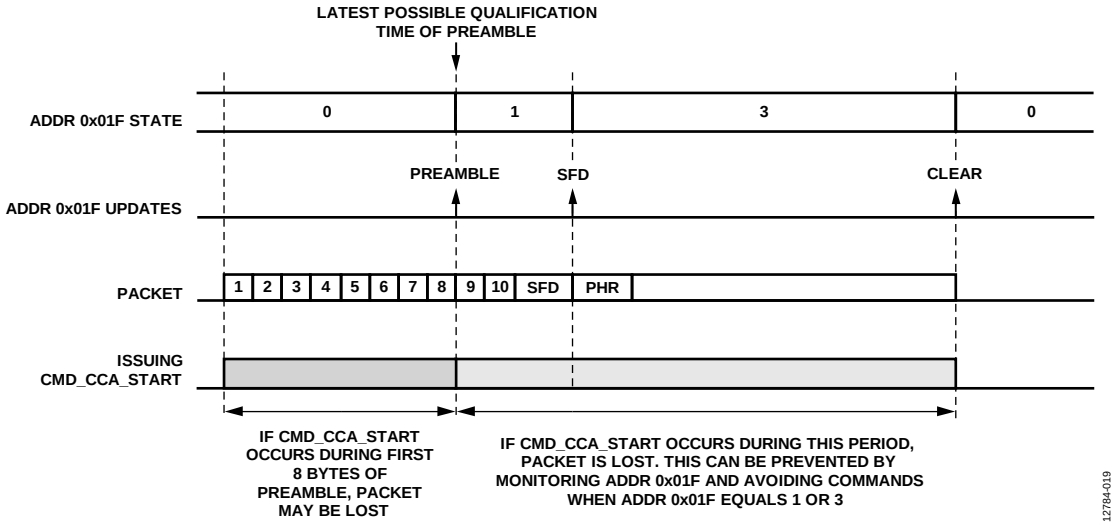

Figure 19. Packet Loss Due to Issuing the CMD_CCA_START Command During Preamble (Worst Case)

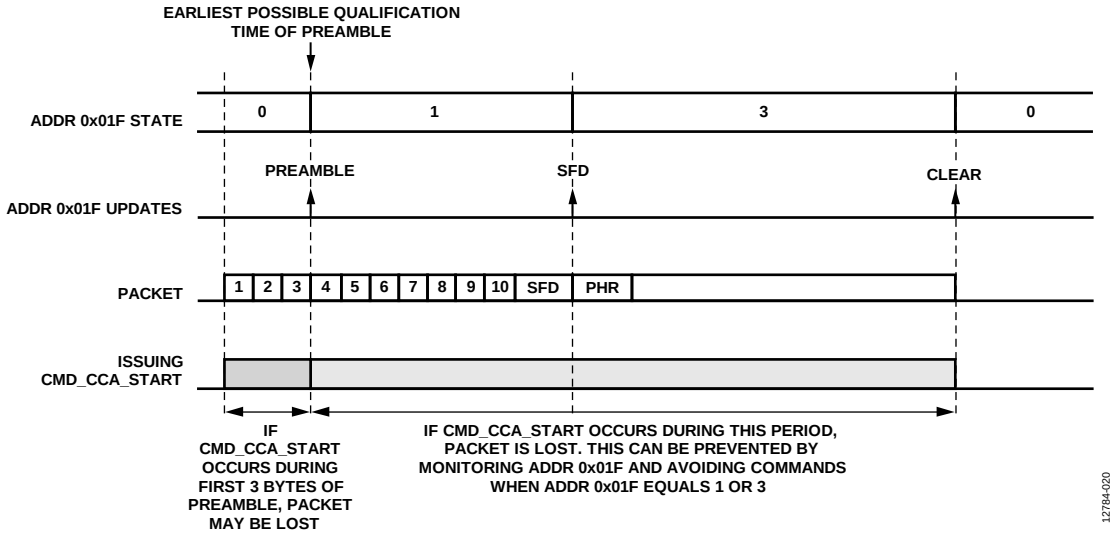

Figure 20. Packet Loss Due to Issuing the CMD_CCA_START Command During Preamble (Best Case)

PACKET STRUCTURE IN 15d4 MODE

PREAMBLE	SFD	PHR					PSDU		
4 BYTES TO 1024 BYTES PREAMBLE	0110 1111 0100 1110	MODE SWITCH	RESERVED	FCS	WHITENING	LENGTH	MAC HEADER	MAC PAYLOAD	FCS
		0	00	1	0	00000010000	NOT WHITENED	NOT WHITENED	NOT WHITENED AND 16-BIT

12784-021

Figure 21. PPDU Format Example

The ADF7023-J AD_15d4g firmware download module supports the MR_FSK PPDU header format without mode switching.

The packet structure is displayed in Figure 21.

In transmit mode, the ADF7023-J firmware download module adds the requested number of preamble bytes, and then inserts the requested SFD and PHR. If whitening is enabled, the PSDU is whitened. If a 16-bit FCS is enabled, the 16-bit CRC is automatically calculated and appended to the transmit payload.

In receive mode, the preamble optionally generates a preamble detect interrupt, and is not stored to the packet RAM. The SFD is used for byte level synchronization, optionally generates an interrupt synchronous with PHR reception, and is not stored to the packet RAM. PHR is received next, and, depending on its contents, dictates the receive packet length, whether dewhitening is to be applied or not, and whether or not FCS bytes are validated (the 16-bit FCS case is handled). Dewhitening is required in Rx if whitening is applied in Tx.

PREAMBLE

Preamble is a 1010 sequence added to the start of the packet during transmission, and removed after receiving the packet. Preamble length is defined in bytes, with a programmable range of 4 bytes to 1000 bytes. It is configured by writing to the BB_NB_PREAMBLE_BYTES_HIGH register (Address 0x12F) and the BB_NB_PREAMBLE_BYTES_LOW register (Address 0x12E).

SFD

SFD is a 2-byte word that is controlled by writing to the BB_SFD_HIGH register (Address 0x131) and the BB_SFD_LOW register (Address 0x130). The SFD takes on one of four valid options selected from Table 34. Note that the SFD is transmitted starting from Bit 0.

Table 34. SFD Values

phyMRFSKSFD	SFD Value for Coded PHR and PSDU (Bit 0 to Bit 15)	SFD Value for Uncoded PHR and PSDU (Bit 0 to Bit 15)
0	0110 1111 0100 1110	1001 0000 0100 1110
1	0110 0011 0010 1101	0111 1010 0000 1110

PHR

PHR is a 2-byte word, as defined in the PHR section in Figure 21. This word is controlled by writing the low byte to the TX_BASE_ADR register, and the high byte to the address value, TX_BASE_ADR + 1, because these form the first two bytes of the transmit packet. After issuing the CMD_PHY_TX_15d4 command, the contents of these two bytes are copied into the BB_PHR_LOW (Address 0x132) and BB_PHR_HIGH (Address 0x133) registers, respectively. Likewise, upon successful packet reception, the packet header bytes are copied into the BB_PHR_LOW register and the BB_PHR_HIGH register.

The following sections detail the PHR bit definitions: mode switch, reserved, FCS, whitening, and length.

Mode Switch

Bit 7 of the BB_PHR_LOW register is the MODE_SWITCH bit. The MODE_SWITCH bit is set to 0, indicating there is no data rate or modulation scheme change during the packet transmission. If the ADF7023-J receives a packet with mode switch the MODE_SWITCH bit set to 1, it does not generate a PHR interrupt, but does generate an INTERRUPT_CRC_CORRECT interrupt and INTERRUPT_RX_EOF interrupt (if they are enabled).

Reserved

The BB_PHR_LOW register, Bits[6:5], are reserved. The reserved bits are set to 0 for the ADF7023-J firmware for transmit mode, and are ignored by the ADF7023-J firmware download module in receive mode.

FCS

Bit 4 of the BB_PHR_LOW register is the FCS bit.

FCS = 0 indicates a 32-bit FCS. This case is not handled automatically by the ADF7023-J firmware download module. For transmit, the user must calculate the 32-bit CRC and add it to the PSDU. In receive mode, the 32-bit CRC is received as part of the PSDU and stored in the packet RAM, CRC is not validated, and the CRC interrupt is not asserted. The INTERRUPT_RX_EOF interrupt indicates when the packet is received.

FCS = 1 indicates a 16-bit CRC. This case is handled automatically by the firmware. In transmit mode, the 16-bit CRC is calculated and appended to the transmit PSDU. In receive mode, the 16-bit CRC is calculated from the incoming payload and, if the CRC is correct, the CRC interrupt is asserted (if enabled).

Whitening

Bit 3 of the BB_PHR_LOW register is the whitening bit. If the whitening bit = 0, the PSDU is not whitened, and if the whitening bit = 1, the PSDU is whitened on transmission. Only the PSDU is whitened, not the SFD or PHR.

In receive mode, if the whitening bit is set to 1 in the received packet header, the ADF7023-J firmware download module automatically dewhitens the received PSDU.

Length

Bits[2:0] of the BB_PHR_LOW register define Bits[10:8] of the PSDU_LENGTH[10:0] word, and Bits[7:0] of the BB_PHR_HIGH register define Bits[7:0] of the PSDU_LENGTH[10:0] word.

The PSDU_LENGTH[10:0] word can be set to values in the range of 3 to 2047.

Tx/Rx ROLLING DATA BUFFER

In packet mode, when the ADF7023-J receives a packet, the data is stored in a linear sequence in the packet RAM. Prior to transmission, the data to be transmitted is written to the packet RAM in a linear sequence. This functionality is described in the ADF7023-J data sheet.

If the AD_15d4g firmware download module is used, it is possible to receive or transmit packets that are longer than the available packet RAM, which is accomplished via a rolling buffer. The registers applicable to the operation of the rolling buffer are given in Table 35.

Packet RAM locations 0x20 to 0xFF are available for packet data. Bytes 0x00 to 0x1F are allocated for use by the on-chip processor and must not be used for packet data.

Table 35. Registers for Use with Tx/Rx Rolling Data Buffer

Address (Hex)	Register	Description
0x124	TX_BASE_ADR	Start location in packet RAM of Tx buffer
0x125	RX_BASE_ADR	Start location in packet RAM of Rx buffer
0x134	BB_RX_BUFFER_SIGNAL	Rx buffer nearly full
0x135	BB_RX_BUFFER_SIZE	Rx buffer full
0x136	BB_TX_BUFFER_SIGNAL	Tx buffer nearly full
0x137	BB_TX_BUFFER_SIZE	Tx buffer full

ROLLING BUFFER IN TRANSMIT MODE

In transmit mode, the TX_BASE_ADR register sets the start of the rolling buffer in packet RAM. The BB_TX_BUFFER_SIZE register sets the size of the buffer. Do not allow the buffer size to exceed the available packet RAM. When the value in the BB_TX_BUFFER_SIZE register is added to the value in the TX_BASE_ADR register, do not exceed Address 0x0FF.

Set the value in the BB_TX_BUFFER_SIGNAL register so that an INTERRUPT_BUFFER_ALMOST_FULL interrupt is generated prior to transmission of all the data in the buffer. Typically, the BB_TX_BUFFER_SIGNAL register is set so the interrupt is asserted when half of the data in the buffer has been transmitted.

When an INTERRUPT_BUFFER_ALMOST_FULL interrupt is asserted, the host microprocessor writes new data to the locations from address value TX_BASE_ADR to address value, TX_BASE_ADR + BB_TX_BUFFER_SIGNAL.

When the data in the last byte of the Tx buffer has been transmitted, the ADF7023-J continues transmitting, starting with the data at the address value TX_BASE_ADR. If enabled, an INTERRUPT_BUFFER_FULL interrupt is asserted when the last byte in the buffer is transmitted.

When an INTERRUPT_BUFFER_FULL interrupt is asserted, the host microprocessor writes new data to the locations from address value, TX_BASE_ADR + BB_TX_BUFFER_SIGNAL + 1, to address value, TX_BASE_ADDRESS + BB_TX_BUFFER_SIZE.

Transmission of data continues until PSDU_LENGTH[10:0] bytes are sent, the INTERRUPT_TX_EOF interrupt goes high if enabled, or the user issues the CMD_PHY_ON_15d4 command.

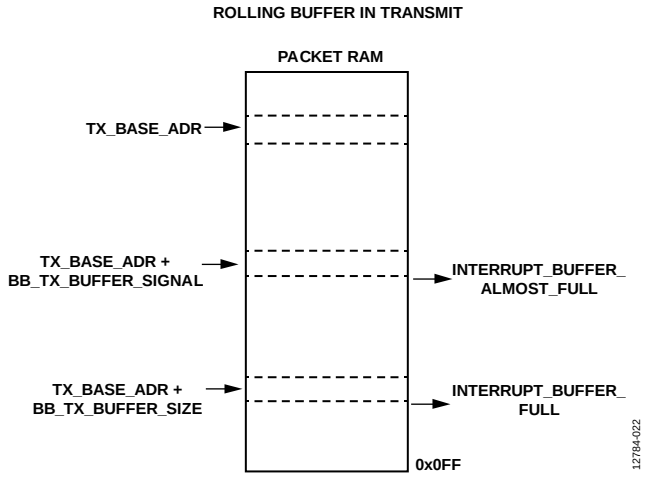

Figure 22. Rolling Buffer in Transmit Mode

ROLLING BUFFER IN RECEIVE MODE

In receive mode, the RX_BASE_ADDRESS register sets the start of the rolling buffer in packet RAM. The BB_RX_BUFFER_SIZE register sets the size of the buffer. Do not allow the buffer size to exceed the available packet RAM. When the value in the BB_RX_BUFFER_SIZE register is added to the value in the RX_BASE_ADR register, do not exceed 0x0FF. If the 16-bit FCS checking on the ADF7023-J is enabled, 0x0FD is not exceeded.

Set the value in the BB_RX_BUFFER_SIGNAL register so that an INTERRUPT_BUFFER_ALMOST_FULL interrupt is asserted prior to the buffer being filled by received data. Typically, the BB_RX_BUFFER_SIGNAL register is set so the interrupt is asserted when half the buffer has been filled with received data.

When an INTERRUPT_BUFFER_ALMOST_FULL interrupt is asserted, the host microprocessor reads in the data in the locations from address value RX_BASE_ADDRESS to address value, RX_BASE_ADR + BB_RX_BUFFER_SIGNAL.

When the last byte of the Rx buffer has been filled, the ADF7023-J continues writing the received data starting at the RX_BASE_ADR register. If enabled, an INTERRUPT_BUFFER_FULL interrupt is asserted when the buffer has been filled.

When an INTERRUPT_BUFFER_FULL interrupt is asserted, the host microprocessor reads in the data in the locations from address value, RX_BASE_ADDRESS + BB_RX_BUFFER_SIGNAL + 1, to address value, RX_BASE_ADDRESS + BB_RX_BUFFER_SIZE.

Reception of data continues until the number of bytes defined in the PSDU_LENGTH[10:0] word has been received and INTERRUPT_RX_EOF and/or INTERRUPT_CRC_CORRECT are asserted (if enabled), or the host microprocessor issues the CMD_PHY_ON_15d4 command.

Note that if a 16-bit CRC is enabled (16-bit FCS), the FCS bytes are placed into the packet RAM as two bytes after the payload, outside of the rolling buffer control. What this means is that if the payload fills up to address value, RX_BASE_ADDRESS + BB_RX_BUFFER_SIZE, when the 16-bit FCS is calculated and checked vs. the incoming FCS, the received FCS bytes are placed in the next two memory locations (beyond the address value, RX_BASE_ADDRESS + BB_RX_BUFFER_SIZE). If another buffer is defined to start in the memory location immediately following an address value, RX_BASE_ADDRESS + BB_RX_BUFFER_SIZE, in this instance the first two bytes are overwritten.

To avoid this situation arising for any length and buffer size, leave an overflow area of two bytes vacant immediately after the Rx buffer. If the Rx buffer is assigned to the upper part of the packet memory, set it to not exceed memory location 0xFD.

If the Rx buffer is placed lower down in packet memory, and is immediately followed in packet memory by a Tx buffer, set the TX_BASE_ADR register to be three bytes greater than address value, RX_BASE_ADDRESS + BB_RX_BUFFER_SIZE. This procedure ensures that if the payload length places the packet end at the BB_RX_BUFFER_SIZE boundary, the overflow of the FCS bytes does not cause overwriting of the first two bytes of the following Tx buffer. The FCS bytes are written into the overflow bytes, instead.

This overwriting issue does not arise in 32-bit CRC mode. In 32-bit CRC mode, the ADF7023-J does not calculate the CRC itself, so the incoming four bytes of FCS are considered the same as the payload, and are loaded into the receive buffer under rolling buffer control.

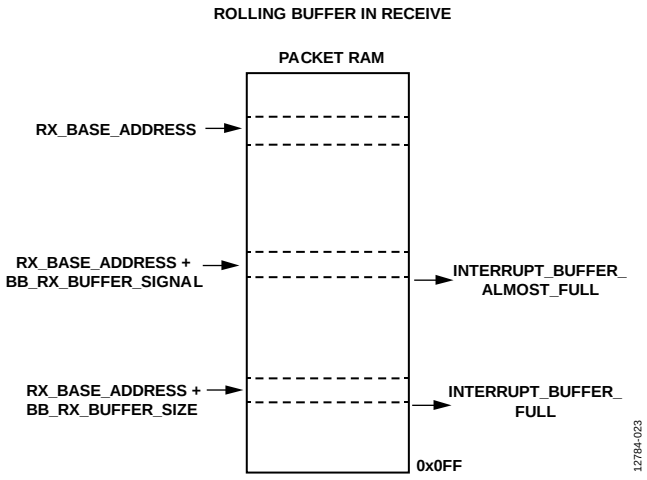

Figure 23. Rolling Buffer in Receive Mode

RECOMMENDED REGISTER SETTINGS

RECOMMENDED AUTOMATIC GAIN CONTROL (AGC) SETTINGS

To optimize the receiver for robust PER performance over the full input power range, overwrite the default AGC clock divide setting in the modem configuration random access memory (MCR). It is recommended to set the AGC_CLOCK_DIVIDE register (Address 0x32F) to 0x12.

Tx LOOKUP TABLE (LUT) SETTINGS

The optimized phase-locked loop (PLL) bandwidth settings for T108 operation are built into the AD_15d4g firmware download. Therefore, it is unnecessary to write a custom transmit LUT. Set Bits[5:4] of the RADIO_CFG_7 register (Address 0x113) to 0 when using the PHY_TX_15d4 state.

REUSED BBRAM SETTINGS

The ADF7023-J AD_15d4g firmware download reuses the BBRAM registers, and, thus, some default functions are no longer available when in 15d4 mode (see Table 1).

Smart wake mode is not available with the AD_15d4g firmware download because BBRAM Address 0x103, Address 0x104, and Address 0x105 are reused for CCA functionality in the firmware download.

Address matching and static register fix are not available with the AD_15d4g download because BBRAM Address 0x129 to Address 0x137 are reused by the firmware to control the antenna diversity and packet structure.

Transmit test modes are not available within the PHY_TX_15d4 state. To use the transmit test modes, it is necessary to revert to the PHY_ON state to get to the PHY_TX state.

To use the optimized PLL settings for T108 operation in PHY_TX state, the sequence outlined in the ADF7023-J data sheet must be followed.

Therefore, the full sequence from the PHY_ON_15d4 state to transmit test mode with optimized T108 PLL settings is as follows:

1. Issue Command 0xB1 to exit 15d4 mode.
2. Use the custom transmit LUT. Write 0x2 to Bits[5:4] of the RADIO_CFG_7 register (Address 0x113).
3. Issue the CMD_CONFIG_DEV command.
4. Write the custom LUT, as defined in Table 36.
5. Select the transmit test mode desired (see the test modes information in the ADF7023-J data sheet).
6. Enter the PHY_TX state.

Table 36. T108 Custom Transmit LUT

Register	Data Rate = 50 kbps or 100 kbps (Closed Loop Bandwidth (CLBW) = 130 kHz)	Data Rate = 200 kbps (CLBW = 223 kHz)
0x010	0x10	0x20
0x011	0x10	0x20
0x012	0x0F	0x0F
0x013	0x0F	0x0F
0x014	0x1F	0x1F
0x015	0x0F	0x05
0x016	0x1F	0x1F
0x017	0x33	0x33
0x018	0x22	0x22

EXAMPLE RECEIVER SETTINGS FOR 100 kbps AND 200 kbps OPERATION, AUTOMATIC FREQUENCY CONTROL (AFC) ENABLED

Table 37. Example Rx Settings, AFC Enabled

Parameter	100 kbps, f_{DEV} = 50 kHz	200 kbps, f_{DEV} = 100 kHz
Data Rate	0x3E8	0x7D0
Deviation	0x1F4	0x3E8
IF Filter Bandwidth (BW)	150 kHz	200 kHz
Discriminator Bandwidth	0x20	0x10
Post Demodulated Bandwidth	0x26	0x4B
AGC Thresholds	Default	Default
AGC Clock Divide	0x12	0x12

SPECIFICATIONS

All specifications are for 100 kbps, 50 kHz deviation only unless otherwise indicated.

Table 38. Application to the IEEE 802.15.4g Standard

Parameter	Typical Specification	Test Conditions/Comments
PPDU FORMAT		
Preamble	4 bytes to 1000 bytes	
SFD	2 bytes	
PHR	2 bytes	
PSDU	3 bytes to 2047 bytes	
CRC	16-bit	$x^{16} + x^{12} + x^5 + 1$
DATA WHITENING	PN9	As defined in the IEEE 802.15.4g standard
BIT SEQUENCE	LSB first	
TURNAROUND TIME		
Rx (CCA) to Tx (Data)	216 µs	The CCA_AUTO_TX bit = 0, fast Rx/Tx transitions enabled
Rx (CCA) to Tx (Data)	270 µs	The CCA_AUTO_TX bit = 0, fast Rx/Tx transitions disabled
Rx (Data) to Tx (Acknowledge)	210 µs	The RX_TO_TX_AUTO_TURNAROUND bit enabled, fast Rx/Tx transitions enabled
Rx (Data) to Tx (Acknowledge)	350 µs	The RX_TO_TX_AUTO_TURNAROUND bit enabled, fast Rx/Tx transitions disabled
Tx (Data) to Rx	125 µs	The TX_TO_RX_AUTO_TURNAROUND bit enabled, fast Rx/Tx transitions enabled
Tx (Data) to Rx	281 µs	The TX_TO_RX_AUTO_TURNAROUND bit enabled, fast Rx/Tx transitions disabled

TEST CONDITIONS

Table 39.

Parameter	Typical Specification	Test Conditions/Comments
ANTENNA DIVERSITY		
Minimum Preamble	10 bytes	Antenna diversity enabled, 100 kbps, 50 kHz deviation, AGC on, AFC on
	20 bytes	Antenna diversity enabled, 200 kbps, 100 kHz deviation, AGC on, AFC on
Sensitivity	−103.0 dBm	Antenna diversity enabled, delta between antennas = 0 dB, 100 kbps, 50 kHz deviation, PER = 1%, AGC on, AFC on, IF BW = 150 kHz, PSDU length = 12 bytes
	−101.5 dBm	Antenna diversity enabled, delta between antenna = 20 dB, 100 kbps, 50 kHz deviation, PER = 1%, AGC on, AFC on, IF BW = 150 kHz, PSDU length = 12 bytes
Sensitivity Including IFBW Switching	−101.5 dBm	Antenna diversity enabled, CCA enabled, 200 kHz to 150 kHz, PER = 1%, delta between antennas = 20 dB, 100 kbps, 50 kHz deviation, AGC on, AFC on, IF BW = 150 kHz, PSDU length = 12 bytes
Processing Gain of Antenna Diversity	9 dB	PER = 1%, PSDU length = 12 bytes, 100 kbps, 50 kHz deviation, Rayleigh/static fading: f_D = 4 Hz pitch, correlation factor of 0, 1

CODE DOWNLOAD SEQUENCE

The AD_15d4g firmware download module must be stored in the PRAM starting from Address 0x0000.

The program RAM can be written to only by using the memory block write. Set the SPI_MEM_WR command to 0x1E.

The sequence to write a firmware module to program RAM is as follows:

1. Ensure that the ADF7023-J is in the PHY_OFF state.
2. Issue the CMD_RAM_LOAD_INIT command.
3. Write the module to PRAM using an SPI memory block write.
4. Issue the CMD_RAM_LOAD_DONE command.

The firmware module is now stored on program RAM.