

# Μοσχογιάννης Πασχάλης AM 2114026

## Άσκηση 1

```
1 //testbench for DFF
2 timescale 1ns / 1ps
3 module dff_tb;
4   reg CLK;
5   reg D;
6   wire Q;
7
8   dff DUT(
9     .CLK(CLK),
10    .D(D),
11    .Q(Q));
12
13   initial begin
14     $dumpfile("dff_tb.vcd");
15     $dumpvars;
16
17     D=0;
18     CLK=0;
19     forever #10 CLK = ~CLK;
20   end
21
22   initial begin
23     D <= 0;
24     #100; D <= 1;
25     #100; D <= 0;
26     #100; D <= 1;
27   end
28
29 endmodule
30
31
```

```
1 timescale 1ns / 1ps
2 // Verilog code for D Flip Flop
3 module dff (CLK, D, Q);
4   input CLK;
5   input D;
6   output reg Q;
7
8   always @ (posedge CLK)
9     begin
10      Q <= D;
11    end
12
13 endmodule
```

iverilog - Icarus Verilog compiler Version 10.2 (stable)  
vvp - Icarus Verilog vvp runtime engine Version 10.2 (stable)

```
$ iverilog -Wall -o dff_tb.vvp dff_tb.v dff.v
```

```
$ vvp dff_tb.vvp
```

```
$ ls
```

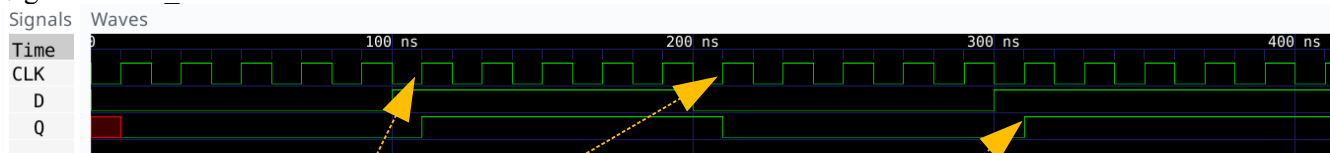
```
dff_tb.v
```

```
dff_tb.vcd
```

```
dff_tb.vvp
```

```
dff.v
```

```
$ gtkwave dff_tb.vcd
```



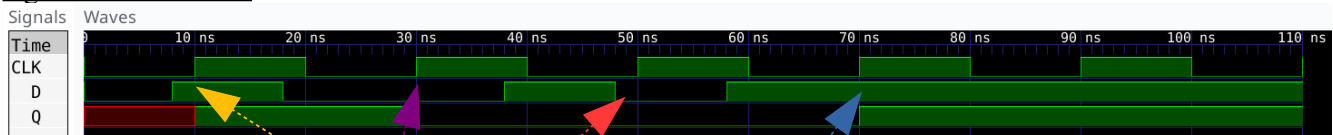
1. At rising edge of clock marked 1 - the Data D Input is 1, hence Q becomes 1 right after that.
2. At rising edge of clock marked 2, the Data is 0, hence Q becomes 0 right after the clock rising edge.
3. At 3, Data is 1 at the rising edge of clock, hence Q becomes 1

## Another testbench

```
1 //testbench for DFF
2 timescale 1ns / 1ps
3 module dff_tb;
4     reg CLK;
5     reg D;
6     wire Q;
7     dff DUT(
8         .CLK(CLK),
9         .D(D),
10        .Q(Q));
11     integer i;
12     initial begin
13         $dumpfile("dff_tb.vcd");
14         $dumpvars;
15         D=0;
16         CLK=0;
17         // forever #10 CLK = ~CLK;
18         // OR
19         for (i=0; i <=10; i=i+1)
20             #10 CLK = ~CLK;
21     end
22     initial begin
23         D <= 0;
24         #0; D <= 1;
25         #10; D <= 0;
26         #10; D <= 0;
27         #10; D <= 1;
28         #10; D <= 0;
29         #10; D <= 1;
30         #10;
31     end
32     initial begin
33         $monitor("Clock=%d,D=%d,Q=%d \n",CLK,D,Q);
34     end
35 endmodule
36
```

NORMAL dff\_tb.v  
"dff\_tb.v" 37L, 652C written

\$ gtkwave dff\_tb.vcd



1. At rising edge of clock marked 1 - the Data D Input is 1, hence Q becomes 1 right after that. It is undefined x before that.
2. At rising edge of clock marked 2, the Data is 0, hence Q becomes 0 right after the clock rising edge.
3. At 3, the Data is again 0, hence Q stays 0.
4. At 4, Data is 1 at the rising edge of clock, hence Q becomes 1

## Άσκηση 2

```
1 timescale 1ns / 1ps
2 module dff8_tb;
3   reg [7:0] d;
4   reg clock;
5   wire [7:0] q;
6
7   dff8 DUT(
8     .d(d),
9     .clock(clock),
10    .q(q));
11   integer i;
12   initial begin
13     $dumpfile("dff8_tb.vcd");
14     $dumpvars;
15     clock=1'b0;
16     // forever #10 CLK = ~CLK;
17     // OR
18     for (i=0; i <=10; i=i+1)
19       #10 clock = ~clock;
20   end
21
22   initial begin
23     d <= 8'bxxxxxxx;
24     #8; d <= 8'b11110011;
25     #10; d <= 8'b10000011;
26     #10;
27   end
28   initial begin
29     $monitor("Clock=%d,d=%d,q=%d \n",clock,d,q);
30   end
31 endmodule
32
33
```

```
$ iverilog -Wall -o dff8_tb.vvp dff8_tb.v dff8.v
```

```
$ vvp dff8_tb.vvp
```

VCD info: dumpfile dff8\_tb.vcd opened for output.

Clock=0,d= x,q= x

Clock=0,d=243,q= x

Clock=1,d=243,q=243

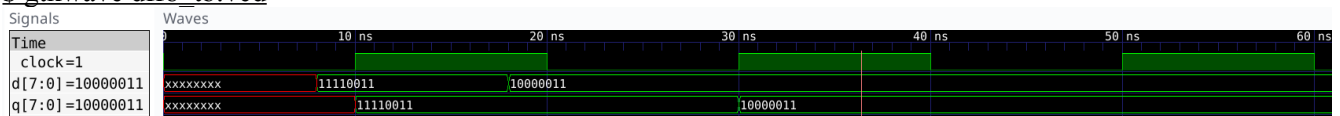
Clock=1,d=131,q=243

Clock=0,d=131,q=243

Clock=1,d=131,q=131

...

```
$ gtkwave dff8_tb.vcd
```



## Άσκηση 3

```
...laptop: ~/Μαθήματα/Οργάνωση ΗΥ/2020-2021/Οργάνωση ΗΥ (Εργαστήριο)/lab2/homework3
1 timescale 1ns / 1ps
2 module dff8 tb;
3   reg [7:0] d;
4   reg clock;
5   reg reset;
6   wire [7:0] q;
7
8   dff8 DUT(.d(d),.clock(clock),.reset(reset),
9     .q(q));
10
11   integer i;
12   initial begin
13     $dumpfile("dff8_tb.vcd");
14     $dumpvars;
15     clock=1'b0;
16     reset=0;
17     // forever #10 CLK = ~CLK;
18     // OR
19     for (i=0; i <=10; i=i+1)
20       #10 clock = ~clock;
21   end
22
23   initial begin
24     reset=0;
25     d <= 8'bxxxxxxxx;
26     #8; d <= 8'b11110011;
27     #10; reset=1;
28     d <= 8'b10000011;
29     #10;
30   end
31   initial begin
32     $monitor("Clock=%d,d=%d,q=%d \n",clock,d,q);
33   end
34 endmodule
35
```

```
...laptop: ~/Μαθήματα/Οργάνωση ΗΥ/2020-2021/Οργάνωση ΗΥ (Εργαστήριο)/lab2/homework3
1 timescale 1ns / 1ps
2 // * positive-edge triggered
3 // * synchronous active-high/low reset
4 module dff8 (
5   output reg [7:0] q,
6   input reset,
7   input clock,
8   input [7:0] d
9 );
10
11 always @ (posedge clock)
12 begin
13   if(!reset)
14     q <= 8'b00000000;
15   else
16     q <= d;
17 end
18 endmodule
19
```

NORMAL dff8\_tb.v unix | utf-8 | verilog 2% 1:1 "dff8\_tb.v" 35L, 680C

NORMAL dff8.v unix | utf-8 | verilog 5% 1:1 "dff8.v" 19L, 321C

```
$ iverilog -Wall -o dff8_tb.vvp dff8_tb.v dff8.v
```

```
$ vvp dff8_tb.vvp
```

VCD info: dumpfile dff8\_tb.vcd opened for output.

Clock=0,d= x,q= x

Clock=0,d=243,q= x

Clock=1,d=243,q= 0

Clock=1,d=131,q= 0

Clock=0,d=131,q= 0

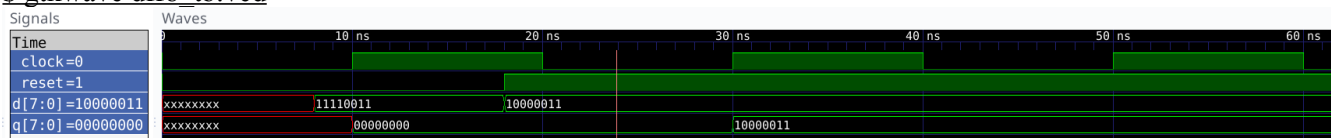
Clock=1,d=131,q=131

Clock=0,d=131,q=131

Clock=1,d=131,q=131

...

```
$ gtkwave dff8_tb.vcd
```



## Άσκηση 4

```
1 timescale 1ns / 1ps
2 module dff_AsyncReset_tb;
3     reg Clock, Reset, D;
4     wire Q;
5     dff_AsyncReset DUT(.D(D),.Clock(Clock),.Reset(Reset),
6         .Q(Q));
7     initial begin
8         $dumpfile("dff_AsyncReset_tb.vcd");
9         $dumpvars;
10        Clock=0;
11        Reset = 0;
12        D = 1'b0;
13        #1;
14        Clock=1;
15        D = 1;
16        Reset = 1;
17        #1;
18        Clock=0;
19        D = 0;
20        #1;
21        Clock=0;
22        Reset=0;
23        #1;
24        Clock=1;
25        Reset = 1;
26        #1;
27        Clock=0;
28        D = 1;
29        #1;
30        Clock=0;
31        Reset=0;
32        #1;
33        Clock=1;
34        D = 1;
35        #1;
36        Clock=0;
37        Reset=0;
38        #1;
39        Clock=1;
40        D = 1;
41        #1;
42        Clock=0;
43        Reset=0;
44        #1;
45        Clock=1;
46        D = 1;
47        #1;
48        Clock=0;
49        Reset=0;
50        #1;
51        Clock=1;
52        D = 1;
53        #1;
54        Clock=0;
55        Reset=0;
56        #1;
57        Clock=1;
58        D = 1;
59        #1;
60        Clock=0;
61        Reset=0;
62        #1;
63        Clock=1;
64        D = 1;
65        #1;
66        Clock=0;
67        Reset=0;
68        #1;
69        Clock=1;
70        D = 1;
71        #1;
72        Clock=0;
73        Reset=0;
74        #1;
75        Clock=1;
76        D = 1;
77        #1;
78        Clock=0;
79        Reset=0;
80        #1;
81        Clock=1;
82        D = 1;
83        #1;
84        Clock=0;
85        Reset=0;
86        #1;
87        Clock=1;
88        D = 1;
89        #1;
90        Clock=0;
91        Reset=0;
92        #1;
93        Clock=1;
94        D = 1;
95        #1;
96        Clock=0;
97        Reset=0;
98        #1;
99        Clock=1;
100       D = 1;
101       #1;
102       Clock=0;
103       Reset=0;
104       #1;
105       Clock=1;
106       D = 1;
107       #1;
108       Clock=0;
109       Reset=0;
110       #1;
111       Clock=1;
112       D = 1;
113       #1;
114       Clock=0;
115       Reset=0;
116       #1;
117       Clock=1;
118       D = 1;
119       #1;
120       Clock=0;
121       Reset=0;
122       #1;
123       Clock=1;
124       D = 1;
125       #1;
126       Clock=0;
127       Reset=0;
128       #1;
129       Clock=1;
130       D = 1;
131       #1;
132       Clock=0;
133       Reset=0;
134       #1;
135       Clock=1;
136       D = 1;
137       #1;
138       Clock=0;
139       Reset=0;
140       #1;
141       Clock=1;
142       D = 1;
143       #1;
144       Clock=0;
145       Reset=0;
146       #1;
147       Clock=1;
148       D = 1;
149       #1;
150       Clock=0;
151       Reset=0;
152       #1;
153       Clock=1;
154       D = 1;
155       #1;
156       Clock=0;
157       Reset=0;
158       #1;
159       Clock=1;
160       D = 1;
161       #1;
162       Clock=0;
163       Reset=0;
164       #1;
165       Clock=1;
166       D = 1;
167       #1;
168       Clock=0;
169       Reset=0;
170       #1;
171       Clock=1;
172       D = 1;
173       #1;
174       Clock=0;
175       Reset=0;
176       #1;
177       Clock=1;
178       D = 1;
179       #1;
180       Clock=0;
181       Reset=0;
182       #1;
183       Clock=1;
184       D = 1;
185       #1;
186       Clock=0;
187       Reset=0;
188       #1;
189       Clock=1;
190       D = 1;
191       #1;
192       Clock=0;
193       Reset=0;
194       #1;
195       Clock=1;
196       D = 1;
197       #1;
198       Clock=0;
199       Reset=0;
200       #1;
201       Clock=1;
202       D = 1;
203       #1;
204       Clock=0;
205       Reset=0;
206       #1;
207       Clock=1;
208       D = 1;
209       #1;
210       Clock=0;
211       Reset=0;
212       #1;
213       Clock=1;
214       D = 1;
215       #1;
216       Clock=0;
217       Reset=0;
218       #1;
219       Clock=1;
220       D = 1;
221       #1;
222       Clock=0;
223       Reset=0;
224       #1;
225       Clock=1;
226       D = 1;
227       #1;
228       Clock=0;
229       Reset=0;
230       #1;
231       Clock=1;
232       D = 1;
233       #1;
234       Clock=0;
235       Reset=0;
236       #1;
237       Clock=1;
238       D = 1;
239       #1;
240       Clock=0;
241       Reset=0;
242       #1;
243       Clock=1;
244       D = 1;
245       #1;
246       Clock=0;
247       Reset=0;
248       #1;
249       Clock=1;
250       D = 1;
251       #1;
252       Clock=0;
253       Reset=0;
254       #1;
255       Clock=1;
256       D = 1;
257       #1;
258       Clock=0;
259       Reset=0;
260       #1;
261       Clock=1;
262       D = 1;
263       #1;
264       Clock=0;
265       Reset=0;
266       #1;
267       Clock=1;
268       D = 1;
269       #1;
270       Clock=0;
271       Reset=0;
272       #1;
273       Clock=1;
274       D = 1;
275       #1;
276       Clock=0;
277       Reset=0;
278       #1;
279       Clock=1;
280       D = 1;
281       #1;
282       Clock=0;
283       Reset=0;
284       #1;
285       Clock=1;
286       D = 1;
287       #1;
288       Clock=0;
289       Reset=0;
290       #1;
291       Clock=1;
292       D = 1;
293       #1;
294       Clock=0;
295       Reset=0;
296       #1;
297       Clock=1;
298       D = 1;
299       #1;
300       Clock=0;
301       Reset=0;
302       #1;
303       Clock=1;
304       D = 1;
305       #1;
306       Clock=0;
307       Reset=0;
308       #1;
309       Clock=1;
310       D = 1;
311       #1;
312       Clock=0;
313       Reset=0;
314       #1;
315       Clock=1;
316       D = 1;
317       #1;
318       Clock=0;
319       Reset=0;
320       #1;
321       Clock=1;
322       D = 1;
323       #1;
324       Clock=0;
325       Reset=0;
326       #1;
327       Clock=1;
328       D = 1;
329       #1;
330       Clock=0;
331       Reset=0;
332       #1;
333       Clock=1;
334       D = 1;
335       #1;
336       Clock=0;
337       Reset=0;
338       #1;
339       Clock=1;
340       D = 1;
341       #1;
342       Clock=0;
343       Reset=0;
344       #1;
345       Clock=1;
346       D = 1;
347       #1;
348       Clock=0;
349       Reset=0;
350       #1;
351       Clock=1;
352       D = 1;
353       #1;
354       Clock=0;
355       Reset=0;
356       #1;
357       Clock=1;
358       D = 1;
359       #1;
360       Clock=0;
361       Reset=0;
362       #1;
363       Clock=1;
364       D = 1;
365       #1;
366       Clock=0;
367       Reset=0;
368       #1;
369       Clock=1;
370       D = 1;
371       #1;
372       Clock=0;
373       Reset=0;
374       #1;
375       Clock=1;
376       D = 1;
377       #1;
378       Clock=0;
379       Reset=0;
380       #1;
381       Clock=1;
382       D = 1;
383       #1;
384       Clock=0;
385       Reset=0;
386       #1;
387       Clock=1;
388       D = 1;
389       #1;
390       Clock=0;
391       Reset=0;
392       #1;
393       Clock=1;
394       D = 1;
395       #1;
396       Clock=0;
397       Reset=0;
398       #1;
399       Clock=1;
400       D = 1;
401       #1;
402       Clock=0;
403       Reset=0;
404       #1;
405       Clock=1;
406       D = 1;
407       #1;
408       Clock=0;
409       Reset=0;
410       #1;
411       Clock=1;
412       D = 1;
413       #1;
414       Clock=0;
415       Reset=0;
416       #1;
417       Clock=1;
418       D = 1;
419       #1;
420       Clock=0;
421       Reset=0;
422       #1;
423       Clock=1;
424       D = 1;
425       #1;
426       Clock=0;
427       Reset=0;
428       #1;
429       Clock=1;
430       D = 1;
431       #1;
432       Clock=0;
433       Reset=0;
434       #1;
435       Clock=1;
436       D = 1;
437       #1;
438       Clock=0;
439       Reset=0;
440       #1;
441       Clock=1;
442       D = 1;
443       #1;
444       Clock=0;
445       Reset=0;
446       #1;
447       Clock=1;
448       D = 1;
449       #1;
450       Clock=0;
451       Reset=0;
452       #1;
453       Clock=1;
454       D = 1;
455       #1;
456       Clock=0;
457       Reset=0;
458       #1;
459       Clock=1;
460       D = 1;
461       #1;
462       Clock=0;
463       Reset=0;
464       #1;
465       Clock=1;
466       D = 1;
467       #1;
468       Clock=0;

```

```
$ iverilog -Wall -o dff_AsyncReset_tb.vvp dff_AsyncReset_tb.v dff_AsyncReset.v
```

```
$ vvp dff_AsyncReset_tb.vvp
```

VCD info: dumpfile dff\_AsyncReset\_tb.vcd opened for output.

Clock=0,D=x,Q=0

Clock=1,D=1,Q=1

Clock=0,D=1,Q=1

Clock=1,D=0,Q=0

Clock=0,D=0,Q=0

Clock=1,D=0,Q=0

Clock=0,D=0,Q=0

Clock=1,D=1,Q=1

Clock=0,D=1,Q=0

Clock=1,D=1,Q=0

\$ 1s

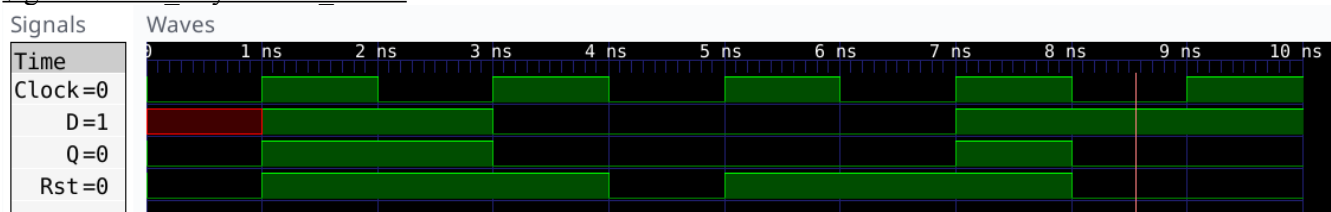
dff\_AsyncReset\_tb.v

dff\_AsyncReset\_tb.vcd

dff\_AsyncReset\_tb.vvp

dff AsyncReset.v

```
$ gtkwave dff AsyncReset tb.vcd
```

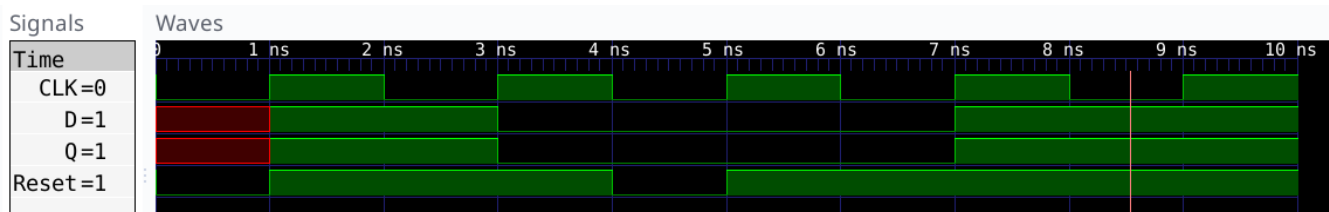


# Άσκηση 5

```
1 timescale 1ns / 1ps
2 module dff_SyncReset_tb;
3   reg Clock, Reset, D;
4   wire Q;
5
6   dff_SyncReset DUT(.Clock(Clock),.D(D),.Reset(Reset),
7     .Q(Q));
8   initial begin
9     $dumpfile("dff_SyncReset_tb.vcd");
10    $dumpvars;
11    Clock=0;
12    Reset = 0;
13    D = 1'bx;
14    #1;
15    Clock=1;
16    D = 1;
17    Reset = 1;
18    #1;
19    Clock=0;
20    #1;
21    Clock=1;
22    D = 0;
23    #1;
24    Clock=0;
25    Reset=0;
26    #1;
27    Clock=1;
28    Reset = 1;
29    #1;
30    Clock=0;
31    #1;
32    Clock=1;
33    D = 1;
34    #1;
35    Clock=0;
36    Reset=0;
37    #1;
38    Clock=1;
39    D = 0;
40    #1;
41    Clock=0;
42    Reset=1;
43    #1;
44    Clock=1;
45    D = 1;
46    #1;
47    Clock=0;
48    Reset=0;
49    #1;
50    Clock=1;
51    D = 0;
52    #1;
53    Clock=0;
54    Reset=1;
55    #1;
56    Clock=1;
57    D = 1;
58    #1;
59    Clock=0;
60    Reset=0;
61    #1;
62    Clock=1;
63    D = 0;
64    #1;
65    Clock=0;
66    Reset=1;
67    #1;
68    Clock=1;
69    D = 1;
70    #1;
71    Clock=0;
72    Reset=0;
73    #1;
74    Clock=1;
75    D = 0;
76    #1;
77    Clock=0;
78    Reset=1;
79    #1;
80    Clock=1;
81    D = 1;
82    #1;
83    Clock=0;
84    Reset=0;
85    #1;
86    Clock=1;
87    D = 0;
88    #1;
89    Clock=0;
90    Reset=1;
91    #1;
92    Clock=1;
93    D = 1;
94    #1;
95    Clock=0;
96    Reset=0;
97    #1;
98    Clock=1;
99    D = 0;
100   #1;
101   Clock=0;
102   Reset=1;
103   #1;
104   Clock=1;
105   D = 1;
106   #1;
107   Clock=0;
108   Reset=0;
109   #1;
110   Clock=1;
111   D = 0;
112   #1;
113   Clock=0;
114   Reset=1;
115   #1;
116   Clock=1;
117   D = 1;
118   #1;
119   Clock=0;
120   Reset=0;
121   #1;
122   Clock=1;
123   D = 0;
124   #1;
125   Clock=0;
126   Reset=1;
127   #1;
128   Clock=1;
129   D = 1;
130   #1;
131   Clock=0;
132   Reset=0;
133   #1;
134   Clock=1;
135   D = 0;
136   #1;
137   Clock=0;
138   Reset=1;
139   #1;
140   Clock=1;
141   D = 1;
142   #1;
143   Clock=0;
144   Reset=0;
145   #1;
146   Clock=1;
147   D = 0;
148   #1;
149   Clock=0;
150   Reset=1;
151   #1;
152   Clock=1;
153   D = 1;
154   #1;
155   Clock=0;
156   Reset=0;
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161   Clock=0;
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168   Reset=0;
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172   #1;
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174   Reset=1;
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204   Reset=0;
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1099  #1;
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1104  Reset=0;
1105  #1;
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1107  D = 0;
1108  #1;
1109  Clock=0;
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1114  #1;
1115  Clock=0;
1116  Reset=0;
1117  #1;
1118  Clock=1;
1119  D = 0;
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1122  Reset=1;
1123  #1;
1124  Clock=1;
1125  D = 1;
1126  #1;
1127  Clock=0;
1128  Reset=0;
1129  #1;
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1134  Reset=1;
1135  #1;
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1137  D = 1;
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1146  Reset=1;
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1170  Reset=1;
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1173  D = 1;
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1176  Reset=0;
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1182  Reset=1;
1183  #1;
1184  Clock=1;
1185  D = 1;
1186  #1;
1187  Clock=0;
1188  Reset=0;
1189  #1;
1190  Clock=1;
1191  D = 0;
1192  #1;
1193  Clock=0;
1194  Reset=1;
1195  #1;
1196  Clock=1;
1197  D = 1;
1198  #1;
1199  Clock=0;
1200  Reset=0;
1201  #1;
1202  Clock=1;
1203  D = 0;
1204  #1;
1205  Clock=0;
1206  Reset=1;
1207  #1;
1208  Clock=1;
1209  D = 1;
1210  #1;
1211  Clock=0;
1212  Reset=0;
1213  #1;
1214  Clock=1;
1215  D = 0;
1216  #1;
1217  Clock=0;
1218  Reset=1;
1219  #1;
1220  Clock=1;
1221  D = 1;
1222  #1;
1223  Clock=0;
1224  Reset=0;
1225  #1;
1226  Clock=1;
1227  D = 0;
1228  #1;
1229  Clock=0;
1230  Reset=1;
1231  #1;
1232  Clock=1;
1233  D = 1;
1234  #1;
1235  Clock=0;
1236  Reset=0;
1237  #1;
1238  Clock=1;
1239  D = 0;
1240  #1;
1241  Clock=0;
1242  Reset=1;
1243  #1;
1244  Clock=1;
1245  D = 1;
1246  #1;
1247  Clock=0;
1248  Reset=0;
1249  #1;
1250  Clock=1;
1251  D = 0;
1252  #1;
1253  Clock=0;
1254  Reset=1;
1255  #1;
1256  Clock=1;
1257  D = 1;
1258  #1;
1259  Clock=0;
1260  Reset=0;
1261  #1;
1262  Clock=1;
1263  D = 0;
1264  #1;
1265  Clock=0;
1266  Reset=1;
1267  #1;
1268  Clock=1;
1269  D = 1;
1270  #1;
1271  Clock=0;
1272  Reset=0;
1273  #1;
1274  Clock=1;
1275  D = 0;
1276  #1;
1277  Clock=0;
1278  Reset=1;
1279  #1;
1280  Clock=1;
1281  D = 1;
1282  #1;
1283  Clock=0;
1284  Reset=0;
1285  #1;
1286  Clock=1;
1287  D = 0;
1288  #1;
1289  Clock=0;
1290  Reset=1;
1291  #1;
1292  Clock=1;
1293  D = 1;
1294  #1;
1295  Clock=0;
1296  Reset=0;
1297  #1;
1298  Clock=1;
1299  D = 0;
1300  #1;
1301  Clock=0;
1302  Reset=1;
1303  #1;
1304  Clock=1;
1305  D = 1;
1306  #1;
1307  Clock=0;
1308  Reset=0;
1309  #1;
1310  Clock=1;
1311  D = 0;
1312  #1;
1313  Clock=0;
1314  Reset=1;
1315  #1;
1316  Clock=1;
1317  D = 1;
1318  #1;
1319  Clock=0;
1320  Reset=0;
1321  #1;
1322  Clock=1;
1323  D = 0;
1324  #1;
1325  Clock=0;
1326  Reset=1;
1327  #1;
1328  Clock=1;
1329  D = 1;
1330  #1;
1331  Clock=0;
1332  Reset=0;
1333  #1;
1334  Clock=1;
1335  D = 0;
1336  #1;
1337  Clock=0;
1338  Reset=1;
1339  #1;
1340  Clock=1;
1341  D = 1;
1342  #1;
1343  Clock=0;
1344  Reset=0;
1345  #1;
1346  Clock=1;
1347  D = 0;
1348  #1;
1349  Clock=0;
1350  Reset=1;
1351  #1;
1352  Clock=1;
1353  D = 1;
1354  #1;
1355  Clock=0;
1356  Reset=0;
1357  #1;
1358  Clock=1;
1359  D = 0;
1360  #1;
1361  Clock=0;
1362  Reset
```

# Another testbench

```
1 timescale 1ns / 1ps
2 module dff_SyncReset_tb;
3     reg Clock, Reset, D;
4     wire Q;
5
6     dff_SyncReset DUT(.Clock(Clock), .D(D), .Reset(Reset),
7                       .Q(Q));
8     initial begin
9         $dumpfile("dff_SyncReset_tb.vcd");
10        $dumpvars;
11        Clock=0;
12        Reset = 0;
13        D = 1'bx;
14        #1; Clock=1;
15        D = 1;
16        Reset = 1;
17        #1; Clock=0;
18        #1; Clock=1;
19        D = 0;
20        #1; Clock=0;
21        Reset=0;
22        #1; Clock=1;
23        Reset = 1;
24        #1; Clock=0;
25        #1; Clock=1;
26        D = 1;
27        #1; Clock=0;
28        #1; Clock=1;
29        #1;
30    end
31    initial begin
32        $monitor("Clock=%d,D=%d,Q=%d \n",Clock,D,Q);
33    end
34 endmodule
35
36
```



# Άσκηση 6

1 / 1 + -

Terminal Default

...laptop: ~/Μαθήματα/Οργάνωση ΗΥ/2020-2021/Οργάνωση ΗΥ (Εργαστήριο)/lab2/homework6

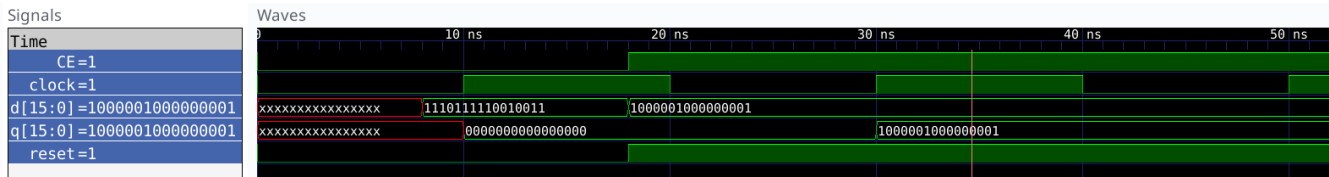
```
1 timescale 1ns / 1ps
2 module dff16 SyncReset_tb;
3   reg [15:0] d;
4   reg clock;
5   reg reset;
6   reg CE;
7   wire [15:0] q;
8
9   dff16_SyncReset DUT(.d(d),.clock(clock),.reset(reset),.CE(CE),
10     .q(q));
11   integer i;
12   initial begin
13     $dumpfile("dff16_SyncReset_tb.vcd");
14     $dumpvars;
15     clock=1'b0;
16     reset=0;
17     // forever #10 CLK = ~CLK;
18     // OR
19     for (i=0; i <=10; i=i+1)
20       #10 clock = ~clock;
21   end
22
23   initial begin
24     reset=0;
25     CE=1'b0;
26     d <= 16'bxxxxxxxxxxxxxxx;
27     #8; d <= 16'b1110111110010011;
28     #10; reset=1;
29     CE=1'b1;
30     d <= 16'b1000001000000001;
31     #10;
32   end
33   initial begin
34     $monitor("Clock=%d,d=%d,q=%d \n",clock,d,q);
35   end
36 endmodule
```

NORMAL dff16\_SyncReset\_tb.v unix | utf-8 | verilog 2% 1:1  
"dff16\_SyncReset\_tb.v" [noeol] 36L, 797C

...laptop: ~/Μαθήματα/Οργάνωση ΗΥ/2020-2021/Οργάνωση ΗΥ (Εργαστήριο)/lab2/homework6

```
1 timescale 1ns / 1ps
2
3 module dff16 SyncReset (clock, CE, d, q, reset);
4   input clock;
5   input CE;
6   input [15:0] d;
7   input reset;
8   output reg [15:0] q;
9
10
11 always @ (posedge clock)
12   begin
13
14     if(!reset)
15       q <= 16'b0000000000000000;
16     else
17       if ( CE == 1)
18         q <= d;
19     end
20
21 endmodule
```

NORMAL dff16\_SyncReset.v unix | utf-8 | verilog 4% 1:1  
"dff16\_SyncReset.v" 21L, 285C

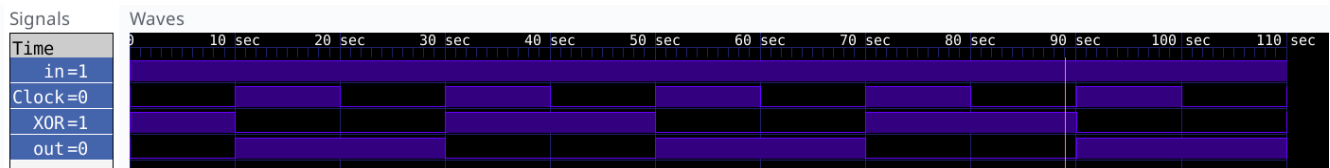




## Άσκηση 7

```
1 // timescale 1ns / 1ps
2 include "toplevel_hw_7.v"
3
4 module homework7_tb;
5     reg in;
6     reg Clock;
7     wire out;
8
9     toplevel_hw_7 DUT(.in(in),.Clock(Clock),
10         .out(out));
11     integer i;
12     initial begin
13         $dumpfile("homework7_tb.vcd");
14         $dumpvars;
15         in=1;
16         Clock=0;
17         // forever #10 CLK = ~CLK;
18         //         OR
19         for (i=0; i <=10; i=i+1)
20             #10 Clock = ~Clock;
21     end
22     initial begin
23         in <= 0;
24         #8; in <= 0;
25         #10; in <= 0;
26         #10; in <= 1;
27         #10; in <= 1;
28         #10; in <= 1;
29         #10; in <= 1;
30         #10;
31     end
32     initial begin
33         $monitor("Clock=%d,D=%d,out=%d \n",Clock,in,out);
34     end
35 endmodule
```

**NORMAL** homework7\_tb.v    unix | utf-8 | verilog    2%    1:1  
"homework7\_tb.v" 35L, 702C



## Άσκηση 10

1 / 1 + - □ □

Terminal Data

⋮ - □ ×

...ptop: ~/Μαθήματα/Οργάνωση ΗΥ/2020-2021/Οργάνωση ΗΥ (Εργαστήριο)/lab2/homework10 ▾ □ ×

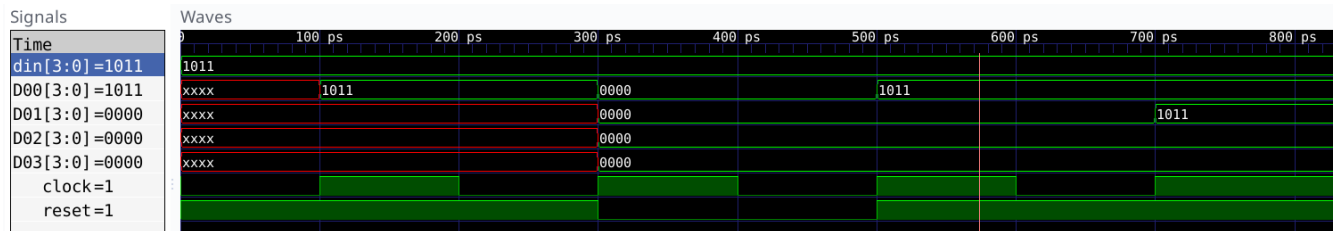
```
1 timescale 1ns/1ps
2
3 module shiftReg4_tb;
4 reg [3:0]din;
5 reg clock, reset;
6 wire [3:0]D00, D01, D02, D03;
7
8 shiftReg4 DUT( .din(din), .clock(clock), .reset(reset),
9 .D00(D00), .D01(D01), .D02(D02), .D03(D03));
10
11 initial begin
12     $dumpfile("shiftReg4_tb.vcd");
13     $dumpvars;
14
15     reset=1'b1;
16     clock=1'b0;
17     din=4'b1011;
18     #0.1 clock=1'b1;
19     #0.1 clock=1'b0;
20     #0.1 clock=1'b1;
21     reset=1'b0;
22     #0.1 clock=1'b0;
23     #0.1 clock=1'b1;
24     reset=1'b1;
25     #0.1 clock=1'b0;
26     #0.1 clock=1'b1;
27     #1
28 end
29 endmodule
```

INSERT shiftReg4\_tb.v | + unix | utf-8 | verilog 3% 1:1  
-- INSERT --

...ptop: ~/Μαθήματα/Οργάνωση ΗΥ/2020-2021/Οργάνωση ΗΥ (Εργαστήριο)/lab2/homework10 ▾ □ ×

```
1 timescale 1ns/1ps
2
3 module shiftReg4(
4     input [3:0] din,
5     input clock, reset,
6     output reg [3:0] D00, D01, D02, D03);
7
8 always @(posedge clock)
9     begin
10         if(!reset)
11             begin
12                 D00 <= 4'b0;
13                 D01 <= 4'b0;
14                 D02 <= 4'b0;
15                 D03 <= 4'b0;
16             end
17         else
18             begin
19                 D00 <= din;
20                 D01 <= D00;
21                 D02 <= D01;
22                 D03 <= D02;
23             end
24         end
25     end
26
27 endmodule
```

NORMAL shiftReg4.v | unix | utf-8 | verilog 3% 1:1  
"shiftReg4.v" 27L, 517C



## Άσκηση 12

```
1 timescale 1ns/1ps
2 module stimulus;
3 reg clk, load,enable;
4 reg reset;
5 reg s_in;
6 wire s_out;
7 free_run_shift_reg #(2) s1 (
8 .clk(clk),
9 .reset(reset),
10 .s_in(s_in),
11 .s_out(s_out),
12 .enable(enable),
13 .load(load)
14 );
15 integer i, j;
16 initial
17 begin
18 clk = 0;
19 for(i=0; i<=40; i=i+1)
20 begin
21 #10 clk = ~clk;
22 end
23 end
24 initial
25 begin
26 $dumpfile("test.vcd");
27 $dumpvars(0,stimulus);
28 s_in = 0; reset = 1;
29 enable=1; load=1;
30 #2 s_in = 0 ; reset = 0;
31 #2 reset =1;
32 for(i=0; i<=10; i=i+1)
33 begin
34 #20 s_in = ~s_in;
35 end
36 #20 s_in =1;
37 end
38 endmodule
```

```
1 module free_run_shift_reg
2 #(parameter N=4)
3 (
4 input wire clk, reset,
5 input wire s_in,
6 input enable,load,
7 output wire s_out
8 );
9 reg [N-1:0] r_reg;
10 wire [N-1:0] r_next;
11
12 always @(posedge clk, negedge reset)
13 begin
14 if (!reset)
15 r_reg <= 0;
16 else if(!load)
17 r_reg=3;
18 else
19 if(enable)
20 r_reg <= r_next;
21 end
22 assign r_next = {s_in, r_reg[N-1:1]};
23 assign s_out = r_reg[0];
24
25 endmodule
```

unix | utf-8 | verilog | 2% | 1:1

unix | utf-8 | verilog | 4% | 1:1

"shiftReg4.v" 25L, 368C

Signals

Time
clk=1
enable=1
load=1
reset=1
s_in=1
s_out=0

Waves

