Μοσχογιάννης Πασχάλης ΑΜ 2114026

Άσκηση 1

Terminal Default

...laptop: ~/Μαθήματα/Οργάνωση ΗΥ/2020-2021/Οργάνωση ΗΥ (Εργαστήριο)/lab3/homework1

```
1  timescale 1ns/1ps
2
3  module fsm_tb;
4
5      reg clk, reset, in;
6      wire out;
7
8      fsm DUT( .out(out), .clk(clk), .reset(reset), .in(in));
9
10     initial begin
11     $dumpfile("fsm_tb.vcd");
12     $dumpvars;
13
14     clk=0;
15     reset=0;
16     in=0;
17
18     #0.1 reset=1;
19     #0.1 clk=1; in=1;
20     #0.1 clk=0;
21     #0.1 clk=1; in=0;
22     #0.1 clk=0;
23     #0.1 clk=1; in=1;
24     #0.1 clk=0;
25     #0.1 clk=1; in=0;
26     #0.1 clk=0;
27     #0.1
28
29     end
30 endmodule
```

NORMAL fsm_tb.v unix | utf-8 | verilog 3% 1:1

...aptop: ~/Μαθήματα/Οργάνωση ΗΥ/2020-2021/Οργάνωση ΗΥ (Εργαστήριο)/lab3/homework1

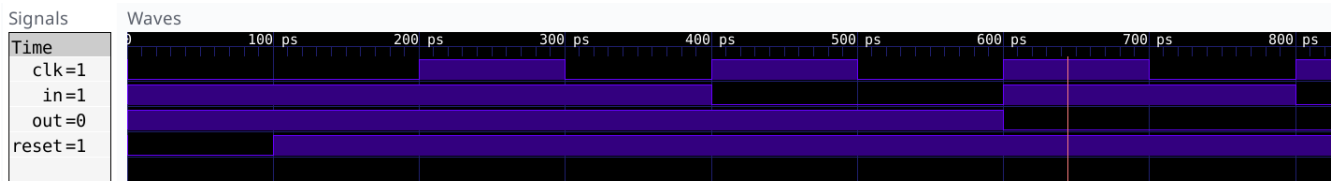
```
1  timescale 1ns/1ps
2  module fsm (output reg out, input wire clk, reset, in);
3
4      reg state;
5      parameter B=0, A=1;
6
7      always @(posedge clk or negedge reset)
8      if(reset==1'b0)
9          begin
10         state=B;
11         out=1;
12         end
13     else
14         begin
15         case (state)
16         B:
17             begin
18                 out=1;
19                 if(in==0)
20                     state=A;
21                 else
22                     state=B;
23             end
24         A:
25             begin
26                 out=0;
27                 if(in==0)
28                     state=B;
29                 else
30                     state=A;
31             end
32         default: state=B;
33         endcase
34     end
35 endmodule
```

NORMAL fsm.v unix | utf-8 | verilog 2% 1:1

iverilog - Icarus Verilog compiler Version 10.2 (stable)
vvp - Icarus Verilog vvp runtime engine Version 10.2 (stable)

```
$ iverilog -Wall -o fsm_tb.vvp fsm_tb.v fsm.v
$ vvp fsm_tb.vvp
$ ls
fsm_tb.v
fsm_tb.vcd
fsm_tb.vvp
fsm.v
```

```
$ gtkwave fsm_tb.vcd
```



Άσκηση 2

Terminal Default

...laptop: ~/Μαθήματα/Οργάνωση Η/Υ/2020-2021/Οργάνωση Η/Υ (Εργαστήριο)/lab3/homework2

```
1  `timescale 1ns/1ps
2
3  module fsm_tb;
4
5      reg clk, reset, j, k;
6      wire out;
7
8      fsm DUT( .out(out), .clk(clk), .reset(reset), .j(j), .k(k));
9
10     initial begin
11     $dumpfile("fsm_tb.vcd");
12     $dumpvars;
13
14     clk=0;
15     reset=0;
16     j=0;
17     k=0;
18
19     #0.1 reset=1;
20     #0.1 clk=1; j=0;
21     #0.1 clk=0;
22     #0.1 clk=1; j=1;
23     #0.1 clk=0;
24     #0.1 clk=1; k=0;
25     #0.1 clk=0;
26     #0.1 clk=1; k=1;
27     #0.1 clk=0;
28
29     end
30 endmodule
```

NORMAL fsm_tb.v unix | utf-8 | verilog 3% 1:1

"fsm_tb.v" [noeol] 30L, 435C

...aptop: ~/Μαθήματα/Οργάνωση Η/Υ/2020-2021/Οργάνωση Η/Υ (Εργαστήριο)/lab3/homework2

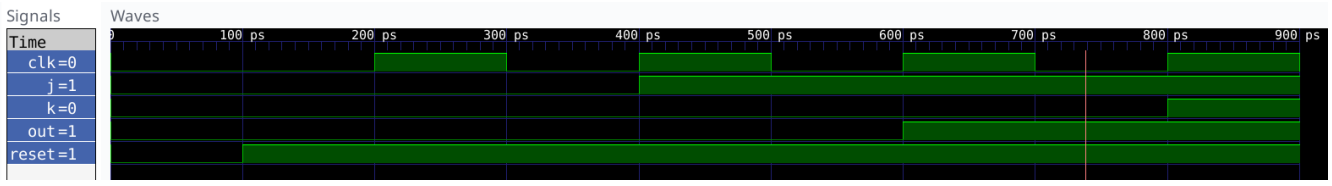
```
1  `timescale 1ns/1ps
2  module fsm (output reg out, input wire clk, reset, j, k);
3      reg state;
4      parameter OFF=0, ON=1;
5      always @(posedge clk or negedge reset)
6          if(reset==1'b0)
7              begin
8              state=OFF;
9              out=0;
10             end
11         else
12             begin
13                 case (state)
14                 OFF:
15                     begin
16                     out=0;
17                     if(j==1)
18                         state=ON;
19                     else
20                         state=OFF;
21                     end
22                 ON:
23                     begin
24                     out=1;
25                     if(k==0)
26                         state=ON;
27                     else
28                         state=OFF;
29                     end
30                 default: state=OFF;
31                 endcase
32             end
33 endmodule
```

NORMAL fsm.v unix | utf-8 | verilog 3% 1:1

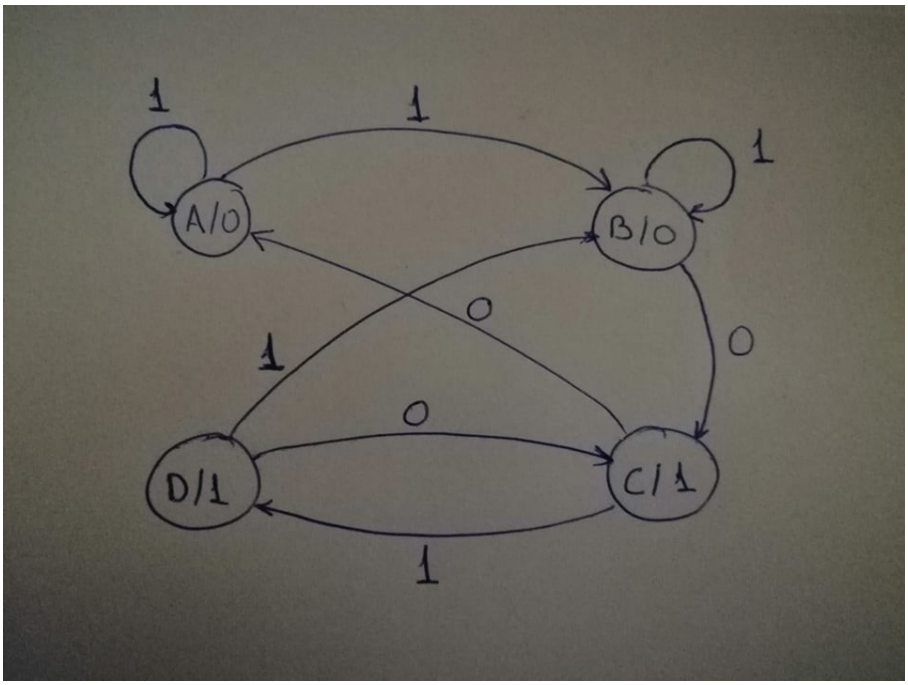
"fsm.v" [noeol] 33L, 852C

$ iverilog -Wall -o fsm_tb.vvp fsm_tb.v fsm.v
$ vvp fsm_tb.vvp
$ ls
fsm_tb.v
fsm_tb.vcd
fsm_tb.vvp
fsm.v

$ gtkwave fsm_tb.vcd



Άσκηση 3



Terminal Default

...laptop: ~/Μαθήματα/Οργάνωση ΗΥ/2020-2021/Οργάνωση ΗΥ (Εργαστήριο)/lab3/homework3

```
1  `timescale 1ns/1ps
2
3  module ask3_tb;
4
5      reg clk, reset, in;
6      wire out;
7
8      ask3 DUT( .out(out), .clk(clk), .reset(reset), .in(in));
9
10     initial begin
11     $dumpfile("ask3_tb.vcd");
12     $dumpvars;
13
14     clk=0;
15     reset=0;
16     in=0;
17
18     #0.1 reset=1;
19     #0.1 clk=1; in=0;
20     #0.1 clk=0;
21     #0.1 clk=1; in=1;
22     #0.1 clk=0;
23     #0.1 clk=1;
24     #0.1 clk=0;
25     #0.1 clk=1; in=0;
26     #0.1 clk=0;
27     #0.1 clk=1; in=1;
28     #0.1 clk=0;
29     #0.1 clk=1; in=1;
30     #0.1 clk=0;
31     #0.1 clk=1; in=0;
32     #0.1 clk=0;
33     #0.1 clk=1;
34     #0.1 clk=0;
35     #0.1 clk=1; in=1;
36     #0.1 clk=0;
```

NORMAL RO | fsm_tb.v unix | utf-8 | verilog 2% 1:1

...aptop: ~/Μαθήματα/Οργάνωση ΗΥ/2020-2021/Οργάνωση ΗΥ (Εργαστήριο)/lab3/homework3

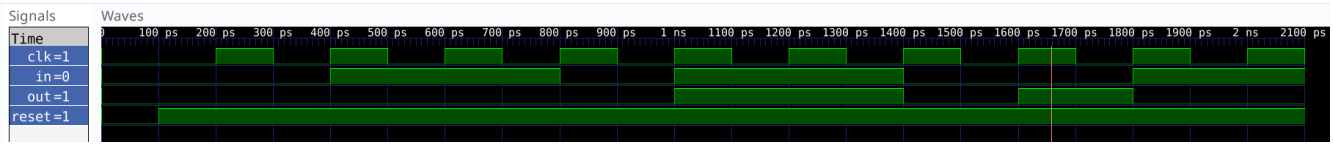
```
1  `timescale 1ns/1ps
2  module ask3 (output reg out, input wire clk, reset, in);
3      reg [1:0]state;
4      parameter A=2'b00, B=2'b01, C=2'b10, D=2'b11;
5      always @(posedge clk or negedge reset)
6          if(reset==1'b0)
7              begin
8              state=A;
9              out=0;
10             end
11         else
12             begin
13             case (state)
14             A:
15                 begin
16                     out=0;
17                     if(in==1) state=B;
18                     else state=A;
19                 end
20             B:
21                 begin
22                     out=0;
23                     if(in==0) state=C;
24                     else state=B;
25                 end
26             C:
27                 begin
28                     out=1;
29                     if(in==1) state=D;
30                     else state=A;
31                 end
32             D:
33                 begin
34                     out=1;
35                     if(in==0) state=C;
36                     else state=B;
```

NORMAL RO | fsm.v unix | utf-8 | verilog 2% 1:1

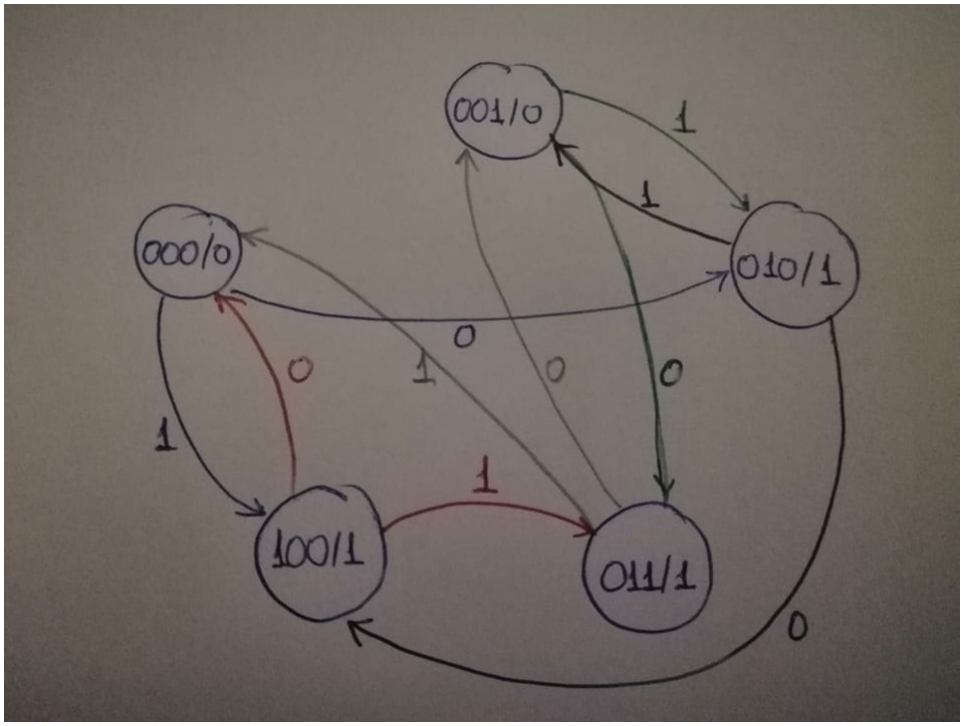
```
$ iverilog -Wall -o fsm_tb.vvp fsm_tb.v fsm.v
$ vvp fsm_tb.vvp
$ ls
fsm_tb.v
fsm_tb.vcd
fsm_tb.vvp
```

fsm.v

$ gtkwave fsm_tb.vcd



Άσκηση 4



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Terminal Default

...laptop: ~/Μαθήματα/Οργάνωση ΗΥ/2020-2021/Οργάνωση ΗΥ (Εργαστήριο)/lab3/homework4

```
1  `timescale 1ns/1ps
2  module ask4_tb;
3      reg clk, reset, in;
4      wire out;
5      ask4 DUT( .out(out), .clk(clk), .reset(reset), .in(in));
6      initial begin
7          $dumpfile("ask4_tb.vcd");
8          $dumpvars;
9          clk=0;
10         reset=0;
11         in=0;
12         #0.1 reset=1;
13         #0.1 clk=1; in=1;
14         #0.1 clk=0;
15         #0.1 clk=1; in=0;
16         #0.1 clk=0;
17         #0.1 clk=1;
18         #0.1 clk=0;
19         #0.1 clk=1;
20         #0.1 clk=0;
21         #0.1 clk=1; in=1;
22         #0.1 clk=0;
23         #0.1 clk=1; in=0;
24         #0.1 clk=0;
25         #0.1 clk=1;
26         #0.1 clk=0;
27         #0.1 clk=1; in=1;
28         #0.1 clk=0;
29         #0.1 clk=1; in=0;
30         #0.1 clk=0;
31         #0.1 clk=1; in=1;
32         #0.1 clk=0;
33         #0.1 clk=1;
34         #0.1 clk=0;
35         end
36 endmodule
```

NORMAL RO | fsm_tb.v unix | utf-8 | verilog 2% 1:1

"fsm_tb.v" [readonly] 36L, 643C

...aptop: ~/Μαθήματα/Οργάνωση ΗΥ/2020-2021/Οργάνωση ΗΥ (Εργαστήριο)/lab3/homework4

```
1  `timescale 1ns/1ps
2  module ask4 (output reg out, input wire clk, reset, in);
3
4      reg [2:0]state;
5      parameter A=3'b000, B=3'b001, C=3'b010, D=3'b011, E=3'b100;
6
7      always @(posedge clk or negedge reset)
8          if(reset==1'b0)
9              begin
10                 state=A;
11                 out=0;
12             end
13         else
14             begin
15                 case (state)
16                     A:
17                         begin
18                             out=0;
19                             if(in==0) state=C;
20                             else state=E;
21                         end
22                     B:
23                         begin
24                             out=0;
25                             if(in==0) state=D;
26                             else state=C;
27                         end
28                     C:
29                         begin
30                             out=1;
31                             if(in==0) state=E;
32                             else state=B;
33                         end
34                     D:
35                         begin
36                             out=1;
```

NORMAL RO | fsm.v unix | utf-8 | verilog 2% 1:1

"fsm.v" [readonly] 49L, 1489C

$ iverilog -Wall -o fsm_tb.vvp fsm_tb.v fsm.v
$ vvp fsm_tb.vvp
$ ls
fsm_tb.v
fsm_tb.vcd
fsm_tb.vvp
fsm.v

$ gtkwave fsm_tb.vcd