Implementation of UART with CRC Error Detection

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Information

Course: PGS618 Dependable Systems

Implement and evaluate an error resilient technique on hardware

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Background: UART Communication

Sending 'M' (0x4D, 01001101 in binary) via UART at 9600 bps includes a start bit (0), data bits (LSB first: 10110010), and a stop bit (1). Each bit lasts 104.17 µs, making the total frame duration 1041.70 µs, as shown in **Figure 1**.

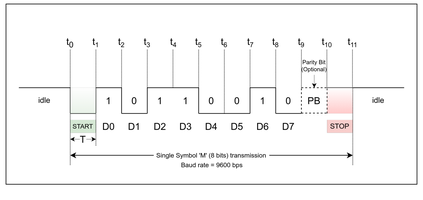


Figure 1. The UART frame.

Errors during data transmission can be detected by checking the parity of the received data. In **Figure 2**, a parity bit, shown as a rectangular patch next to the binary sequence, helps identify errors. If the parity bit does not align with the data's sum (odd with even parity or even with odd parity), it indicates a transmission error.

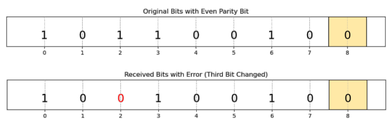


Figure 2. Received bits with an error in the third bit, incorporating an even parity bit.

Background: CRC Error Detection

In CRC encoding, an 8-bit checksum is generated using the polynomial x^8+x^2+x+1 (100000111) to verify data integrity **Figure 3**. The verification process rechecks the message with the appended check value; a zero remainder confirms no detectable errors **Figure 4**.

Figure 3. CRC calculation with bit alignment.

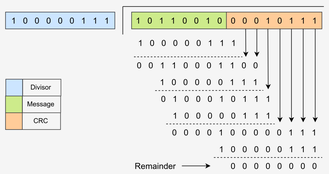


Figure 4. Zero remainder for error-free data.

Proposed Methodology

The UART transmitter state machine **Figure 5** manages data and CRC transmission through multiple states, from IDLE to STOP_BIT, ensuring complete transmission cycles.

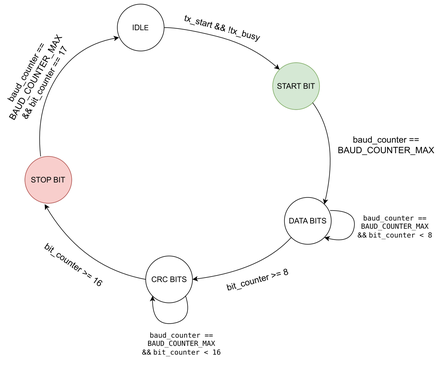


Figure 5. UART Transmitter state machine.

The UART receiver state machine **Figure 6** handles data, CRC reception, and stop bit validation, ensuring accurate data capture and completion before returning to idle.

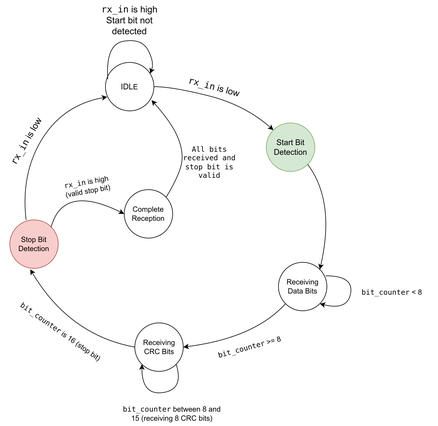
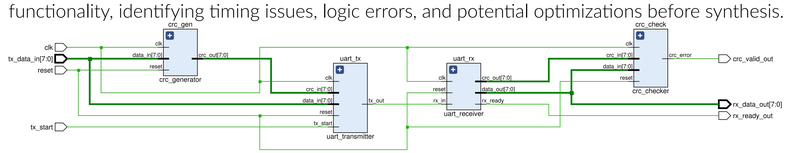


Figure 6. UART Receiver state machine.

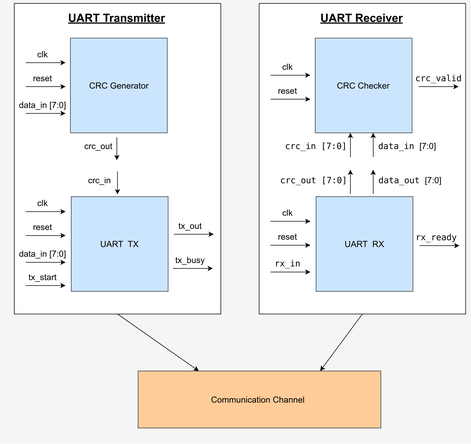
RTL Analysis Schematic for the 'uart_crc_top' Module

The RTL Analysis Schematic for the uart_crc_top module visually represents the logic-level interactions, interconnections, data paths, and control signals essential for verifying design functionality, identifying timing issues, logic errors, and potential optimizations before synthesis.



The structure diagram of UART

The diagram illustrates the interconnection of signals between modules, representing the structure of the proposed methodology.



Experimental Setup, Results, and Analysis

The simulation software is Xilinx's Vivado Design Suite, and the selected FPGA device is the Nexys A7-100T featuring the part number XC7A100T-1CSG324C.

Figure 7. Simulation Results of UART with CRC Error Detection

References

GitHub QR code

References QR Code