

# SoC wave generation design



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# Agenda

- Overview on AXI
- Architecture
- Interfacing
- VHDL Core and Process
- Functionality of wave generator
- Algorithm of wave generator
- Reports of ISE



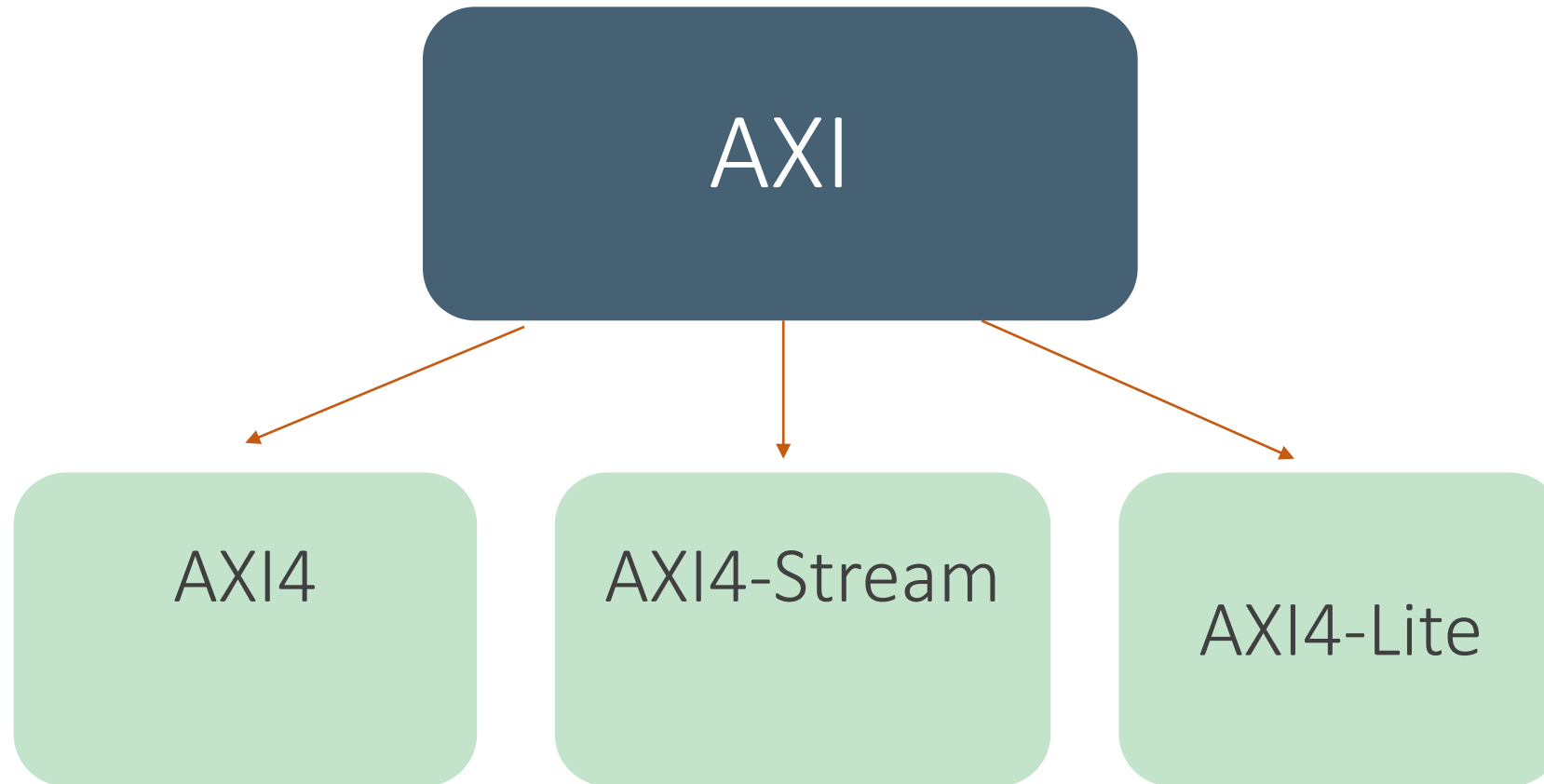
# Tools

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- 1- Xilinx Platform Studio
- 2- Xilinx ISE
- 3- Xilinx SDK
- 4- I Simulator



AXI



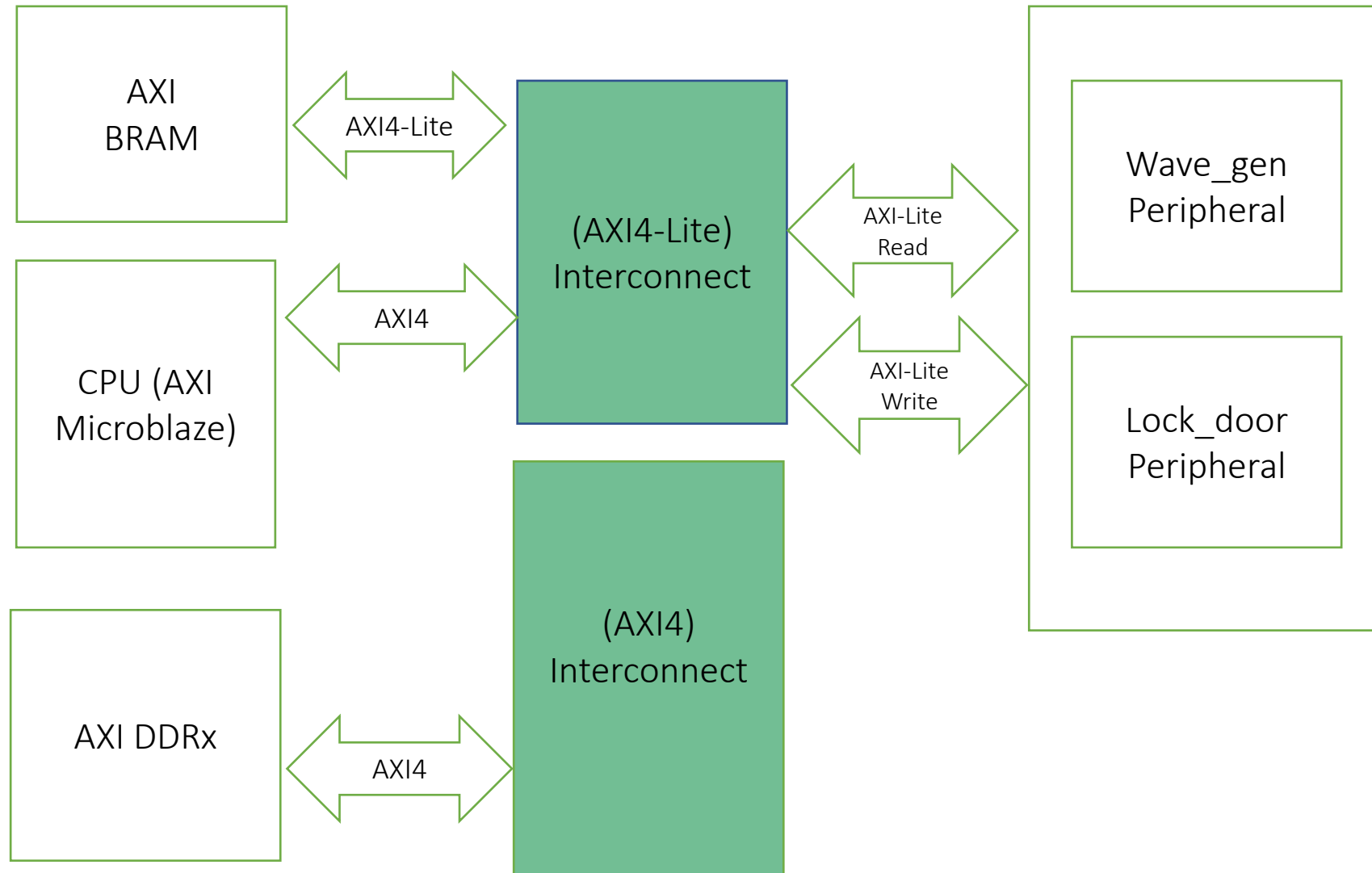


# AXI

Interface	Features	Burst	Data Width
AXI4	Traditional address/Data Burst	UP to 256	32 to 1024 bits
AXI4-Stream	Data-only-Burst unidirectional	Unlimited	Any Number
AXI4-Lite	Traditional address Single address, Single data	1	32 or 64 bits

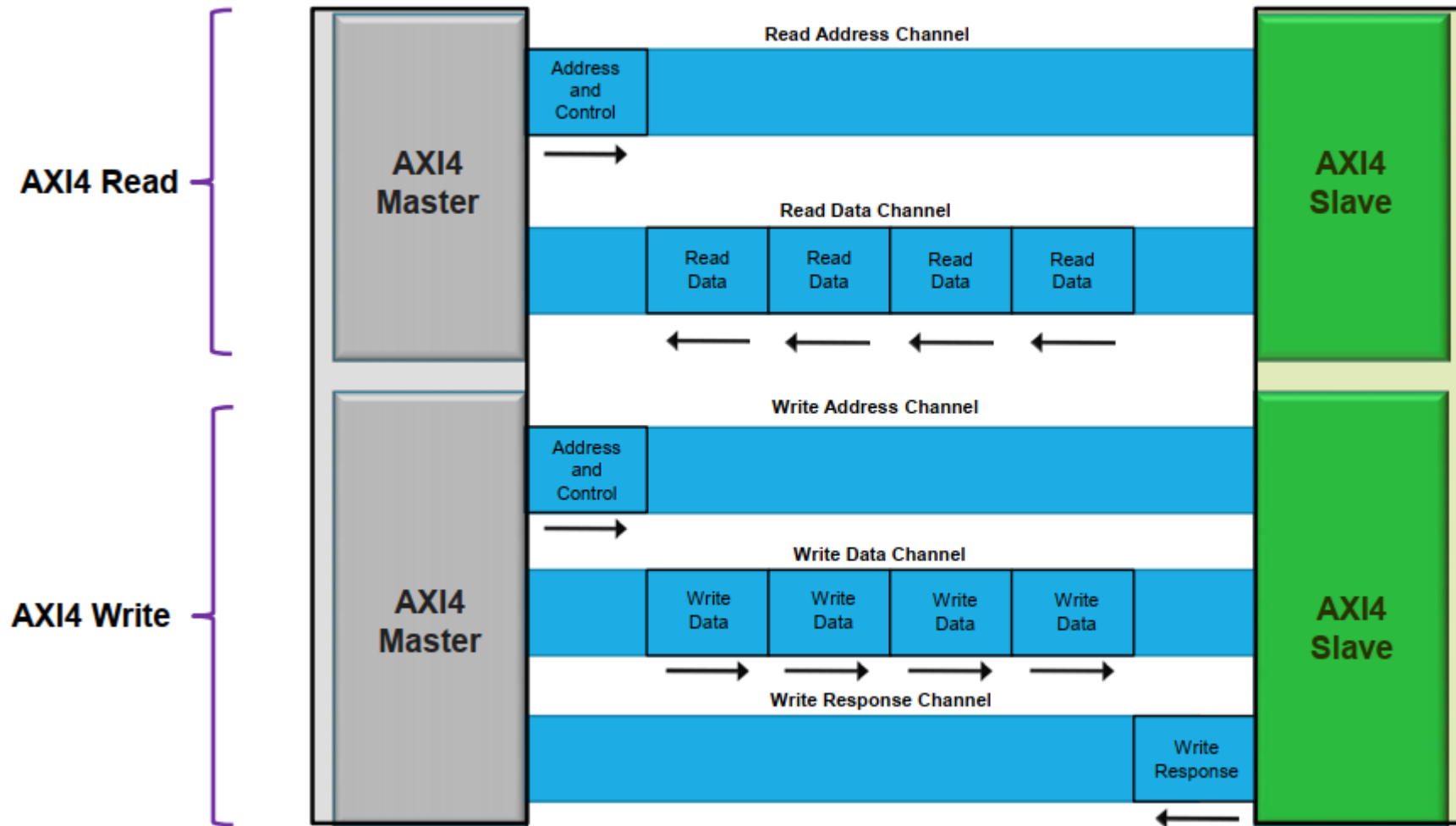


# Architecture



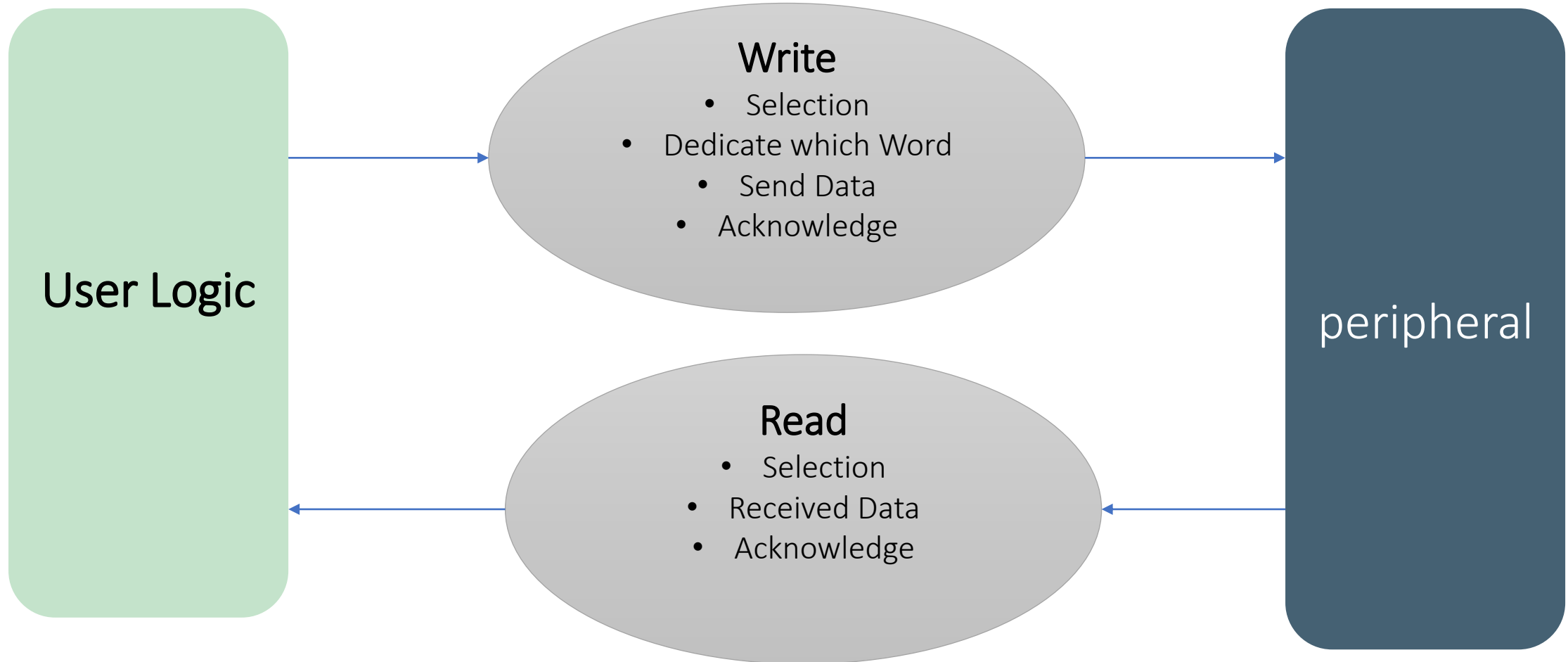


# Interfacing





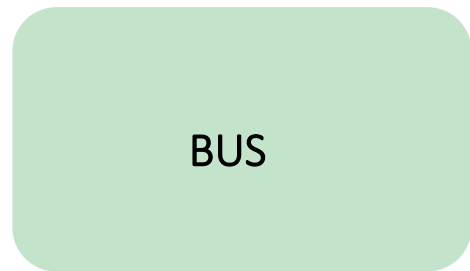
## Process







# VHDL Core



## User Logic

Top module

sine  
gen 1

sine  
gen 2



# Functionality of wave generator

theory

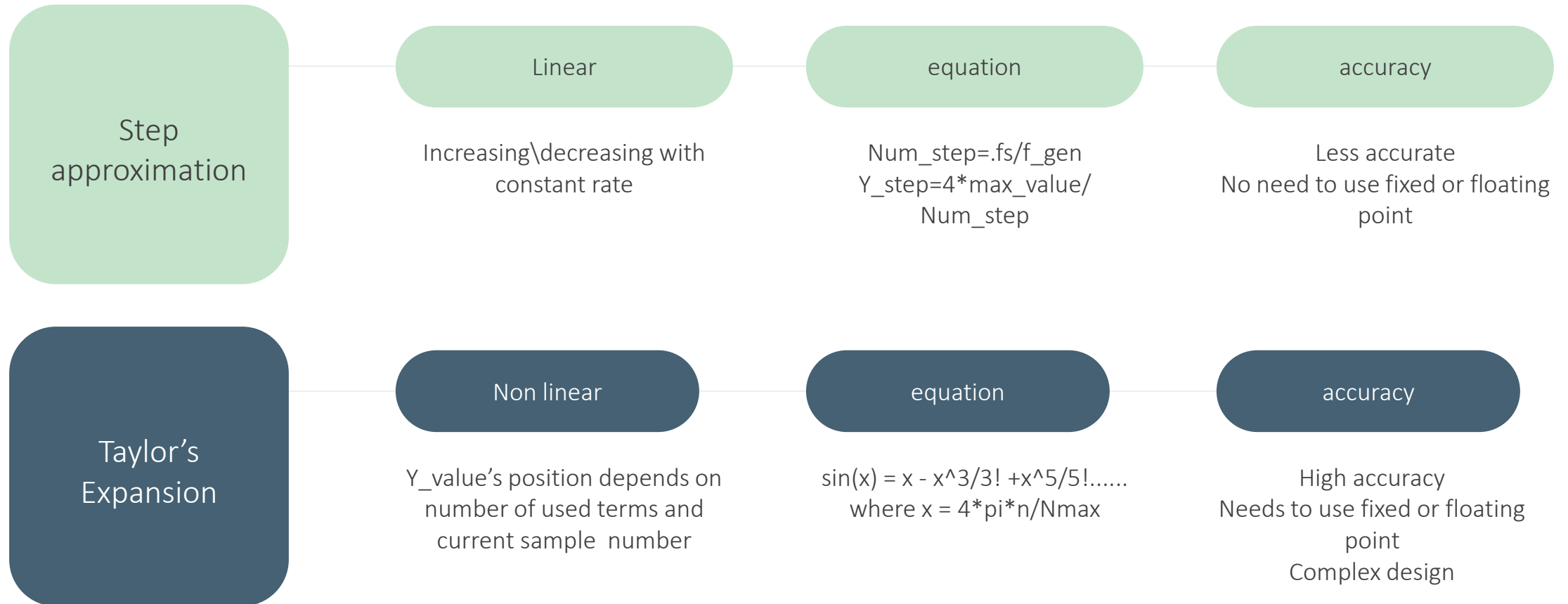
To generate wave in digital form:

The frequency which is used to sample the wave should be at least the double of frequency of generated wave

According to Nyquist theory  $f_s \geq 2f$ .



# Algorithm of wave generator



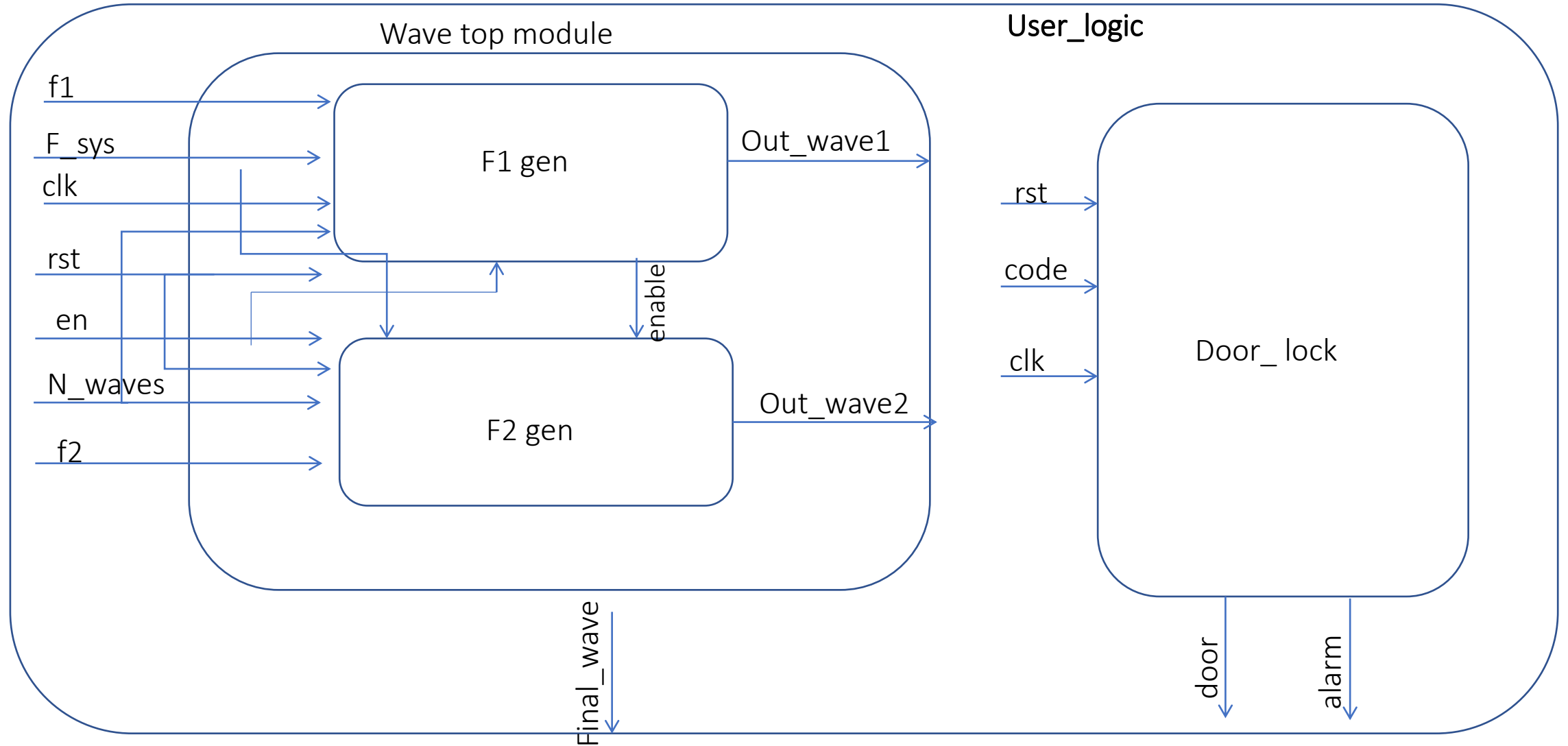


## Architecture of wave generator





## Proposed design





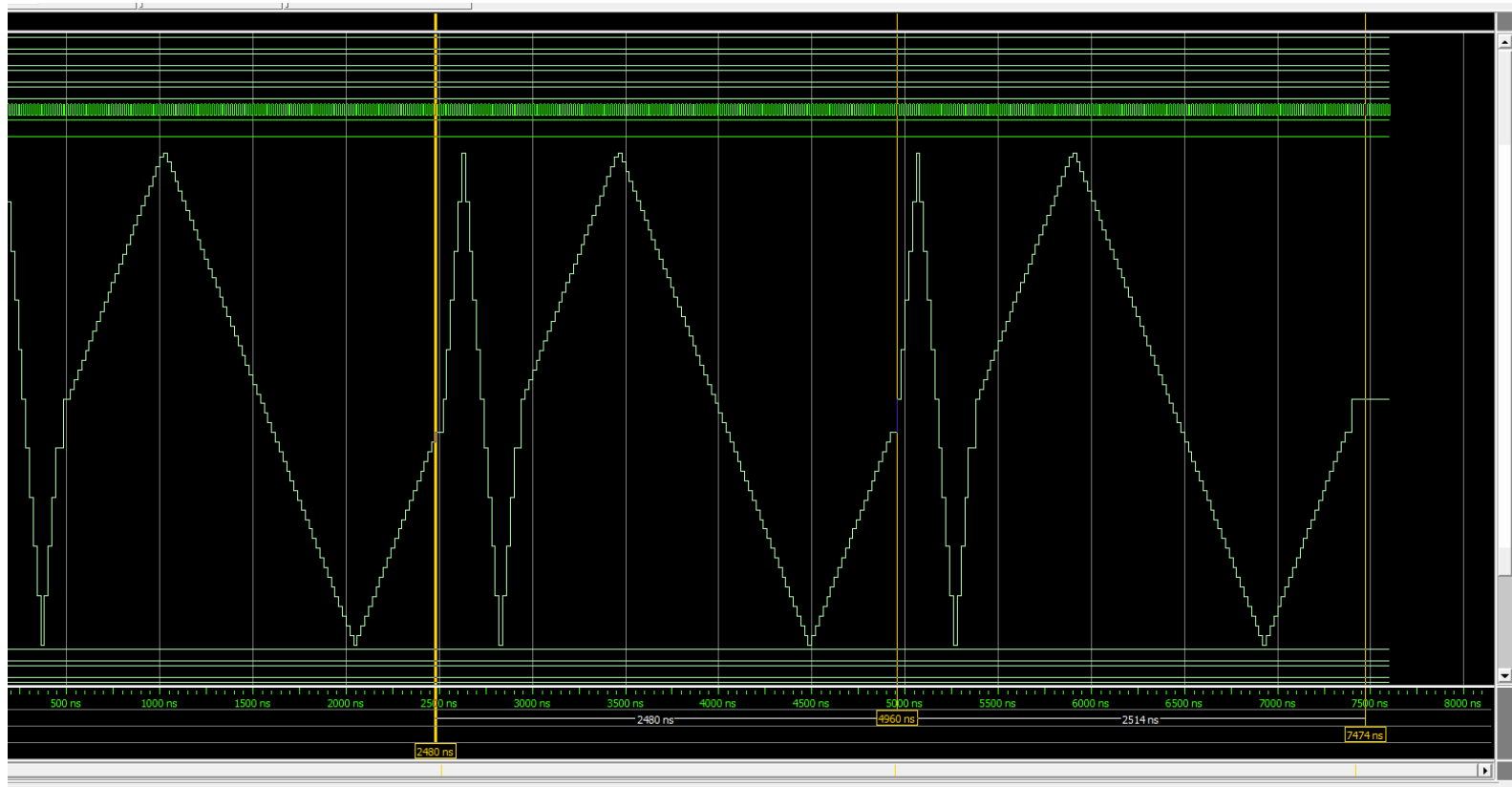
# Simulation of wave generator

Case (1) :  $f_1, f_2 < f_s$

$f_{\text{system}} = 100 \text{ MHz}$

-  $f_1 = 5 \text{ MHz}$  ,  $n_1 = 100/5 = 20$  ,  $y_1 = 51$

-  $f_2 = 1 \text{ MHz}$  ,  $n_2 = 100$  ,  $y_2 = 10$ .

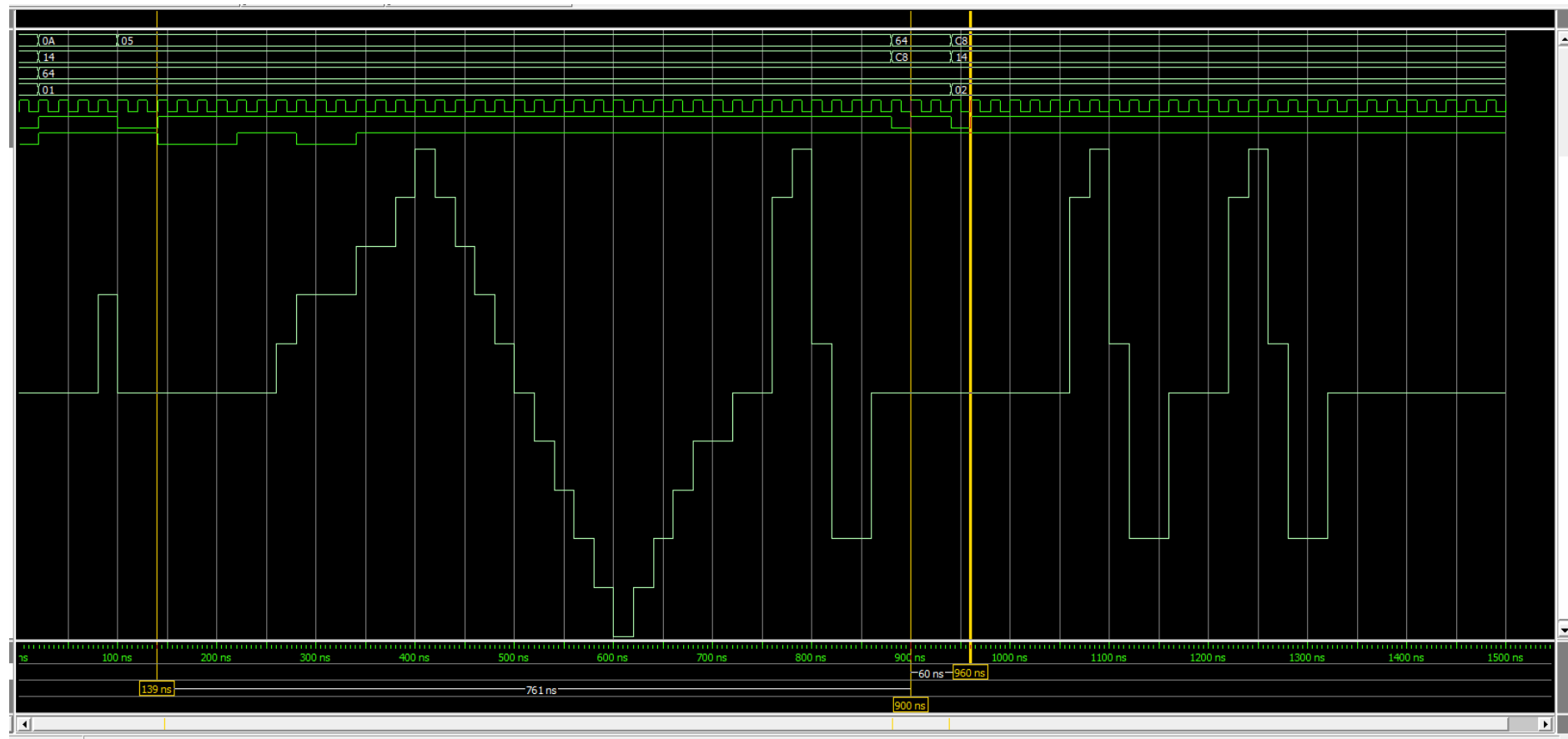




# Simulation of wave generator

Case (2) : test bench

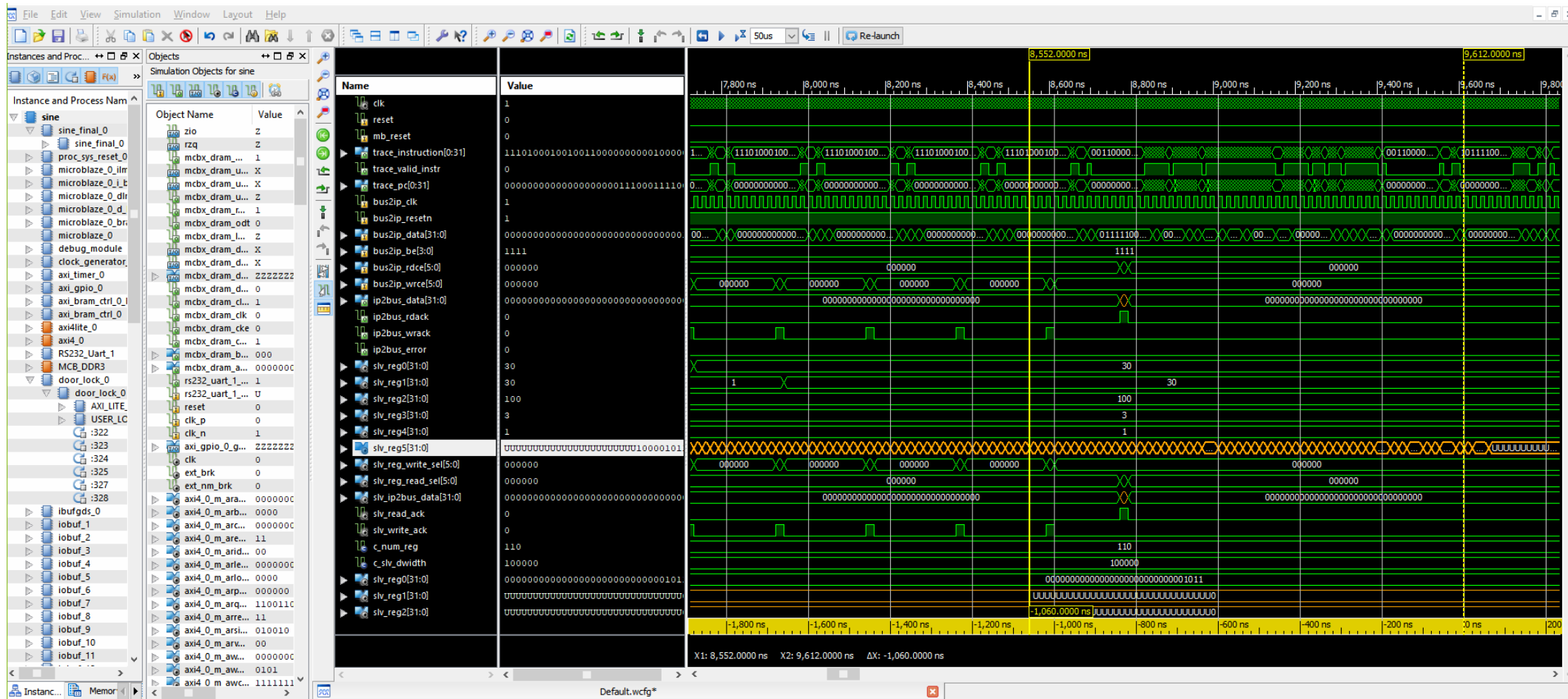
Different cases (regions)





# Simulation of wave generator

## Micro Blaze








# Reports of ISE

Device Utilization Summary					[+]
Slice Logic Utilization	Used	Available	Utilization	Note(s)	
Number of Slice Registers	148	54,576	1%		
Number used as Flip Flops	148				
Number used as Latches	0				
Number used as Latch-thrus	0				
Number used as AND/OR logics	0				
Number of Slice LUTs	949	27,288	3%		
Number used as logic	895	27,288	3%		
Number using O6 output only	696				
Number using O5 output only	68				
Number using O5 and O6	131				
Number used as ROM	0				
Number used as Memory	0	6,408	0%		
Number used exclusively as route-thrus	54				
Number with same-slice register load	0				
Number with same-slice carry load	54				
Number with other load	0				
Number of occupied Slices	308	6,822	4%		
Number of MUXCYs used	484	13,644	3%		
Number of LUT Flip Flop pairs used	952				
Number with an unused Flip Flop	804	952	84%		
Number with an unused LUT	3	952	1%		
Number of fully used LUT-FF pairs	145	952	15%		
Number of unique control sets	9				
Number of slice register sites lost to control set restrictions	52	54,576	1%		
Number of bonded IOBs	41	296	13%		
Number of RAMB16BWRs	0	116	0%		
Number of RAMB8BWRs	0	232	0%		
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%		
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%		
Number of BUFG/BUFGMUXs	1	16	6%		
Number used as BUFGs	1				



# Reports of ISE

							
	Met	Constraint	Check	Worst Case Slack	Best Case Achievable	Timing Errors	Timing Score
1	Yes	<a href="#">Autotimespec constraint for clock net clk BUFGP</a>	SETUP HOLD	 0.415ns	7.029ns	 0	 0

**THANK YOU**