CPS310 – COMPUTER ORGANIZATION II

LAB 1

ALU, REGISTER DESIGN

Submission instruction:

Labs will be done individually. Please complete and submit this lab on D2L by the submission deadline according to the details provided by your TA. Each student should submit a pdf file that includes all their written work and screenshots of their ALU. In addition to the pdf file, students should submit a copy of their Logisim file in the same submission. Please note that Lab 1 is for practice only and will be graded based on attendance and participation but not on design.

1. Design a 4-bit ALU that performs Arithmetic (add, subtraction), and Logic operations (AND, OR). The following control signals are to be considered:
    - A/S: add/subtract (0:add, 1:subtract)
    - A/O: AND/OR logic functions (0:AND, 1:OR)
    - R/W: read/write signal (0:read, 1:write)

2. Simulate your design.

Unit 1 - Design a 4-bit adder/subtractor that accepts two 4-bits numbers, A and B, and either add them up (A + B) or subtract them (A – B) depending on a control signal A/S (when the control signal is 0 perform ADD, otherwise if the signal is 1 then perform SUB). The result will be stored in C.

Unit 2 - Design a 4-bit AND/OR unit that accepts two 4-bits numbers, A and B, and either AND them or OR them depending on a control signal A/O (when the control signal is 0 perform AND, otherwise if the signal is 1 then perform OR – bitwise logical operation). The result will be stored in C.

Unit 3 - Design three 4-bit parallel registers to hold A, B, and C where C keeps the output of the ALU. The registers have a R/W control signal that indicates that they are being written to or read from.