EE2003:Computer Organization

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Question 10:

Plot the DTLB Miss Rate by varying the Virtual Memory size keeping the Physical Page size constant (at least 4 different sizes of page table). Also vary the number of levels of tables (at least 2 values including default). Analyze the result

Result :

The Miss Ratios I got for 3 levels of Tables are:

- 512 – Deadlock
- 1024 – 12.6144%
- 2048 – 12.6145%
- 4096 – 12.6192%

The Miss Ratios I got for 5 levels of Tables are:

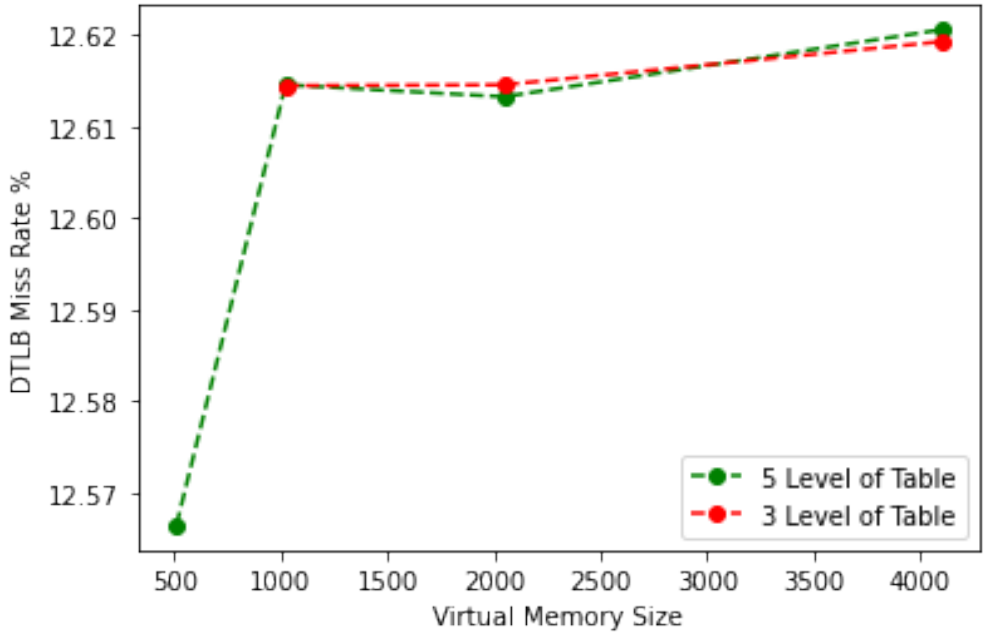
- 512 – 12.5665%
- 1024 – 12.6145%
- 2048 – 12.6132%
- 4096 – 12.6205%

The Miss Ratios I got for 7 levels of Tables are:

- 512 – 12.5665%
- 1024 – 12.6145%
- 2048 – Deadlock

The simulation results have been provided in the zip file.

The miss ratios can be visualised from the given plot below:



It means that changing the size of virtual memory won't product much effect after a point of time, i.e. after 1024 number of virtual pages it remains constant. This is the case for both levels.

Changing the level of Table produces slight effect of the miss ratios. Decreasing the levels increases the miss ratio first, then after a point of time it decreases.

My System's Cache Configuration:

```
Architecture:            x86_64
  CPU op-mode(s):        32-bit, 64-bit
  Address sizes:         39 bits physical, 48 bits virtual
  Byte Order:            Little Endian
CPU(s):                  4
  On-line CPU(s) list:   0-3
Vendor ID:               GenuineIntel
  Model name:            Intel(R) Core(TM) i5-10300H CPU @ 2.50GHz
    CPU family:          6
    Model:               165
    Thread(s) per core:  1
    Core(s) per socket:  4
    Socket(s):           1
    Stepping:            2
    BogoMIPS:            4991.98
    Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mc
                         a cmov pat pse36 clflush mmx fxsr sse sse2 ht syscall n
                         x rdtscp lm constant_tsc rep_good nopl xtopology nonsto
                         p_tsc cpuid tsc_known_freq pni pclmulqdq ssse3 cx16 pci
                         d sse4_1 sse4_2 x2apic movbe popcnt aes xsave avx rdran
                         d hypervisor lahf_lm abm 3dnowprefetch invpcid_single f
                         sgsbase bmi1 avx2 bmi2 invpcid rdseed clflushopt md_cle
                         ar flush_l1d arch_capabilities
Virtualization features:
  Hypervisor vendor:     KVM
  Virtualization type:   full
Caches (sum of all):
  L1d:                   128 KiB (4 instances)
  L1i:                   128 KiB (4 instances)
  L2:                    1 MiB (4 instances)
  L3:                    32 MiB (4 instances)
NUMA:
  NUMA node(s):          1
  NUMA node0 CPU(s):     0-3
Vulnerabilities:
  Gather data sampling:  Unknown: Dependent on hypervisor status
  Itlb multihit:         KVM: Mitigation: VMX unsupported
  L1tf:                  Not affected
  Mds:                   Not affected
  Meltdown:              Not affected
  Mmio stale data:       Vulnerable: Clear CPU buffers attempted, no microcode;
                         SMT Host state unknown
  Retbleed:              Vulnerable
  Spec rstack overflow:  Not affected
  Spec store bypass:     Vulnerable
  Spectre v1:            Mitigation; usercopy/swapgs barriers and __user pointer
                         sanitization
  Spectre v2:            Mitigation; Retpolines, STIBP disabled, RSB filling, PB
```

RSB-eIBRS Not affected
Srbds: Unknown: Dependent on hypervisor status
Tsx async abort: Not affected