Cache Simulation

In this assignment, you will be using the ChampSim simulator to determine the best configuration of cache by modifying the mentioned parameters. The trace you will be using is allotted to you. **DO NOT** modify the source code of the ChampSim or other configuration parameters unless specified while doing the assignment. You are, however, encouraged to look into the source code and understand how a CPU is modeled using C++.

For all the questions, take the number of warmup instructions to be 20 million and number of simulation instructions to be 100 million. For each question begin by specifying the relevant cache parameters and then the parameter which is modified for each plot. If the time taken is very large (more than 3 hrs) then try using a lesser number of (warmup+simulation) instructions. Reducing it excessively might result in transient effects while analyzing performance.

Cache size, Cache Replacement Policies

1) Fix L1 and L2 Caches to be Direct Mapped and the **size to be the same as default size**. Plot the Miss Rate for L1d (Cache Miss Rate) and IPC for at least 2 different Cache Replacement Policies by varying the cache size for **L1d** (at least 4 reasonable sizes).
   Bonus points for using more advanced Cache Replacement Policies (like MockingJay).

2) Fix L1 and L2 Caches to be Direct Mapped and the **size to be the same as default size**. Plot the Miss Rate for L2 and IPC for at least 2 different Cache Replacement Policies by varying the cache size for **L2** (at least 4 reasonable sizes).
   Bonus points for using more advanced Cache Replacement Policies (like MockingJay).

3) Fix L1 and L2 Caches to be Direct Mapped and the **size to be the same as default size**. Plot the Miss Rate for L3 and IPC for any 1 Cache Replacement Policies by varying the cache size for **L3** by varying the ways and sets (at least 8 reasonable variations).
   Bonus points for using more advanced Cache Replacement Policies (like MockingJay).

4) Fix all levels of Cache to be Fully Associative and the **size to be the same as default size**. Plot the Miss Rate for L1d and IPC for at least 2 different Cache Replacement Policies by varying the cache size for **L1d** (at least 4 reasonable sizes).
   Bonus points for using more advanced Cache Replacement Policies (like MockingJay).

5) Fix all levels of Cache to be Fully Associative and the **size to be the same as default size**. Plot the Miss Rate for L2 and IPC for at least 2 different Cache Replacement Policies by varying the cache size for **L2** (at least 4 reasonable sizes).
   Bonus points for using more advanced Cache Replacement Policies (like MockingJay).

6) Fix all levels of Cache to be Fully Associative and the **size to be the same as default size**. Plot the Miss Rate for L3 and IPC for at least 2 different Cache Replacement Policies by varying the cache size for **L3** (at least 4 reasonable sizes).
Bonus points for using more advanced Cache Replacement Policies (like MockingJay).

Virtual Memory, Physical Memory, TLB

7) Plot the DTLB Miss Rate by varying the Physical Page size keeping the Virtual Memory size constant (at least 4 different sizes of rows). Also vary the number of levels of tables (at least 2 values including default). Analyze the result.

8) Plot the DTLB Miss Rate by varying the Physical Page size keeping the Virtual Memory size constant (at least 4 different sizes of columns). Also vary the number of levels of tables (at least 2 values including default). Analyze the result.

9) Plot the DTLB Miss Rate by varying the Physical Page size keeping the Virtual Memory size constant (at least 4 different numbers of ranks). Also vary the number of levels of tables (at least 2 values including default). Analyze the result.

10) Plot the DTLB Miss Rate by varying the Virtual Memory size keeping the Physical Page size constant (at least 4 different sizes of page table). Also vary the number of levels of tables (at least 2 values including default). Analyze the result.

11) Plot the DTLB Miss Rate by varying the TLB size by varying the number of sets (8 combinations). Analyze the result.

12) Plot the DTLB Miss Rate by varying the TLB size by varying the number of ways (8 combinations). Analyze the result.

Cache size, Cache latency

13) Assuming the latency is proportional to the size of the cache, identify the best cache sizes suitable for your trace. For finding the proportionality constant use the default size and latency for each level of cache. **NOTE** that the latency parameter needs to be changed to enable appropriate simulation. Both ways and sets can be changed (details of the procedure followed needs to be mentioned briefly). Use plots/tables to justify your solution (minimum of 8 different configurations).
Eg: If default size is 10 bytes and default latency is 10, then if the new size is 20 bytes then the latency needs to be modified to 20.

Prefetcher

14) Plot the Miss Rates for L1d, L2C, L3 and IPC for different prefetch policies (at least 5 different ones). *Bonus points for using more advanced prefetch policies!*

Cache associativity

15) Analyze how the Average Miss Latency for the CPU changes with varying associativity at L2 and LLC (at least 4 different associativity for each).

16) Analyze how the Average Miss Latency for the CPU changes with varying associativity at L1i and L1d (at least 4 different associativity for each).

Multi tasking - For the following questions consider a system with shared L2 and L3 and private L1d, L1i

17) Plot the Miss Rate for L2 for any 2 replacement policies and 4-way associativity for L2 while varying the number of cores (1, 2, 4, 8).
Bonus points for using more advanced Cache Replacement Policies (like MockingJay).

18) Plot the Miss Rate for L2 for any 2 replacement policies and 16-way associativity for L2 while varying the number of cores (1, 2, 4, 8).
Bonus points for using more advanced Cache Replacement Policies (like MockingJay).

19) Plot the Miss Rate for L3 for any 2 replacement policies and 4-way associativity for L3 while varying the number of cores (1, 2, 4, 8).
Bonus points for using more advanced Cache Replacement Policies (like MockingJay).

20) Plot the Miss Rate for L3 for any 2 replacement policies and 16-way associativity for L3 while varying the number of cores (1, 2, 4, 8).
Bonus points for using more advanced Cache Replacement Policies (like MockingJay).

21) Plot the Average Miss Latency for the CPU for single and 2-core and vary the associativity for L1d, L2, L3 cache levels. Use 1-way and 8-way for associativity. Minimum 8 different configurations need to be considered.
Bonus points for using more advanced Cache Replacement Policies (like MockingJay).