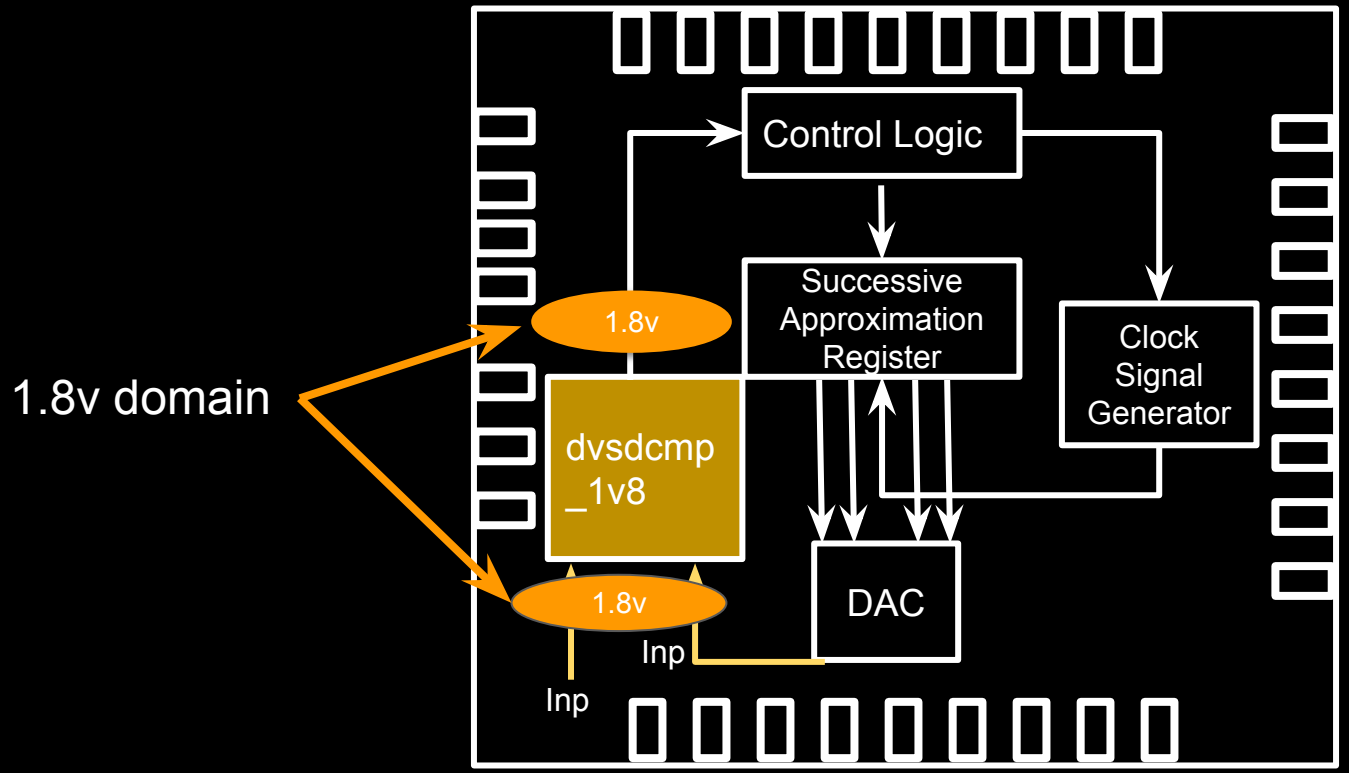
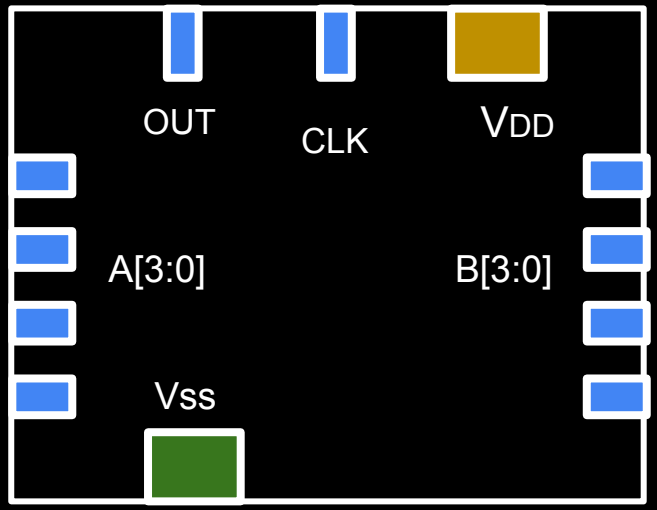
4 bit High Speed Domino Logic Footed Comparator (dvsdcmp_1v8)

- Specs released under Apache License 2.0
- Please contact Kunal at kunalpghosh@gmail.com in case of any doubts

Application Note for comparator (dvsdcmp_1v8)



dvsdcmp_1v8 preferred dimensions, pin locations and metal layers

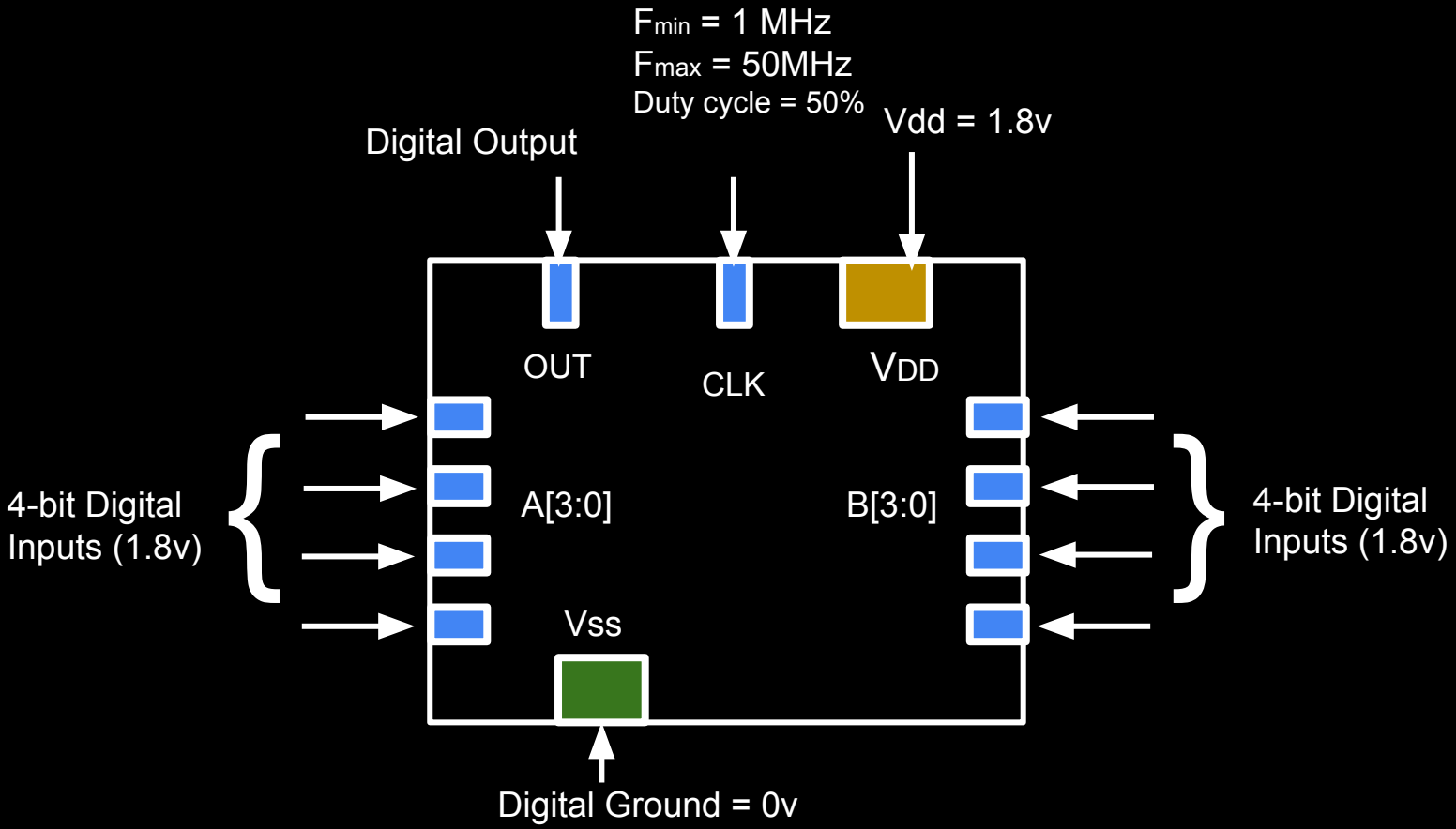


Signal Pins - 0.28um x 0.28um (metal 1)

Vss - 3um x 0.28um (metal 3)

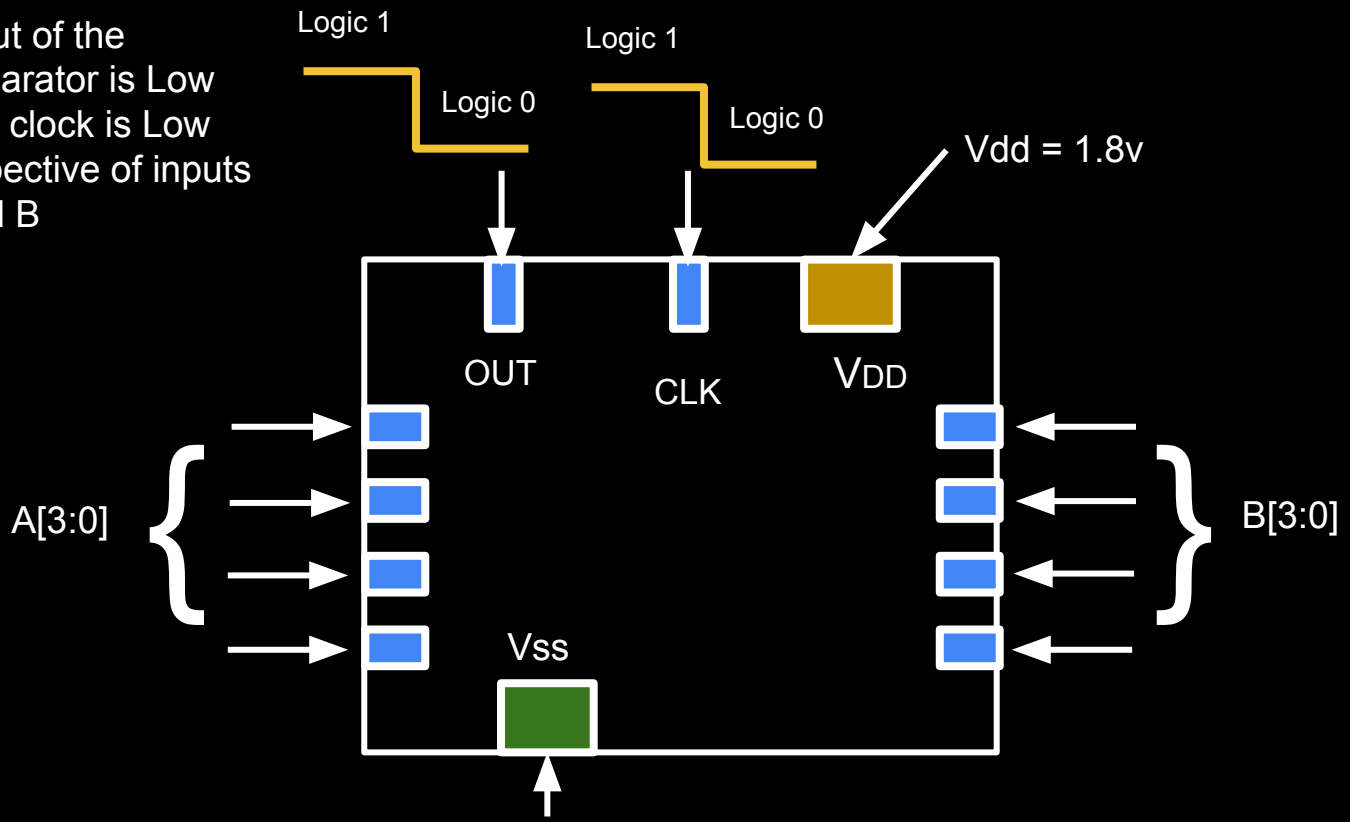
Vdd - 3um x 0.28um (metal 2)

dvsdcmp_1v8 operating modes



dvsdcmp_1v8 operating modes

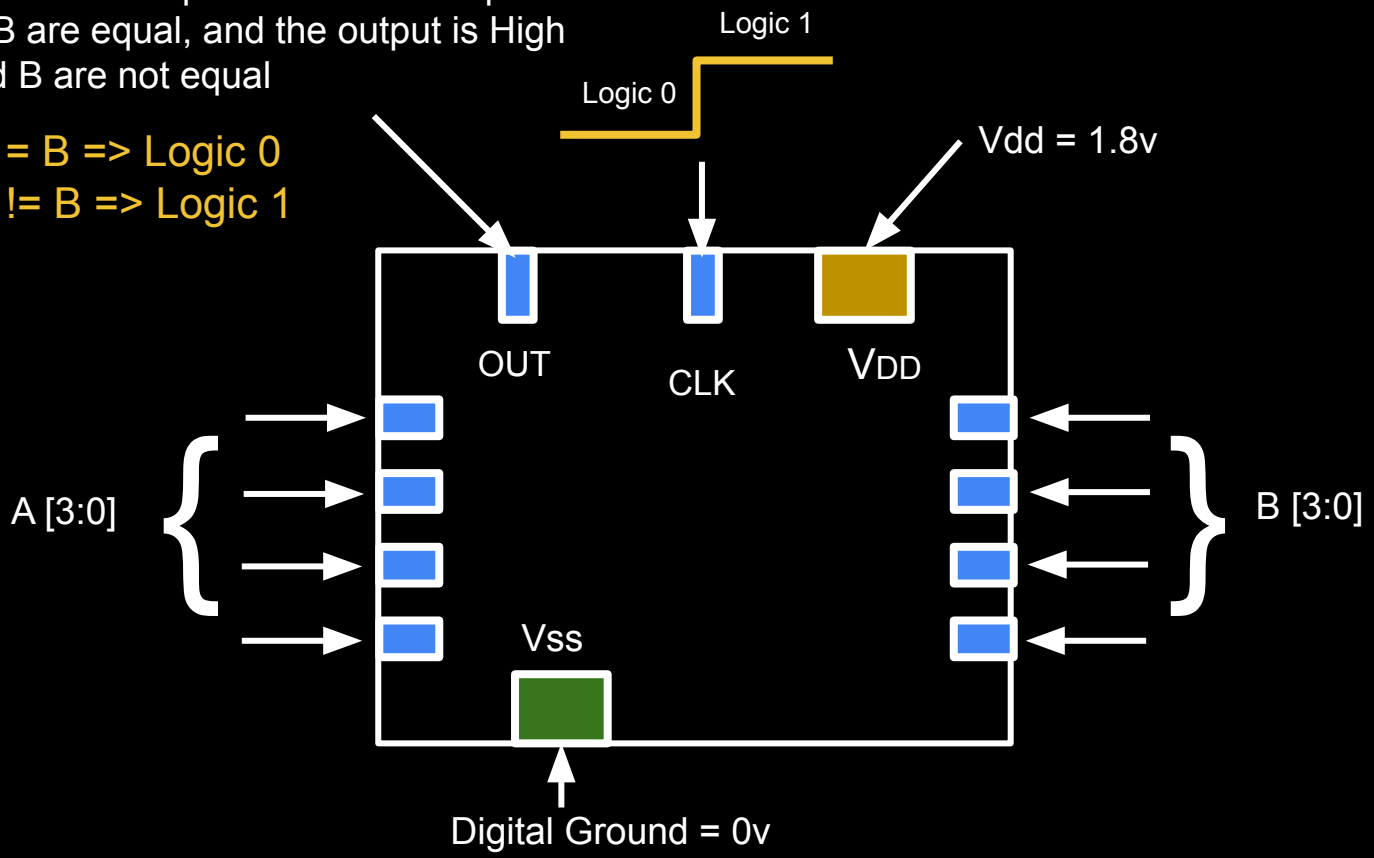
Output of the comparator is Low when clock is Low irrespective of inputs A and B



dvsdcmp_1v8 operating modes

Output of the comparator is Low if inputs A and B are equal, and the output is High if A and B are not equal

If A = B => Logic 0
If A != B => Logic 1



dvsdcmp_1v8 plots and values needed

1) Clock vs Time at F_{clk} = 5 MHz and V_{dd} = 1.8V
2) A [3:0] vs Time at F_{clk} = 5 MHz
3) B [3:0] vs Time at F_{clk} = 5 MHz
4) Out vs Time at F_{clk} = 5 MHz