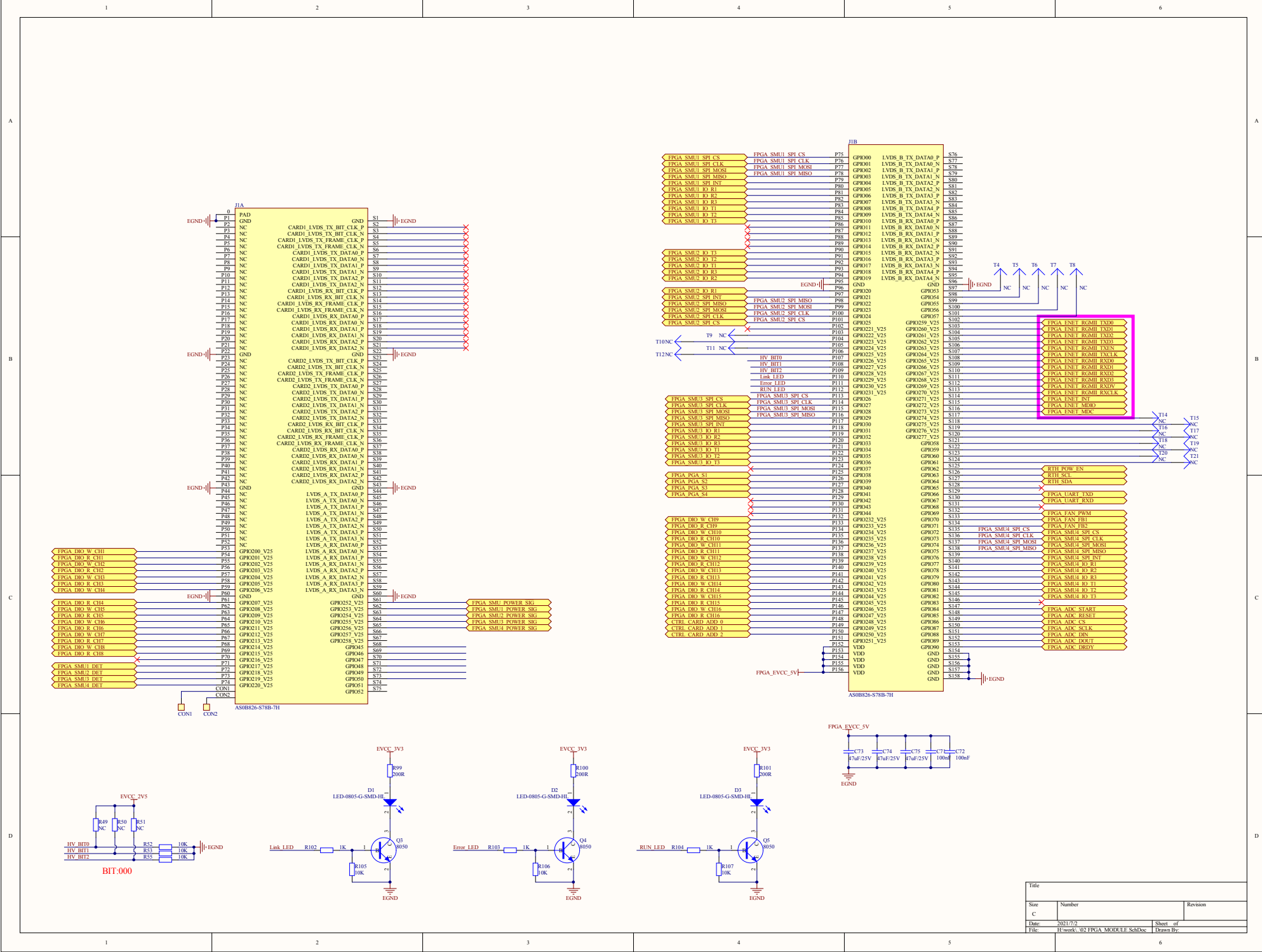
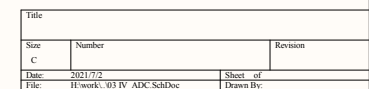


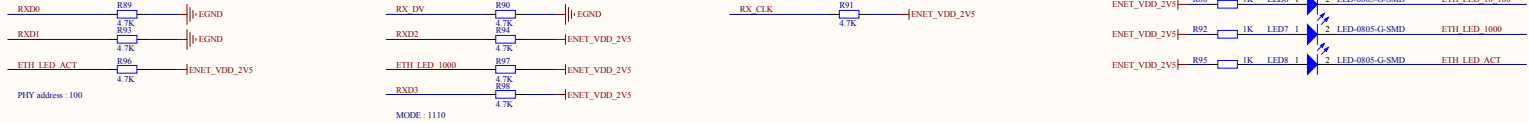
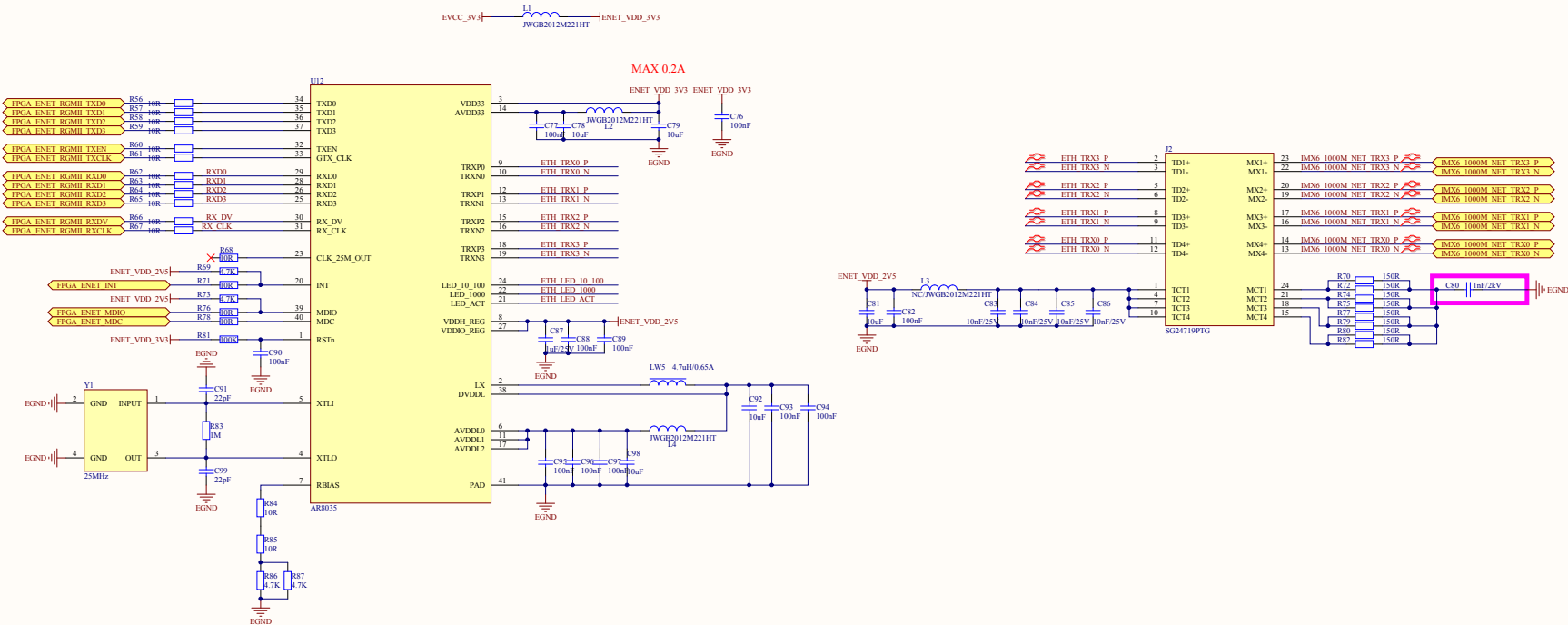
Title		
Size	Number	Revision
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Date:	2021/7/3	Sheet 1 of 1
File:	U-work\01 POWER_SchDoc	Drawn By:



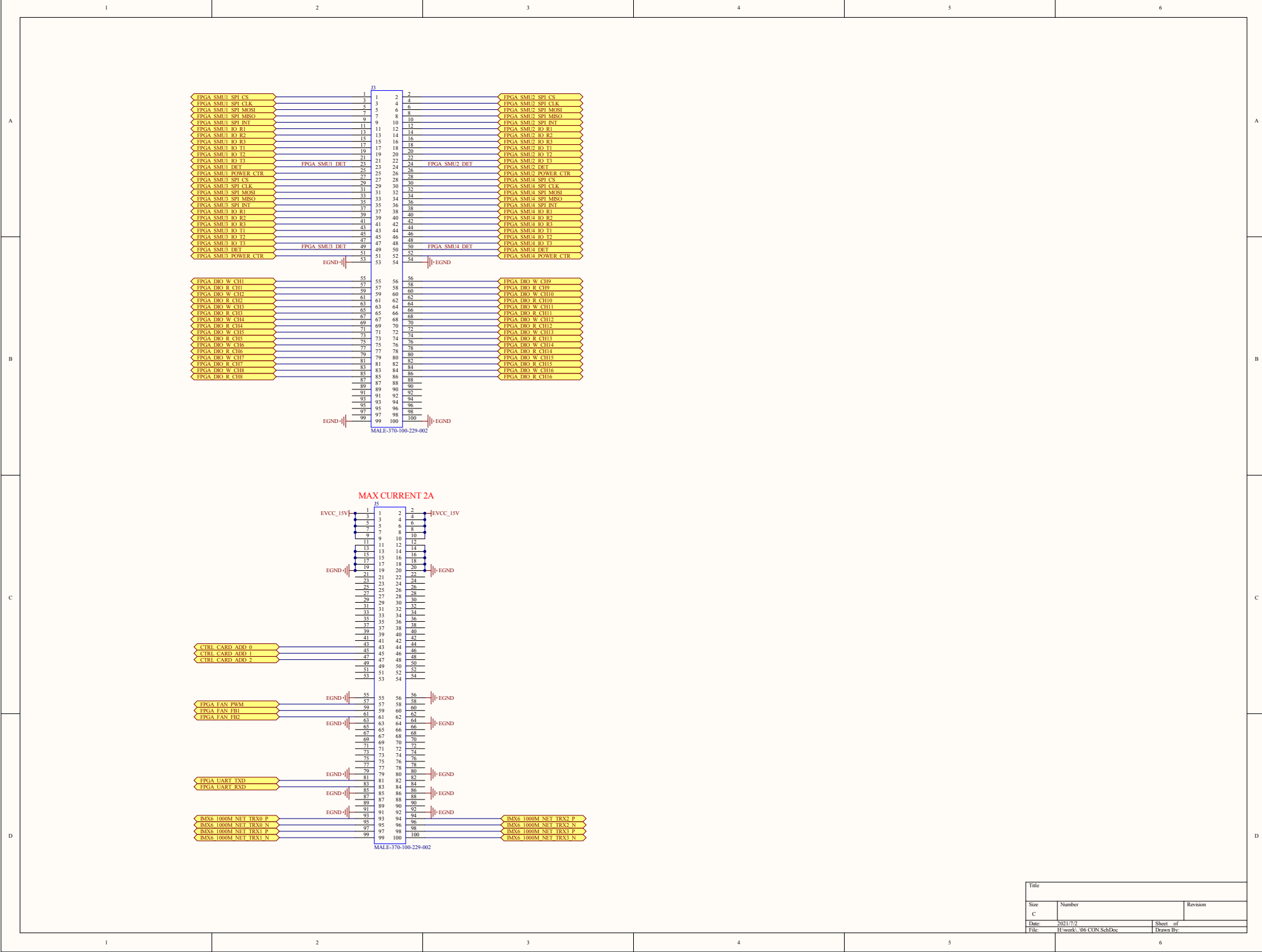
Title		
Size	Number	Revision
C		
Date:	2021/7/2	Sheet: 6 of 6
File:	U-work_02 FPGA MODULE SchDoc	Drawn by







Title		
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Date:	2021/7/2	Sheet: 1 of 1
File:	U-work\05 FPGA_ENET_SchDoc	Drawn By:



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Size	Number	Revision
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Date:	2021/7/2	Sheet of
File:	U-work\06 CON SchDoc	Drawn By

	1	2	3	4	5	6	7	8
A								
B								
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D								
	1	2	3	4	5	6	7	8

Title		
Size	Number	Revision
A3		
Date:	2021/7/2	Sheet of
File:	H:\work\...\TOP.SchDoc	Drawn By: