Q1

The following is a simple function that divides the input by 73 and returns the result:

```
int div2(int num) {

    return num / 73;

}
```

Here is the compiled assembly for RISC-V using GCC:
(https://godbolt.org/z/1Ynx94PjzLinks to an external site.)

```
div73(int):
        li      a5,-529514496
        addi    a5,a5,-2019
        mulh    a5,a0,a5
        srai    a4,a0,31
        add     a5,a5,a0
        srai    a5,a5,6
        sub     a0,a5,a4
        ret
```

This version contains 7 instructions.
Alternatively, the same function could be implemented in only 3 instructions:

```
div73(int):
        li      a1,73
        div     a0,a0,a1
        ret
```

In the 7-instruction version, there is no explicit division instruction. Instead, it uses shifts, additions, and multiplications to perform the division. Interestingly, the number "73" is not directly present in this version either.
Why does the compiler generate the 7-instruction version instead of the simpler 3-instruction version? Is using fewer instructions always preferable?
Discuss this with the concepts covered in Chapter 1.

Q2

A common pitfall is to utilize a subset of the performance equation as a performance metric. To illustrate this, consider the following two processors. P1 has a clock rate of 4.5 GHz, average CPI of 0.9, and requires the execution of 5.0E9 instructions. P2 has a clock rate of 3 GHz, an average CPI of 0.7, and requires the execution of 1.0E9 instructions.

a. One usual fallacy is to consider the computer with the largest clock rate as having the highest performance. Check if this is true for P1 and P2.

b. Another fallacy is to consider that the processor executing the largest number of instructions will need a larger CPU time.

Considering that processor P1 is executing a sequence of 1.0E9 instructions and that the CPI of processors P1 and P2 do not change, determine the number of instructions that P2 can execute in the same time that P1 needs to execute 1.0E9 instructions.

c. A common fallacy is to use MIPS (millions of instructions per second) to compare the performance of two different processors, and consider that the processor with the largest MIPS has the largest performance. Check if this is true for P1 and P2.

Q3

Assume a program requires the execution of 50×10^6 FP instructions, 110×10^6 INT instructions, 120×10^6 L/S instructions, and 16×10^6 branch instructions. The CPI for each type of instruction is 1, 1, 4, and 2, respectively. Assume that the processor has a 2 GHz clock rate.

a. What's the execution time of this program?

b. What is the average CPI when running this program?

c. By how much must we improve the CPI of FP instructions if we want the program to run two times faster?

d. What kinds of instruction takes up the execution time the most? by how much percentage? (What's the performance bottleneck?)

Q4

A color display uses 8 bits per pixel for each of the primary colors: red, green, and blue. The frame resolution is 1280 × 1024 pixels.

a. If the frame buffer needs to store 3 frames simultaneously, what is the minimum size of the frame buffer?

b. Given a 7 Gbps network, what is the maximum number of frames per second that can be transmitted?

Q5

Clock rates, Cycles Per Instruction (CPI), and instruction counts are factors that influence performance.

a. How do algorithms influence Cycles Per Instruction (CPI)? Provide an example to support your explanation.

b. List and explain two additional factors that impact Cycles Per Instruction (CPI).

c. Identify two factors that affect instruction counts, even when the same algorithm is used. Explain why these factors have an impact.

Q6

Let's compare Apple's M2 and M3 chips. Their specifications are as follows:

	M2	M3
Fabrication Technology	5 nm	3 nm
Transistor Count	20 billion	25 billion
(max) CPU Clock Rate	3.49 GHz	4.05 GHz
ISA	ARMv8.6	ARMv8.6

To evaluate their performance, we often run them through benchmarks. For instance, using the GeekbenchLinks to an external site. benchmark, we compare two MacBook Pro models—one with the M2 chip and the other with the M3 chip. Their single-core performance scores are 2614 and 3090, respectively.

a. Based on the hardware specifications above, please explain what contributes to this performance improvement.

b. Which chip is likely to be more energy-efficient? Provide reasoning based on the given data.

c. Given that both processors use the same ISA (ARMv8.6), does this mean their average CPI (Cycles Per Instruction) will be identical? Why or why not?

For detailed information, please refer to: M2 MacBook ProLinks to an external site., M3 MacBook ProLinks to an external site.