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National Taiwan University of Science and Technology

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Design and development practice of power electronic products

-Week 5

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Course content

- Principle of switching converter …1 week
- Understanding of components, materials and loss …2 weeks
- *Operation principle and application scope of common circuit architecture …2 weeks*
- Small signal model and stability analysis …3 weeks
- Basic control methods …1 week
- The stability of the cascade system …1 week
- Introduction and design of EMI conducted noise sources, coupling paths, and non-ideal filters …1 week

Course outline – Week 5

- **Introduction of Zero Voltage Switching / Zero Current Switching technology**
  - Review the switching characteristics and the reasons for adopting ZVS or ZCS
  - The basic principle to realize ZVS
- **Common methods to implement ZVS**
  - Triangular Current Mode, TCM
  - Zero Voltage Transition, ZVT
  - Quasi-Resonant Converter, QRC
  - Active-Clamp
  - Resonant Converter
  - Dual Active Bridge, DAB
  - Phase-Shift Full Bridge, PSFB

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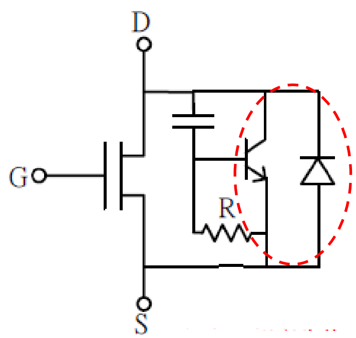
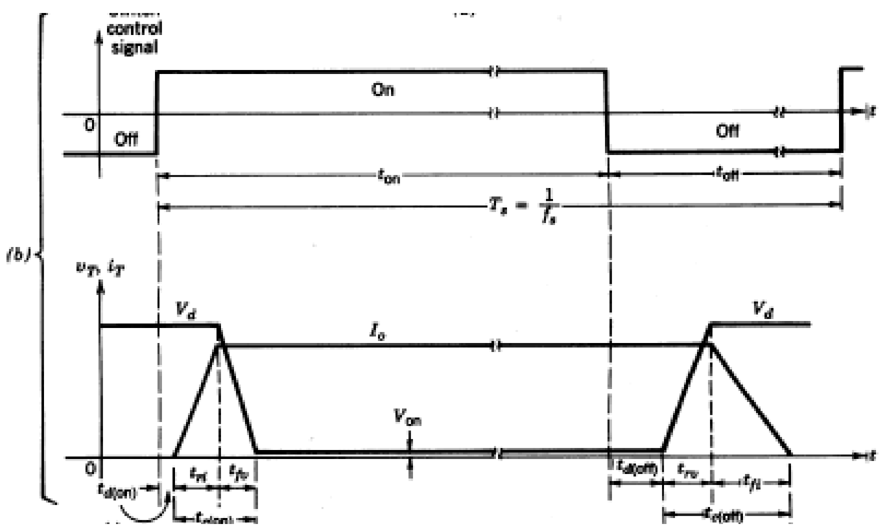
Review the switching characteristics and the reasons for adopting ZVS or ZCS

MOSFET (ZVS)





https://www.st.com/resource/en/application_note/dm00207043-half-bridge-resonant-llc-converters-and-primary-side-mosfet-selection-stmicroelectronics.pdf

IGBT (ZCS)

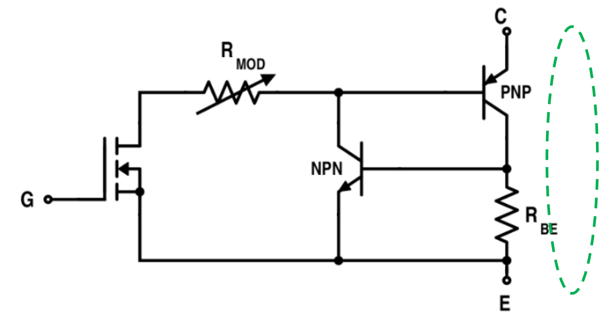
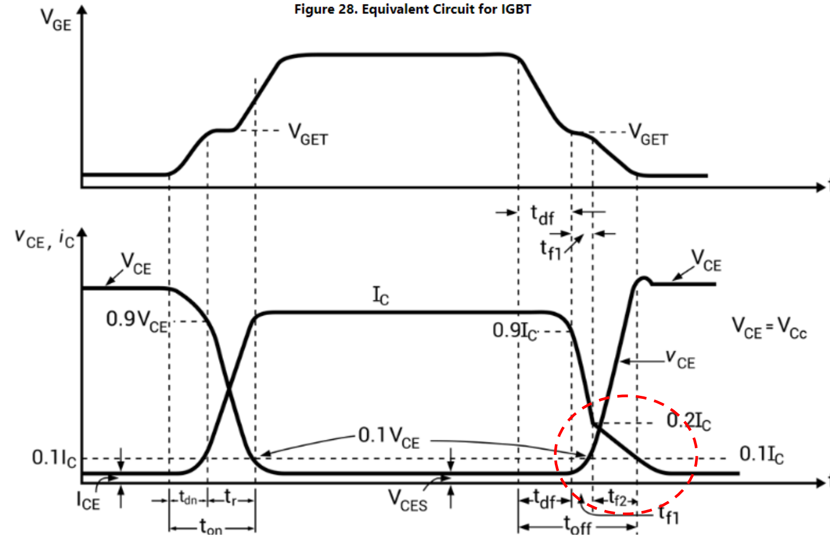
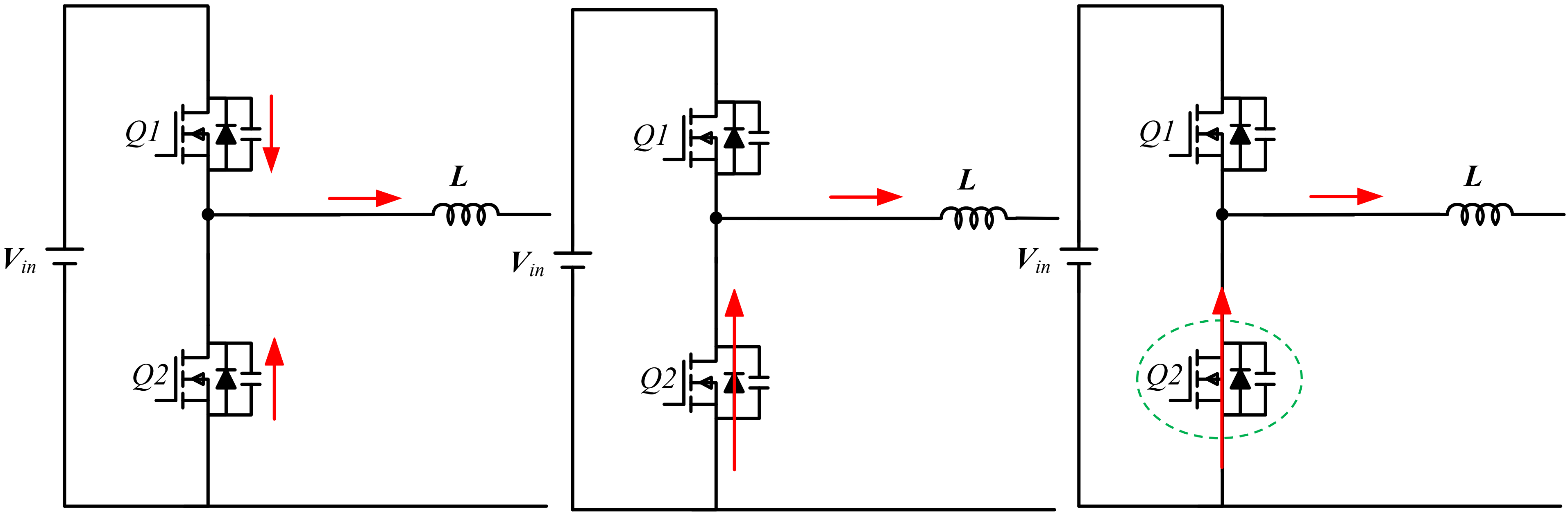


Figure 28. Equivalent Circuit for IGBT



Trivedi, M., & Shenai, K. (1999). *Internal dynamics of IGBT under zero-voltage and zero-current switching conditions. IEEE Transactions on Electron Devices, 46(6), 1274–1282.* doi:10.1109/16.766898

The basic principle to realize ZVS



- Create a current to turn on the body diode in the switch dead zone, and then the switch is turned on
- Whether ZVS can be achieved depends on whether the discharge can be completed during the dead time
- Saving switching loss and turns on driver loss, but still have turns off loss

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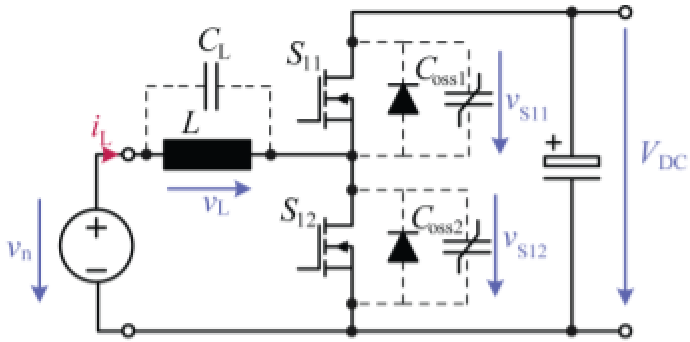
Triangular Current Mode, TCM (Choose TCM-Boost for example)

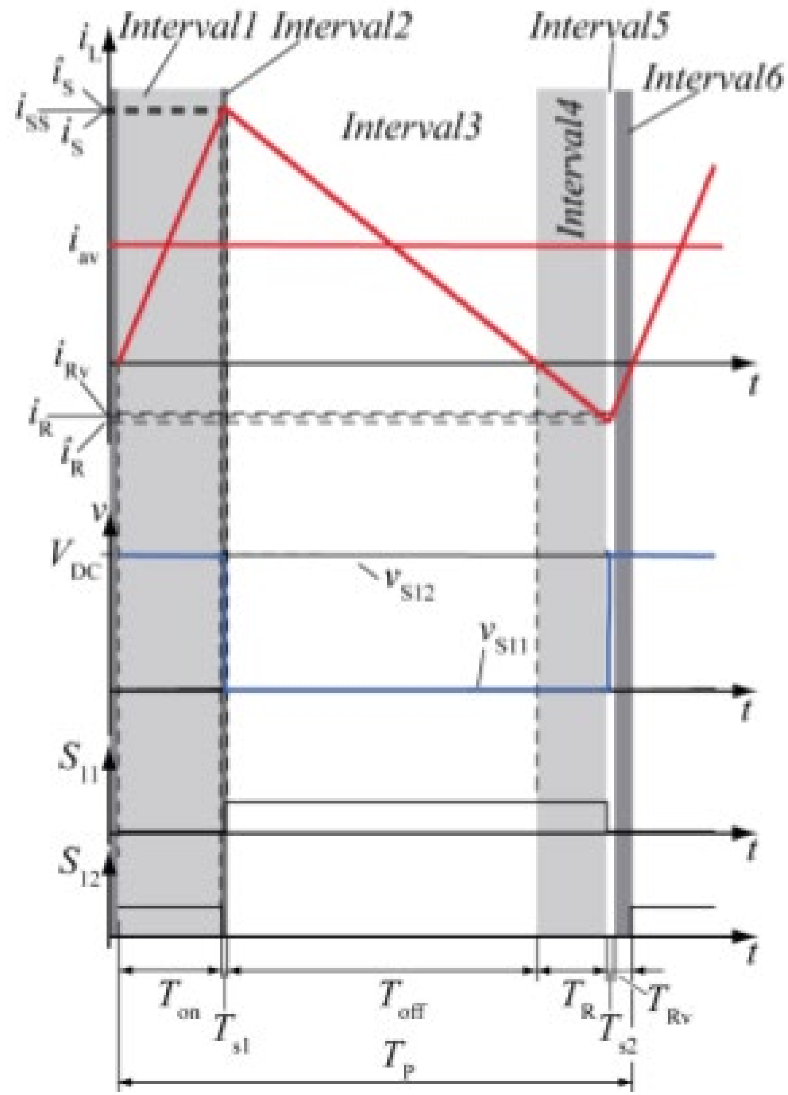


Advantage

1. No additional switches are required. ZVS can be achieved by controlling complementary switches.

Shortcoming

1. The negative current of the switch must reach a certain level to complete the zero voltage switching.
2. If entirely complementary switching control is adopted, although converter can adopt constant switching frequency operation, it will increase the circulating current loss of the switch.
3. If the lowest negative current control is adopted, although the circulating current loss is reduced, the switching frequency must increase under light load conditions, and the switching loss will increase.



[Ref]: C. Marxgut, J. Biela and J. W. Kolar, "Interleaved Triangular Current Mode (TCM) resonant transition, single phase PFC rectifier with high efficiency and high power density," The 2010 International Power Electronics Conference - ECCE ASIA -, 2010, pp. 1725-1732, doi: 10.1109/IPEC.2010.5542048.

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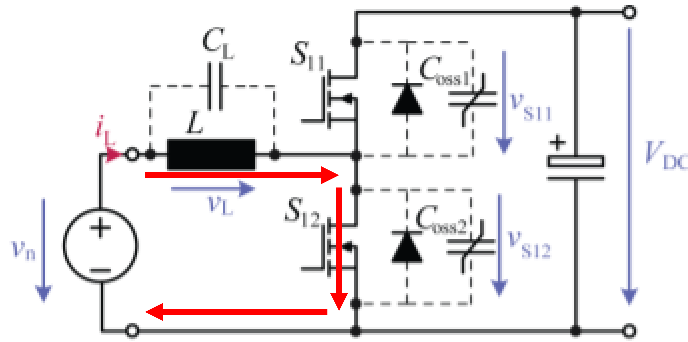
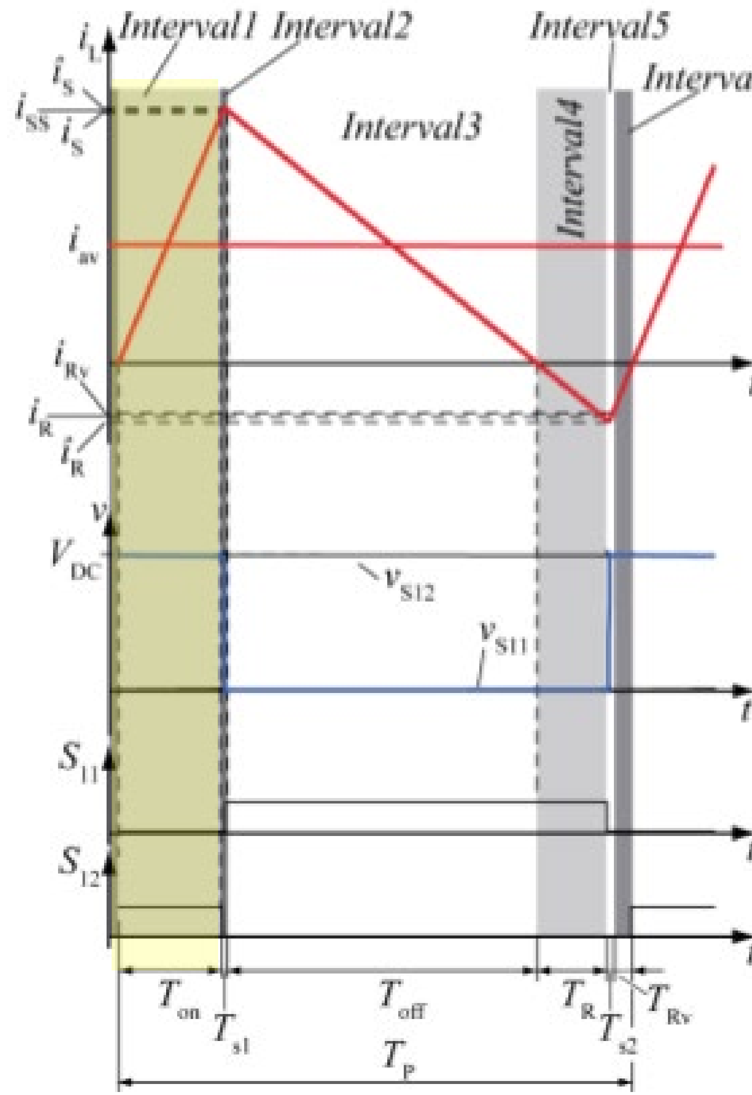
TCM-Boost – Interval 1



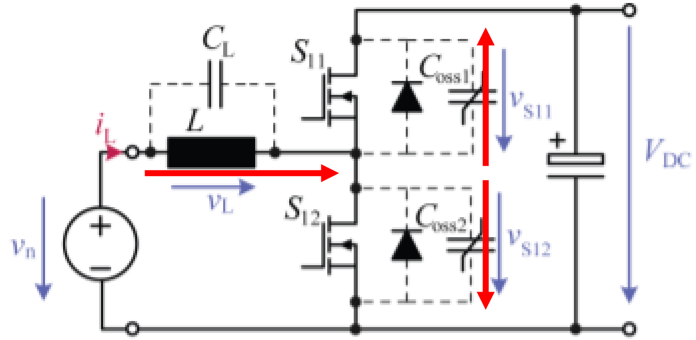


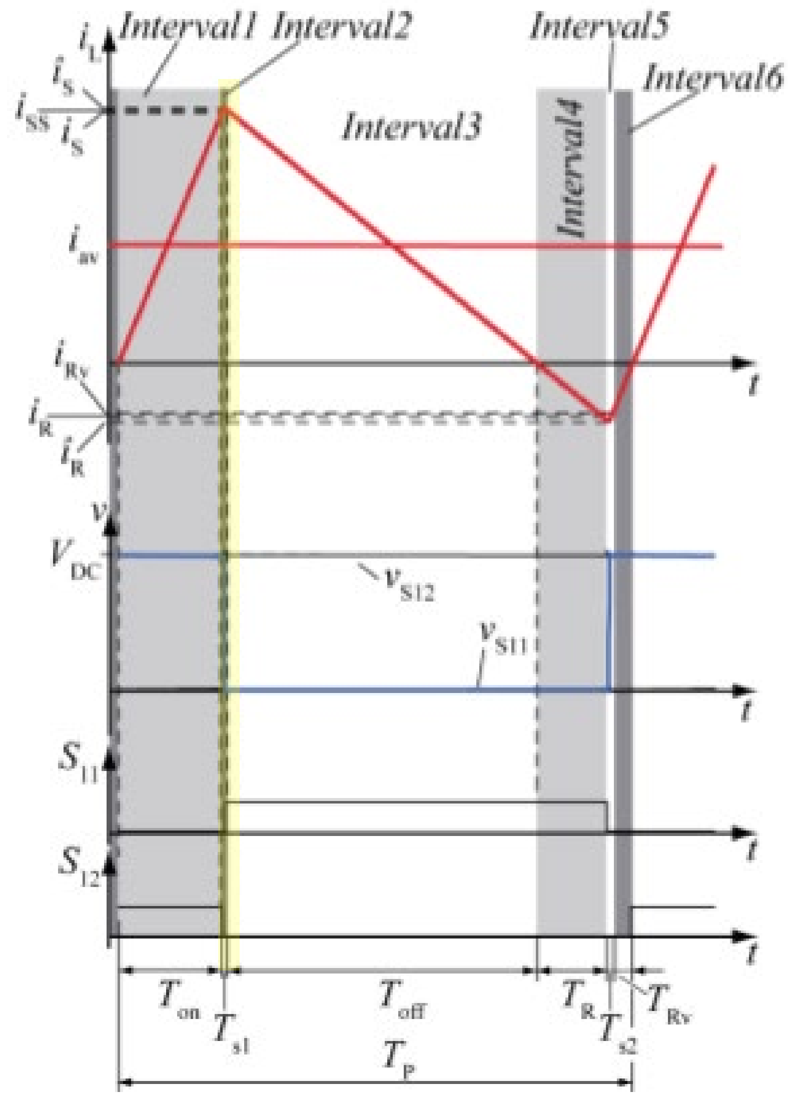
Interval 1

1. Switch S12 ON, $i_L>0$
2. $v_L=v_n$, i_L increase linearly

[Ref]: C. Marxgut, J. Biela and J. W. Kolar, "Interleaved Triangular Current Mode (TCM) resonant transition, single phase PFC rectifier with high efficiency and high power density," The 2010 International Power Electronics Conference - ECCE ASIA -, 2010, pp. 1725-1732, doi: 10.1109/IPEC.2010.5542048.

TCM-Boost – Interval 2



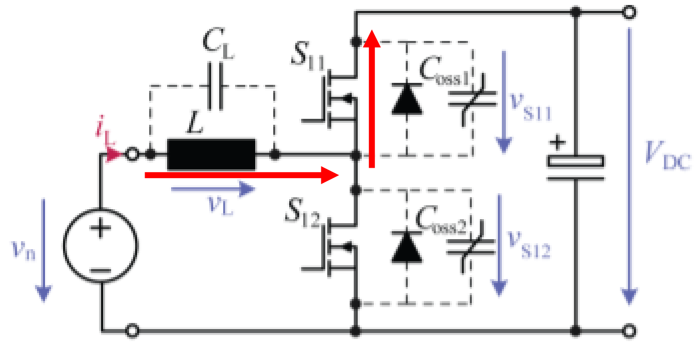


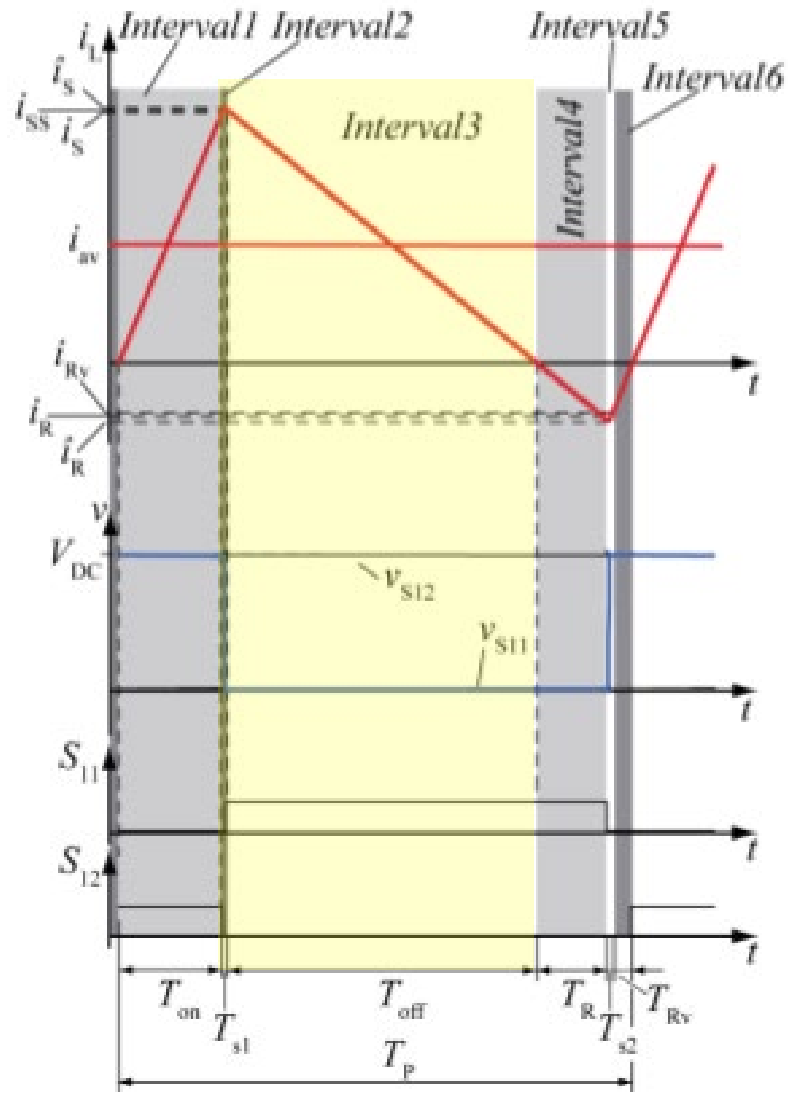
Interval 2

1. Dead time interval, i_L>0, charge Coss2 and discharge Coss1
2. S11's body diode conduct finally

[Ref]: C. Marxgut, J. Biela and J. W. Kolar, "Interleaved Triangular Current Mode (TCM) resonant transition, single phase PFC rectifier with high efficiency and high power density," The 2010 International Power Electronics Conference - ECCE ASIA -, 2010, pp. 1725-1732, doi: 10.1109/IPEC.2010.5542048.

TCM-Boost – Interval 3



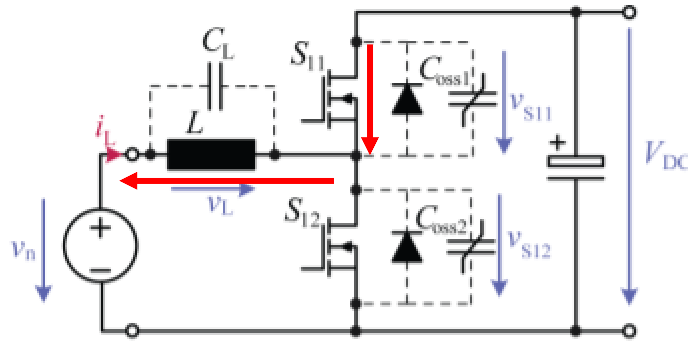


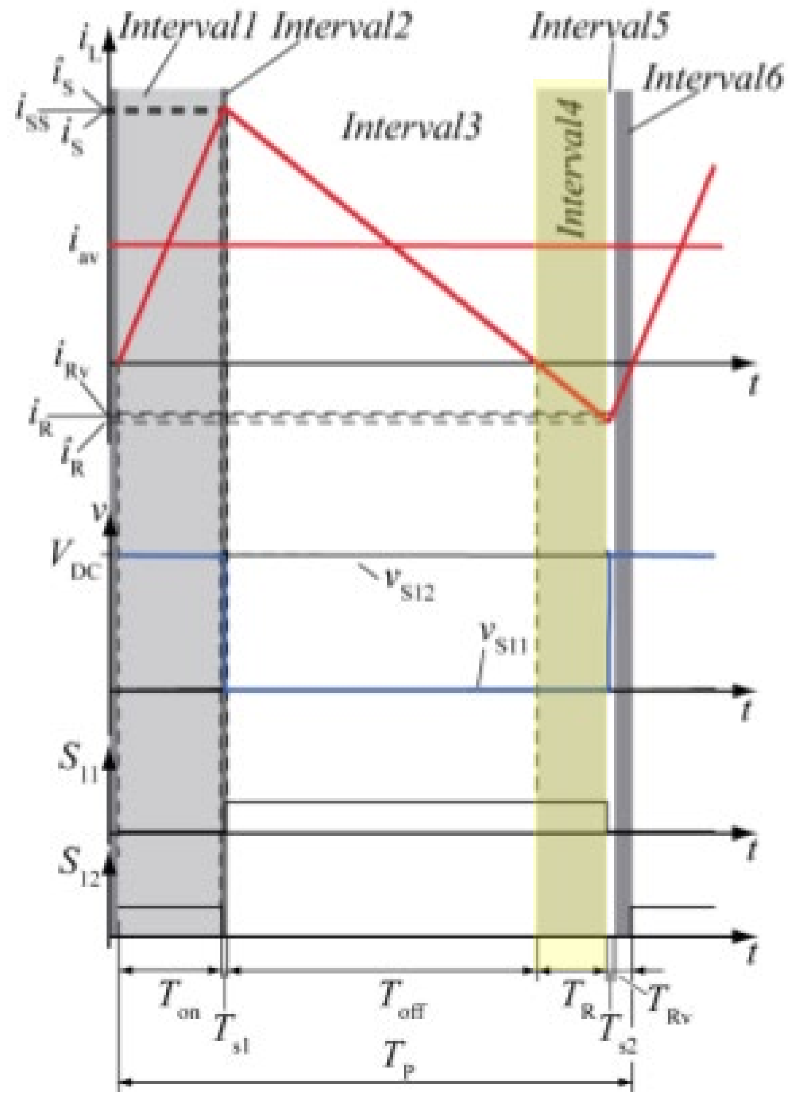
Interval 3

1. S11 turns on with ZVS
2. i_L decrease linearly with $v_L=V_{DC}-V_n$

[Ref]: C. Marxgut, J. Biela and J. W. Kolar, "Interleaved Triangular Current Mode (TCM) resonant transition, single phase PFC rectifier with high efficiency and high power density," The 2010 International Power Electronics Conference - ECCE ASIA -, 2010, pp. 1725-1732, doi: 10.1109/IPEC.2010.5542048.

TCM-Boost – Interval 4



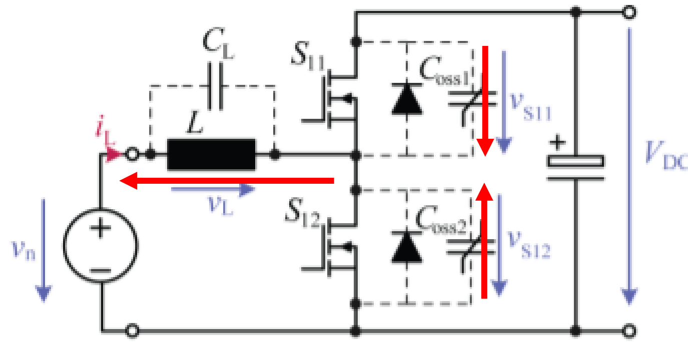


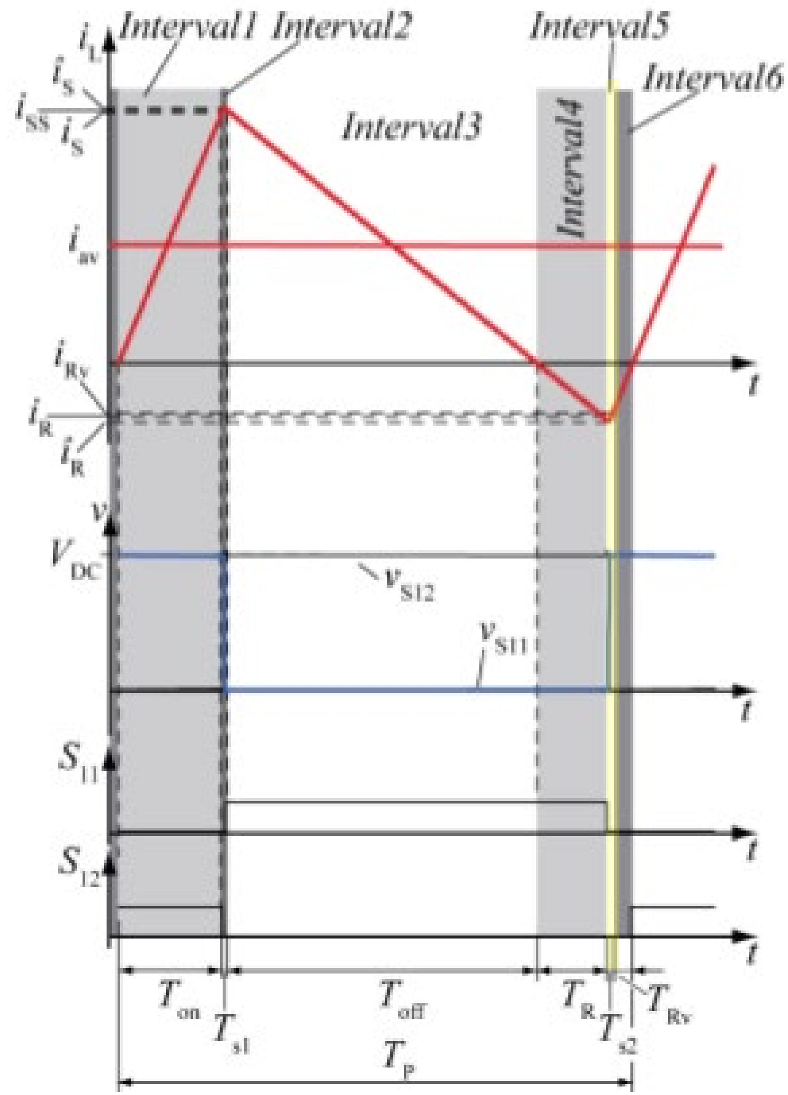
Interval 4

1. i_L decrease linearly with v_L=V_{DC}-V_n
2. iL<0 in interval 4

[Ref]: C. Marxgut, J. Biela and J. W. Kolar, "Interleaved Triangular Current Mode (TCM) resonant transition, single phase PFC rectifier with high efficiency and high power density," The 2010 International Power Electronics Conference - ECCE ASIA -, 2010, pp. 1725-1732, doi: 10.1109/IPEC.2010.5542048.

TCM-Boost – Interval 5



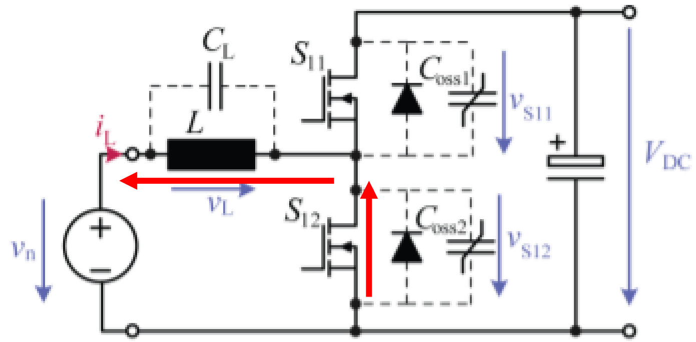


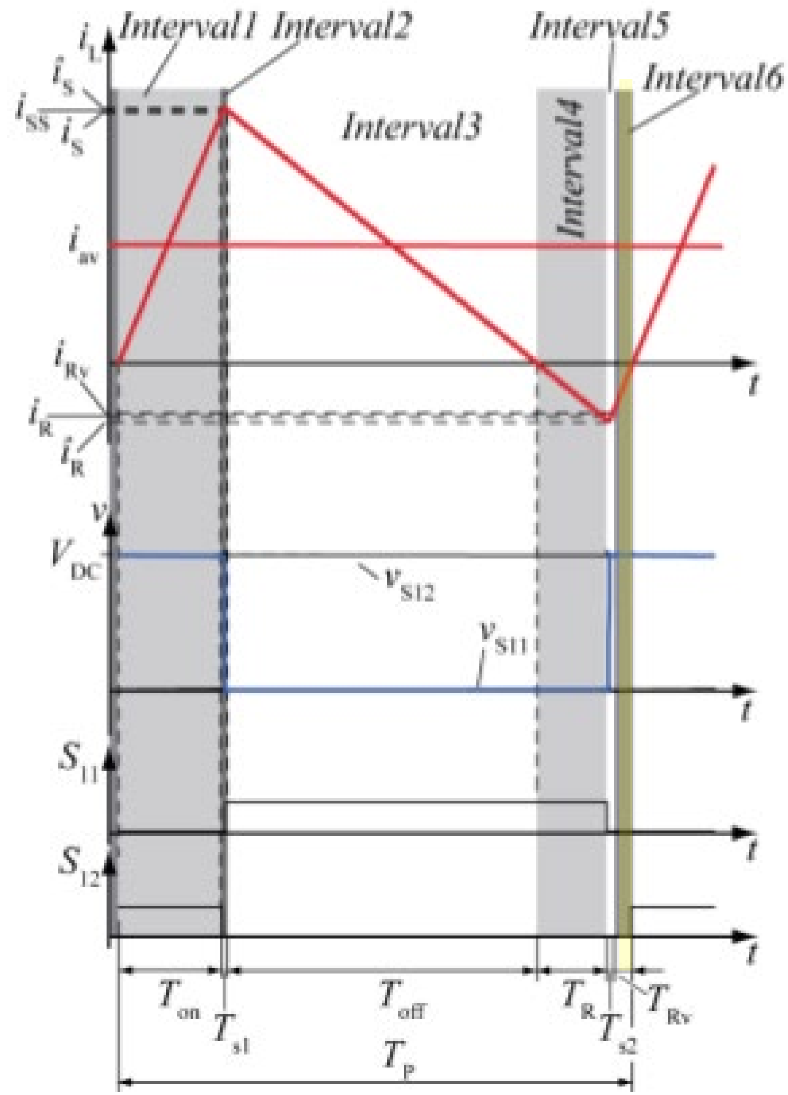
Interval 5

1. Dead time interval, $i_L<0$, charge Coss1 and discharge Coss2
2. S12's body diode conduct finally

[Ref]: C. Marxgut, J. Biela and J. W. Kolar, "Interleaved Triangular Current Mode (TCM) resonant transition, single phase PFC rectifier with high efficiency and high power density," The 2010 International Power Electronics Conference - ECCE ASIA -, 2010, pp. 1725-1732, doi: 10.1109/IPEC.2010.5542048.

TCM-Boost – Interval 6



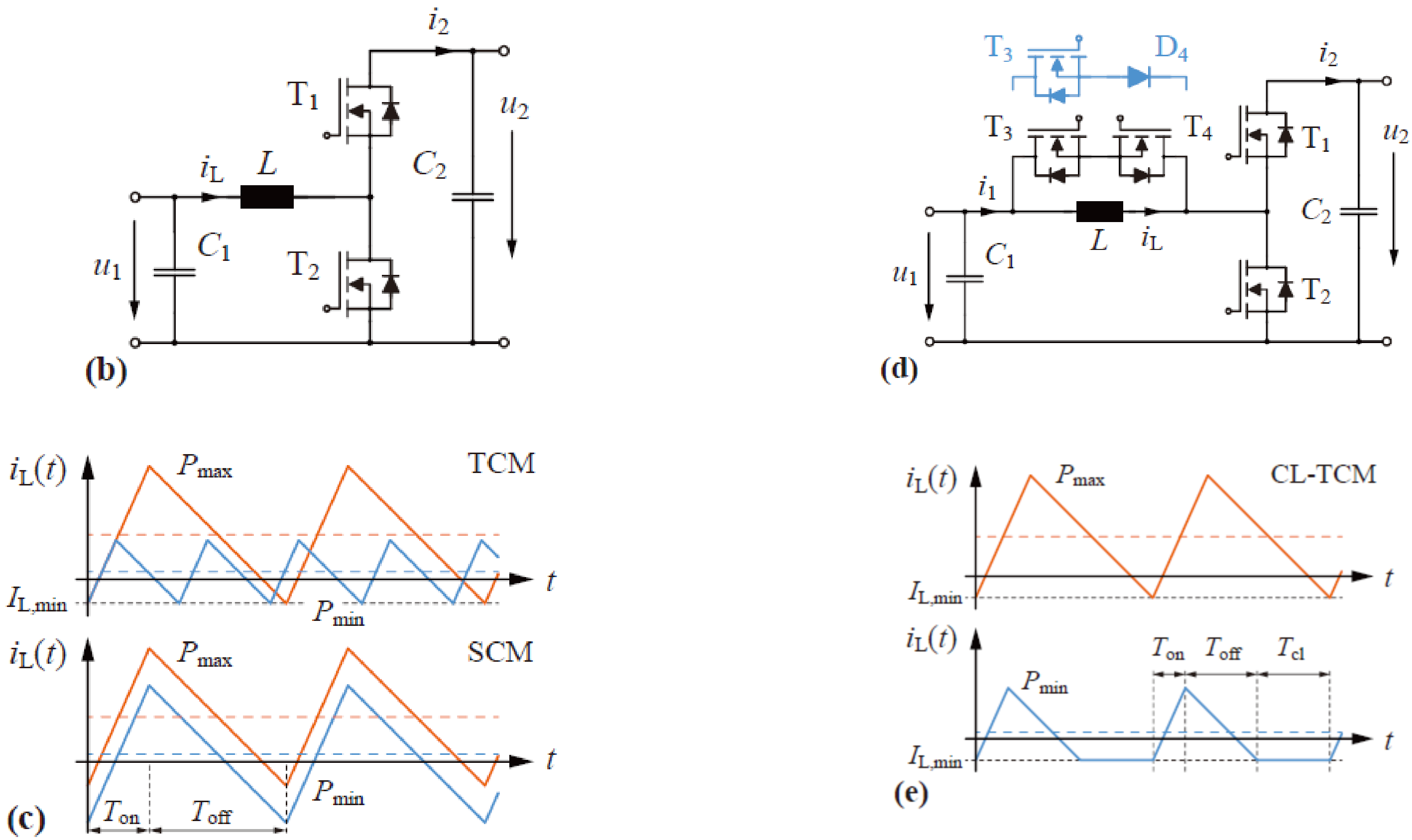


Interval 5

1. S12 turns on with ZVS
2. i_L increase linearly with $v_L=V_n$

[Ref]: C. Marxgut, J. Biela and J. W. Kolar, "Interleaved Triangular Current Mode (TCM) resonant transition, single phase PFC rectifier with high efficiency and high power density," The 2010 International Power Electronics Conference - ECCE ASIA -, 2010, pp. 1725-1732, doi: 10.1109/IPEC.2010.5542048.

Synchronous Conduction Mode (SCM), Triangular Current Mode (TCM) and Clamp-Switch TCM (CL-TCM)



- TCM w/i min negative current, light load with higher switching frequency.
- SCM with constant switching frequency, but have larger circulating current loss.
- CL-TCM could be a better solution but with more components.

[Ref]: Knecht, Oliver, Dominik Bortis, and Johann W. Kolar. "Comparative evaluation of a Triangular Current Mode (TCM) and Clamp-Switch TCM DC-DC boost converter." 2016 IEEE Energy Conversion Congress and Exposition (ECCE). IEEE, 2016.

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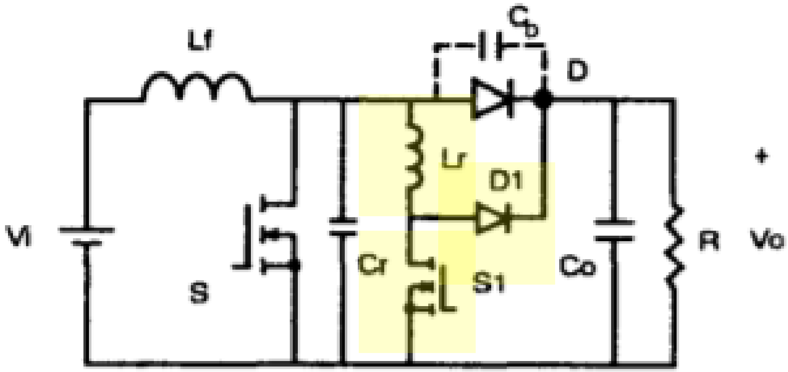
Zero Voltage Transition, ZVT
(Choose ZVT-Boost for example)



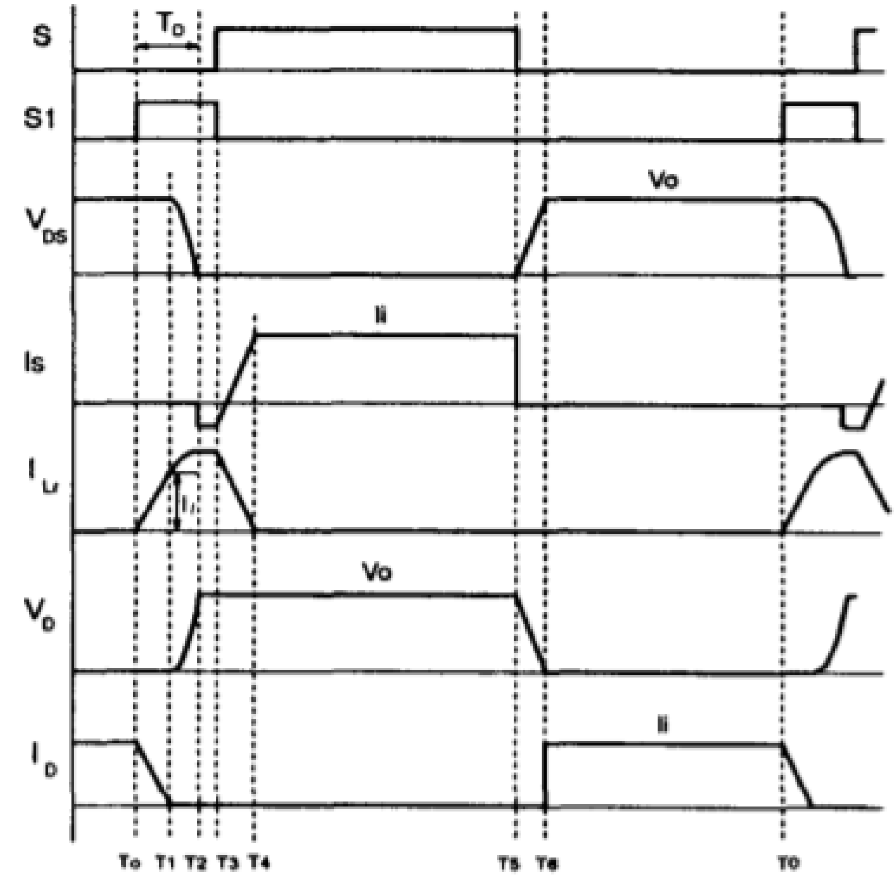


Fig. 1. Circuit diagram and waveforms of the boost ZVT-PWM converter.

Advantage

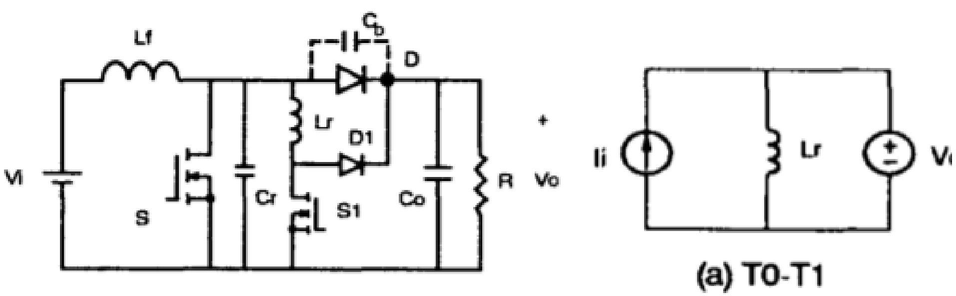
1. Use auxiliary switches to help zero-voltage switching of the main switch
2. The main circuit structure can still switch with zero voltage when working under CCM
3. The linkage sequence of the main switch and auxiliary switch is simple

Shortcoming

1. The withstand current of the auxiliary switch will be larger than that of the main switch
2. The on-time of the auxiliary switch will compress the duty cycle of the main switch.
3. The design of the auxiliary inductor is subject to the auxiliary switch-on time and the highest resonant inductor current

[Ref]: Hua, Guichao, et al. "Novel zero-voltage-transition PWM converters." IEEE transactions on Power Electronics 9.2 (1994): 213-219.

Zero Voltage Transition, ZVT – (T_0~T_1)



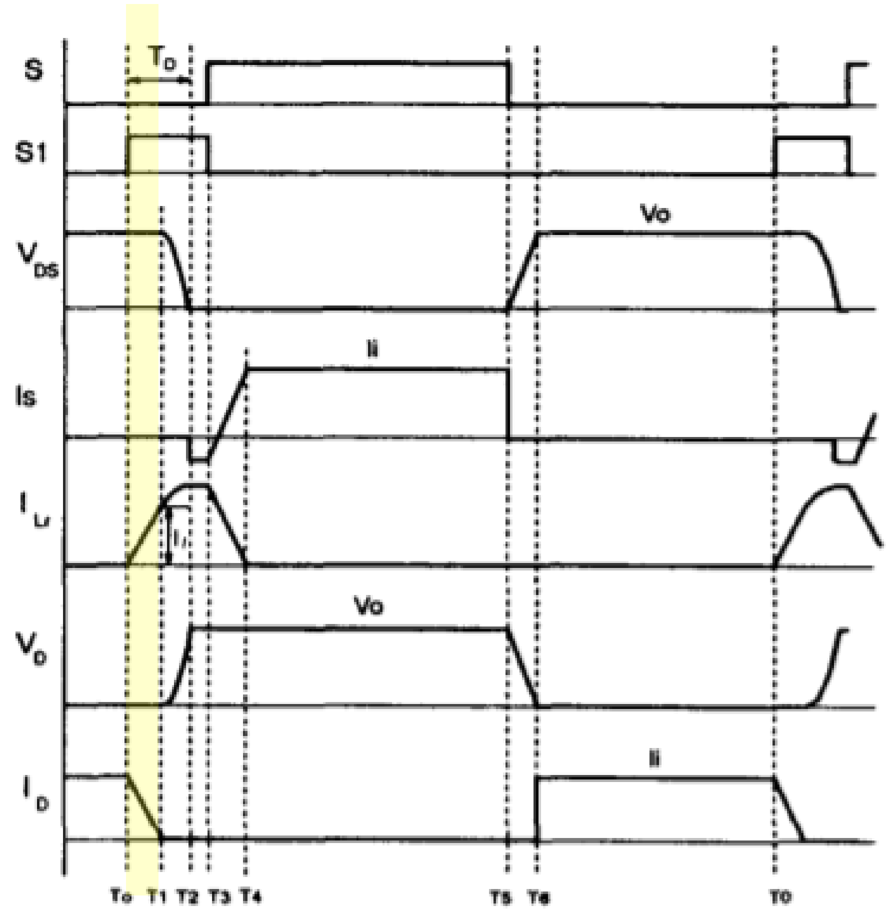


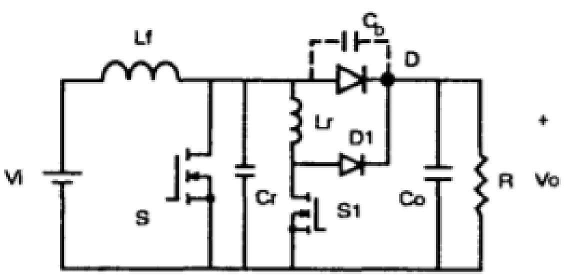
Fig. 1. Circuit diagram and waveforms of the boost ZVT-PWM converter.

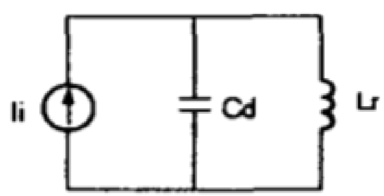
T_0-T_1 : Prior to T_0, the main switch (S) and the auxilia switch (S1) are off, and the rectifier diode (D) is conducting. At T_0, S1 is turned on. **The L_r current linearly ramps up** until it reaches Ii at T1, where **D is turned off with soft switching**. This time interval, to1, is given by:

$$t_{01} = \frac{I_i}{V_0/L_r}.$$

[Ref]: Hua, Guichao, et al. "Novel zero-voltage-transition PWM converters." IEEE transactions on Power Electronics 9.2 (1994): 213-219.

Zero Voltage Transition, ZVT – (T_1~T_2)





(b) T1-T2

T1-T2: L_r current continues to increase due to the resonance between and C_r. C_r is discharged until the resonance brings its voltage to zero at T2, where the anti-parallel diode of S starts to conduct. This resonant time period, t_{12}, is:

$$t_{12} = \frac{\pi}{2}\sqrt{L_r C_s}\,.$$

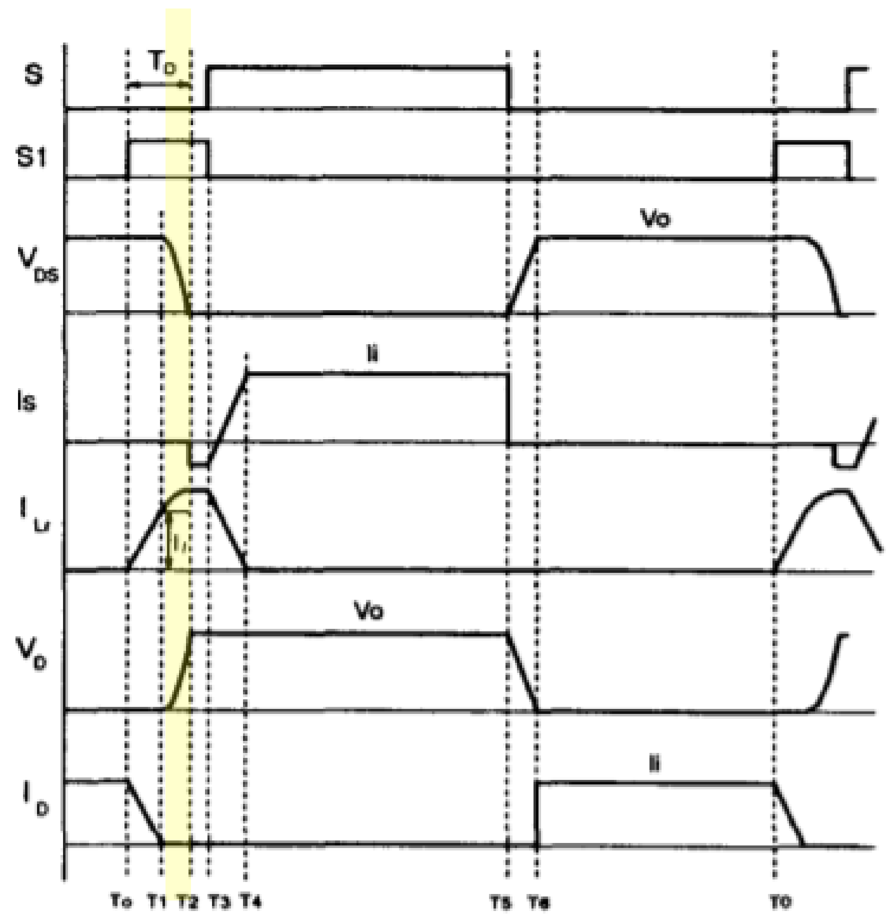
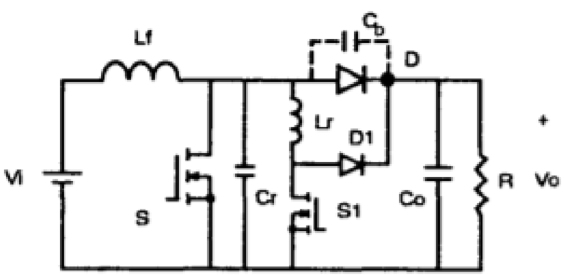
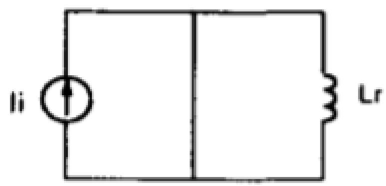


Fig. 1. Circuit diagram and waveforms of the boost ZVT-PWM converter.

[Ref]: Hua, Guichao, et al. "Novel zero-voltage-transition PWM converters." IEEE transactions on Power Electronics 9.2 (1994): 213-219.

Zero Voltage Transition, ZVT – (T_2~T_3)





(c) T2-T3

T2-T3: The anti-parallel diode of S is on. To achieve ZVS, the turn-on signal of S should be applied while its body diode is conducting. Besides, the time delay between S1 and S gate signals, T_D, has to satisfy the following inequality:

$$T_D \geq t_{01} + t_{12} = \frac{I_i}{V_o/L_r} + \frac{\pi}{2}\sqrt{L_r C_S}\,.$$

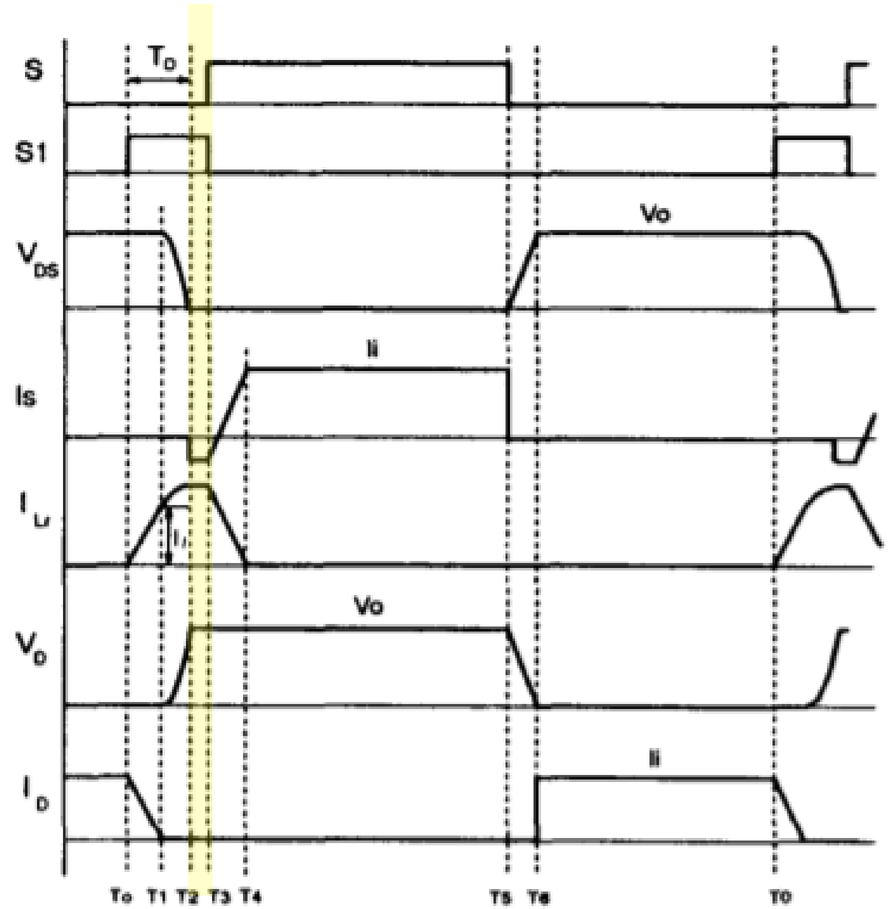


Fig. 1. Circuit diagram and waveforms of the boost ZVT-PWM converter.

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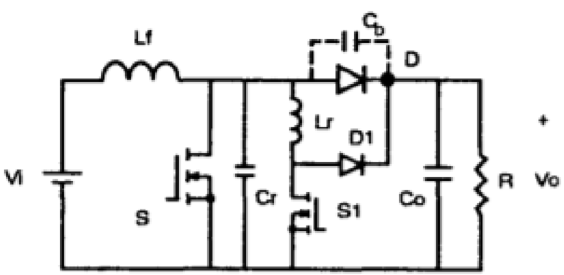
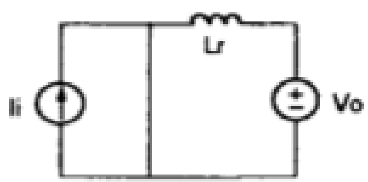
Zero Voltage Transition, ZVT – (T_3~T_4)





(d) T3-T4

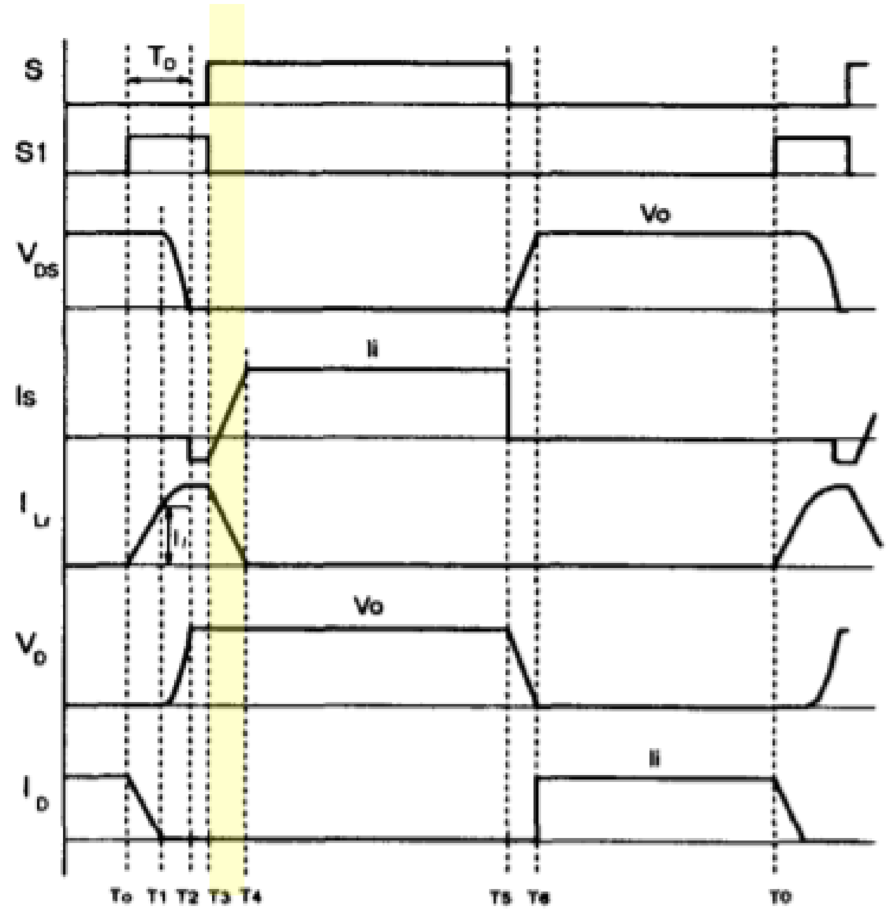
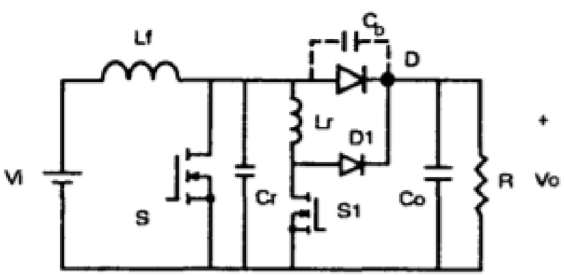


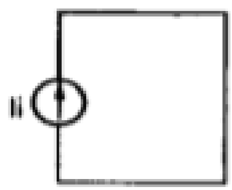
Fig. 1. Circuit diagram and waveforms of the boost ZVT-PWM converter.

T3-T4: At T3, S1 is turned off, and its voltage is clamped at Vo, due to the conduction of D1. During this time period, S is turned on. The energy stored in the resonant inductor is transferred to the load during this time interval. Lr, current decreases linearly until it reaches zero at T4.

[Ref]: Hua, Guichao, et al. "Novel zero-voltage-transition PWM converters." IEEE transactions on Power Electronics 9.2 (1994): 213-219.

Zero Voltage Transition, ZVT – (T_4~T_5)





(e) T4-T5

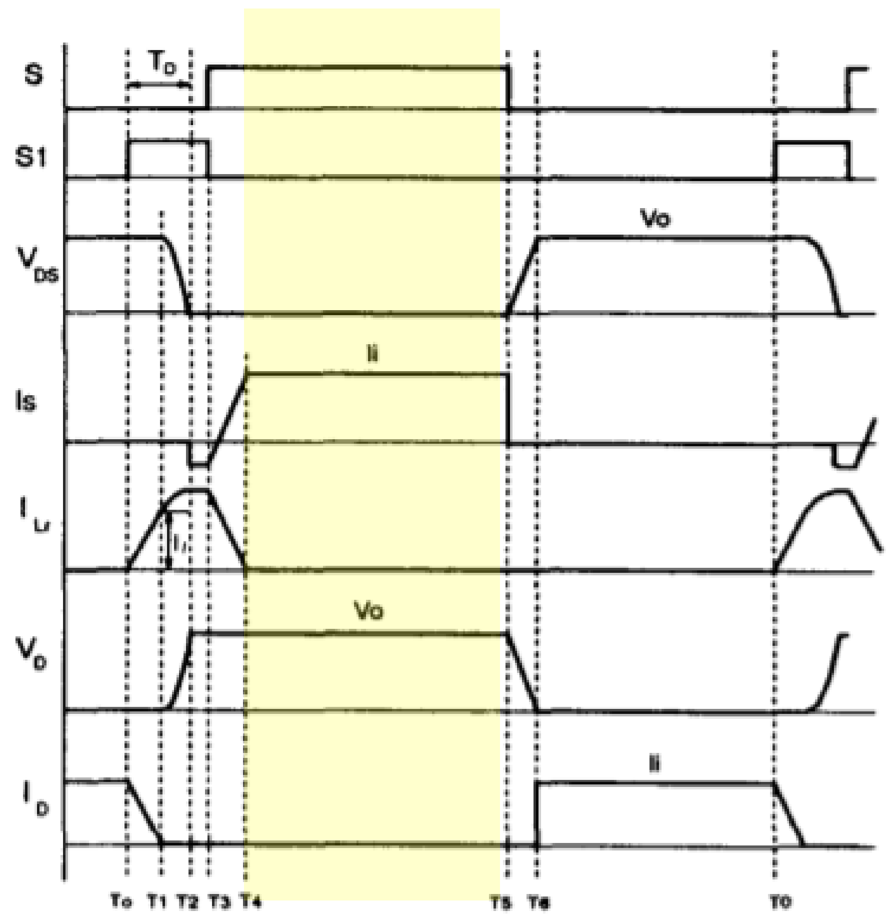
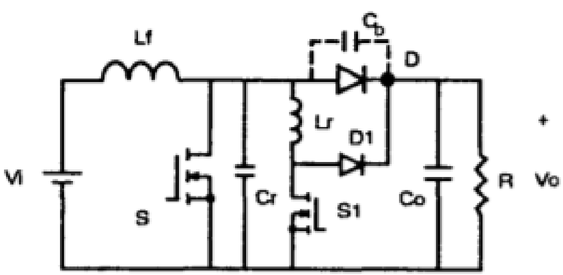


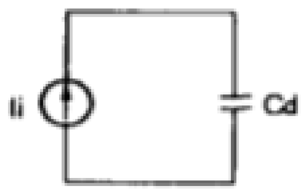
Fig. 1. Circuit diagram and waveforms of the boost ZVT-PWM converter.

T4-T5: D1 is turned off at T4. The operation of the circuit at this stage is identical to that of the PWM boost converter

[Ref]: Hua, Guichao, et al. "Novel zero-voltage-transition PWM converters." IEEE transactions on Power Electronics 9.2 (1994): 213-219.

Zero Voltage Transition, ZVT – (T_5~T_6)





(f) T5-T6

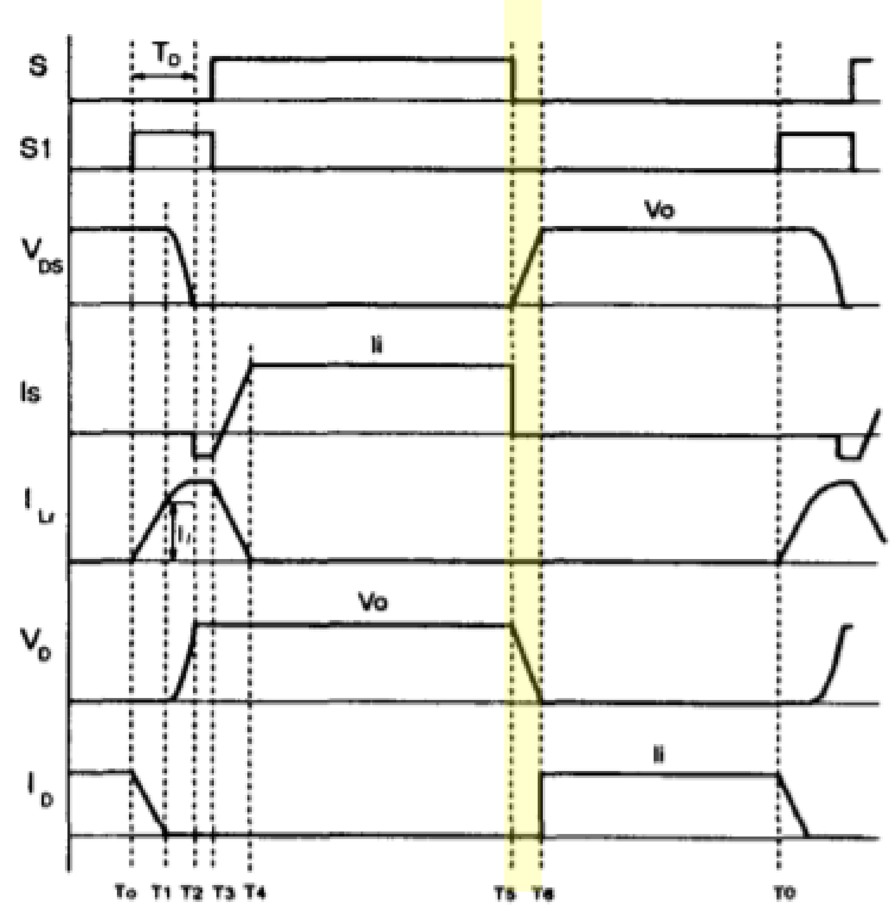
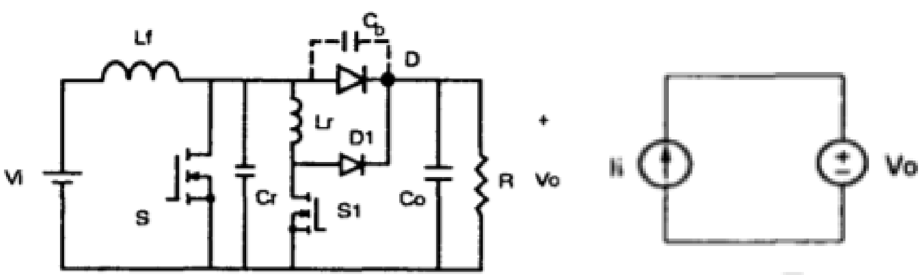


Fig. 1. Circuit diagram and waveforms of the boost ZVT-PWM converter.

T5-T6: At T5, S is turned off. Cr is linearly charged by Ii to Vi voltage

[Ref]: Hua, Guichao, et al. "Novel zero-voltage-transition PWM converters." IEEE transactions on Power Electronics 9.2 (1994): 213-219.

Zero Voltage Transition, ZVT – (T_6~T_0)



(g) T6-T0

T6-T0: This interval is identical to the freewheeling stage of the boost PWM converter. At To, S1 is turned on again, starting another switching cycle.

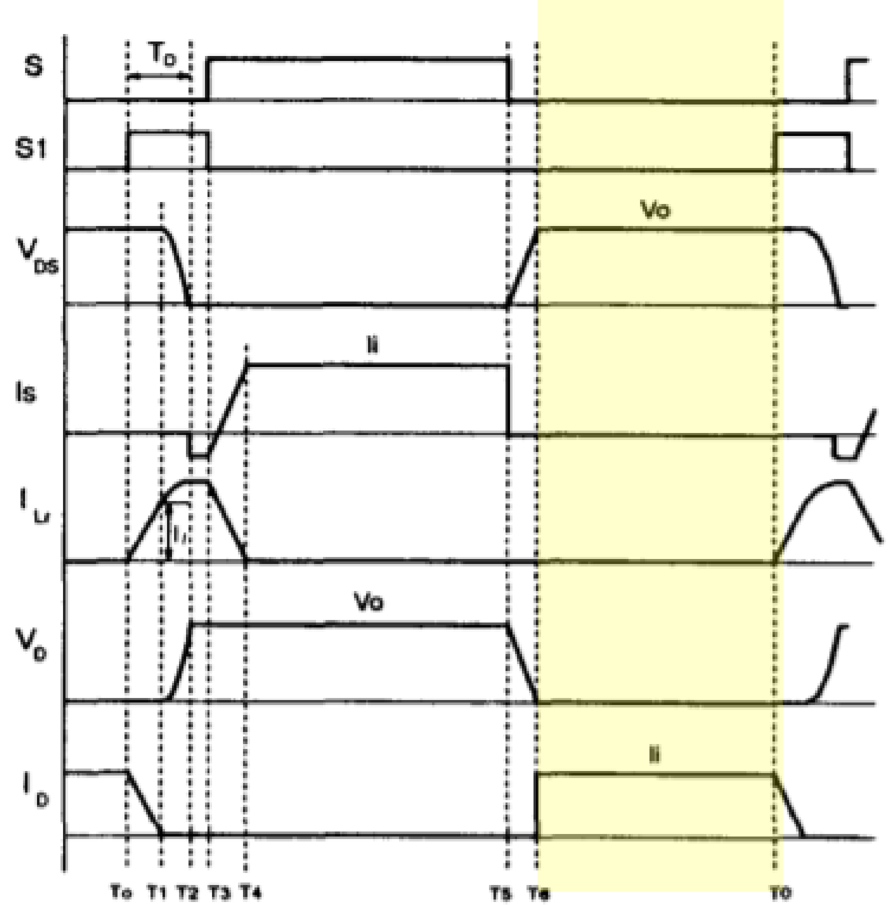


Fig. 1. Circuit diagram and waveforms of the boost ZVT-PWM converter.

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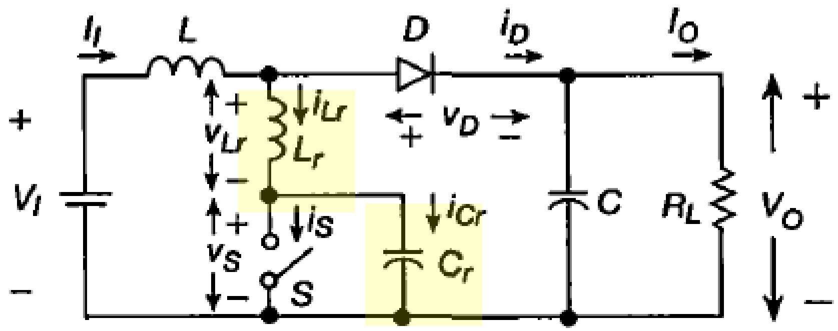
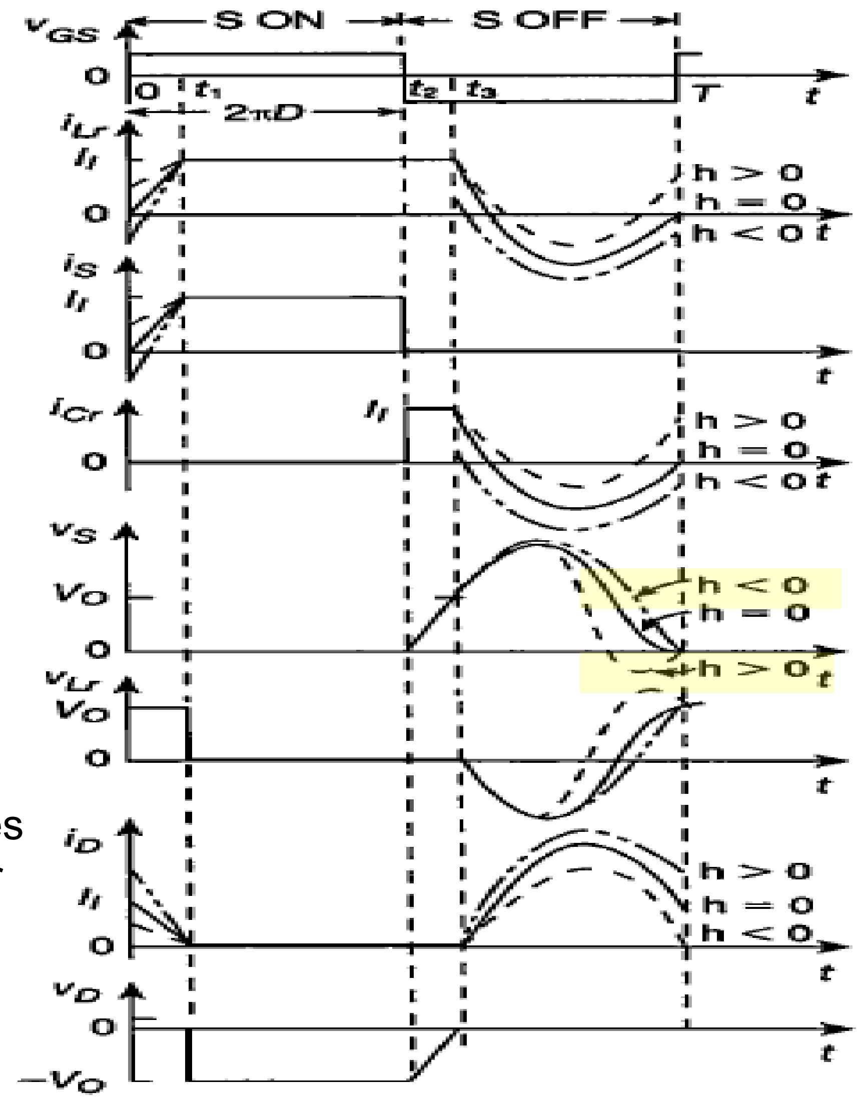
Quasi-Resonant Converter, QRC (Choose QRC-Boost for example)





Advantage:

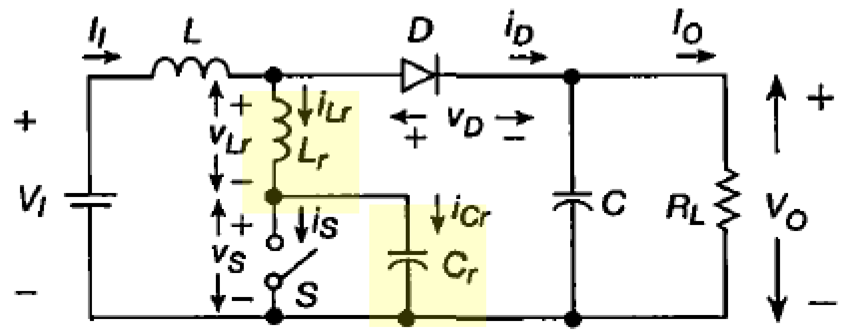
1. No need for additional auxiliary switches and drive signals
2. The main converter can have zero voltage switching function under CCM operation

Shortcoming:

1. Increase the voltage stress level of the main switch
2. The peak value of output diode current increases
3. The voltage conversion formula of the converter is changed to be related to the load and the switching frequency
4. Zero voltage switching can not be achieved under all load conditions

[Ref]: "RESONANT POWER CONVERTERS, Second Edition", A JOHN WILEY & SONS, INC., PUBLICATION, Marian K. Kazimierczuk; Dariusz Czarkowski.

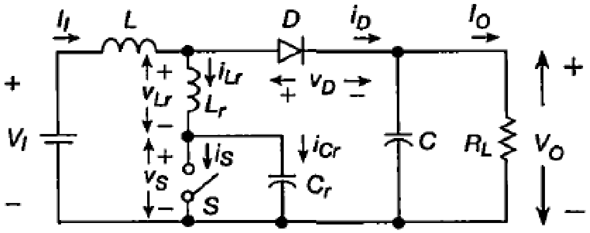
Quasi-Resonant Converter, QRC
(Choose QRC-Boost for example) - Symbol definition

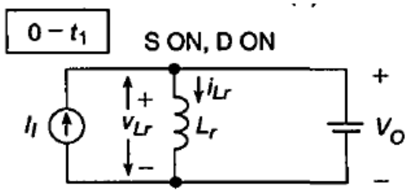


- The following definitions are used in the subsequent analysis.
  - The resonant frequency of the *Lr*-*Cr* circuit is
$$\omega_0 = \frac{1}{\sqrt{L_r C_r}}.$$
  - The normalized switching frequency is
$$A = \frac{f_s}{f_0}.$$
  - The loaded-quality factor is
$$Q = \frac{R_L}{\omega_0 L_r} = \omega_0 C_r R_L = \frac{R_L}{\sqrt{\frac{L_r}{C_r}}} = \frac{A R_L}{\omega_s L_r} = \frac{\omega_s C_r R_L}{A}.$$
  - The DC voltage transfer function is
$$M_{VDC} = \frac{V_O}{V_I}.$$
  - The normalized initial resonant inductor and switch current when the switch turns on are
$$h = \frac{i_L(0)}{I_I} = \frac{i_S(0)}{I_I}.$$

[Ref]: "RESONANT POWER CONVERTERS, Second Edition", A JOHN WILEY & SONS, INC., PUBLICATION, Marian K. Kazimierczuk; Dariusz Czarkowski.

Quasi-Resonant Converter, QRC – $0\sim t_1$





Inductor charging time interval $0 < t < t_1$:

Both the switch and diode are ON, during this time interval, $v_S = 0, v_D = 0$, $i_{Cr} = 0$, $v_{Lr} = V_O$, and

$$i_{Lr} = \frac{1}{\omega_s L_r}\int_0^{\omega_s t} v_{Lr}\, d(\omega_s t) + i_{Lr}(0) = \frac{V_O \omega_s t}{\omega_s L_r} + i_S(0).$$

Since $V_O = R_L I_O$ and $V_O/\omega_S L_r = I_I Q/(AM_{VDC})$,

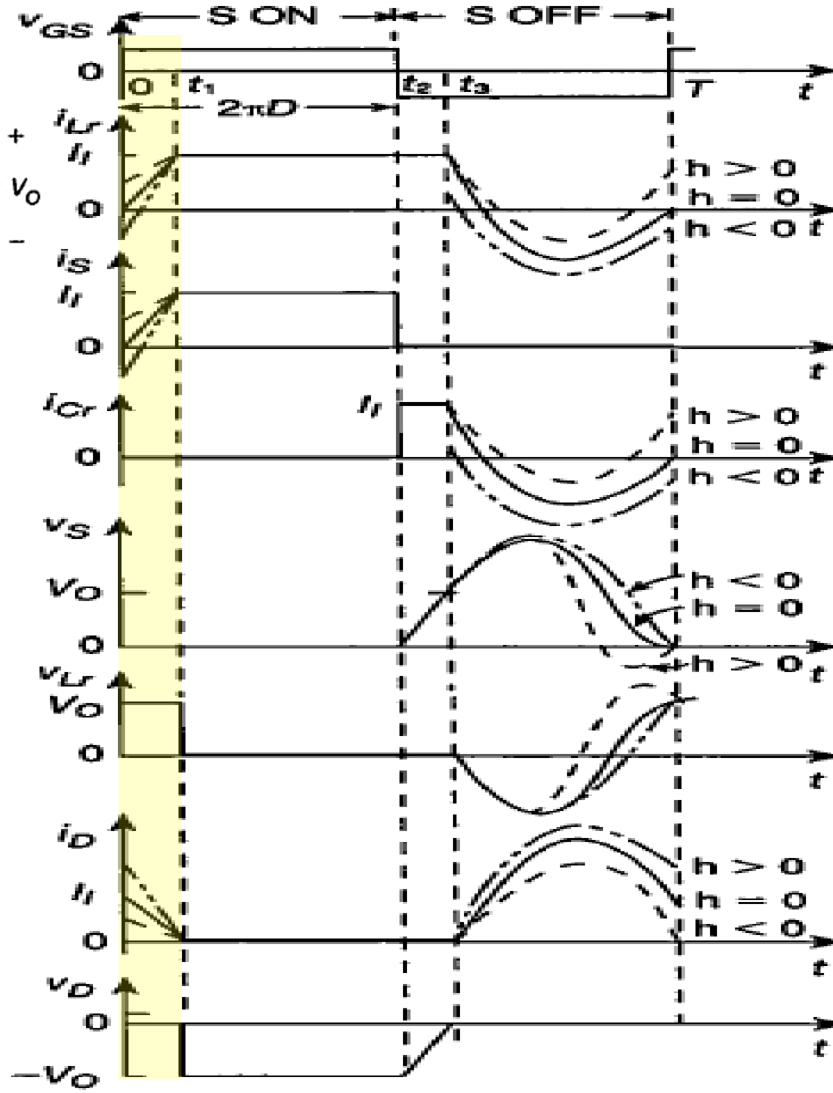
$$\frac{i_{Lr}(\omega_s t)}{I_I} = \frac{i_S(\omega_s t)}{I_I} = \frac{Q}{AM_{VDC}}\omega_s t + h.$$

The diode current waveform is given by

$$\frac{i_D(\omega_s t)}{I_I} = -\frac{Q}{AM_{VDC}}\omega_s t - h + 1.$$

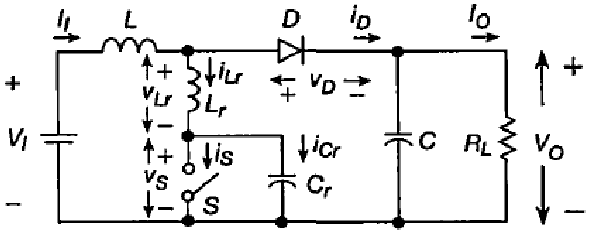
At the end of this time interval, $i_D(\omega_S t_1) = 0$. Hence,

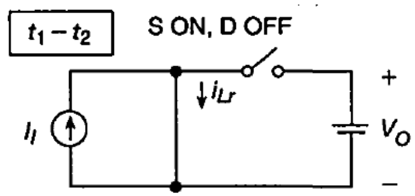
$$\omega_s t_1 = \frac{AM_{VDC}}{Q}(1 - h).$$

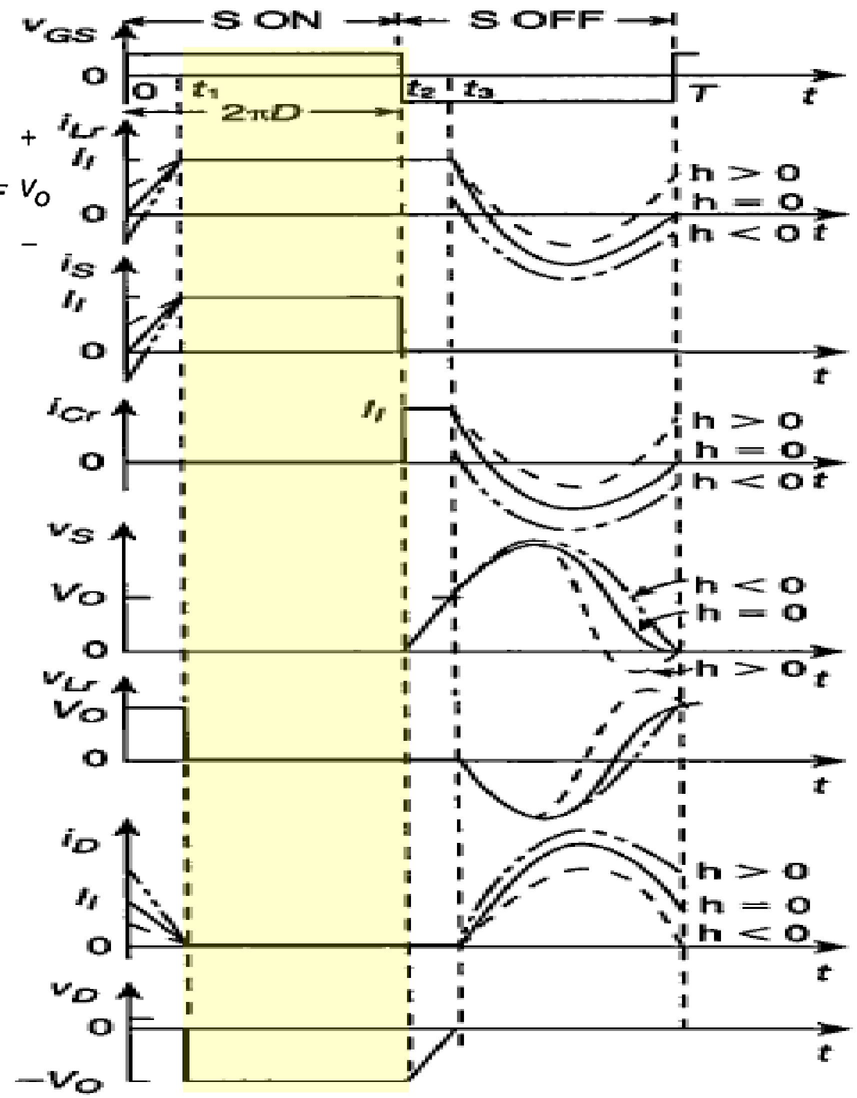


[Ref]: "RESONANT POWER CONVERTERS, Second Edition", A JOHN WILEY & SONS, INC., PUBLICATION, Marian K. Kazimierczuk; Dariusz Czarkowski.

Quasi-Resonant Converter, QRC – t_1~t_2



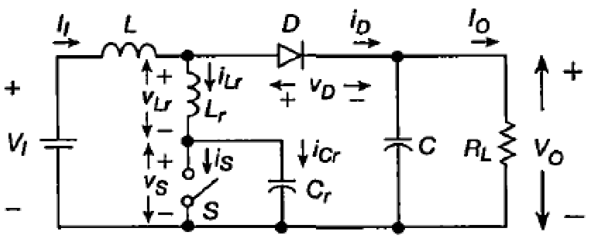


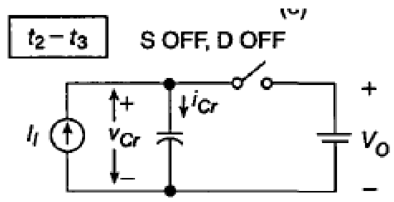


Idle time interval $t_1 < t < t_2$:
The switch is ON and the diode is OFF, during this time interval, During this time interval, $v_S = 0$, $i_{Cr} = 0$, $i_D = 0$, $v_{Lr} = 0$, $i_S = i_{Lr} = I_I$, and $v_D = -V_O$.
This time interval ends at $\omega_S t_2 = s2\pi D$,
when the transistor is turned off by the gate driver.

[Ref]: "RESONANT POWER CONVERTERS, Second Edition", A JOHN WILEY & SONS, INC., PUBLICATION, Marian K. Kazimierczuk; Dariusz Czarkowski.

Quasi-Resonant Converter, QRC – t_2~t_3





Capacitor charging time interval $t_2 < t < t_3$:
Both the switch and the diode are OFF., during this time interval, During this time interval, $i_S=0$, $i_D = 0$, $i_{Lr} = i_{Cr} = I_I$. $v_{Lr} = 0$, and.

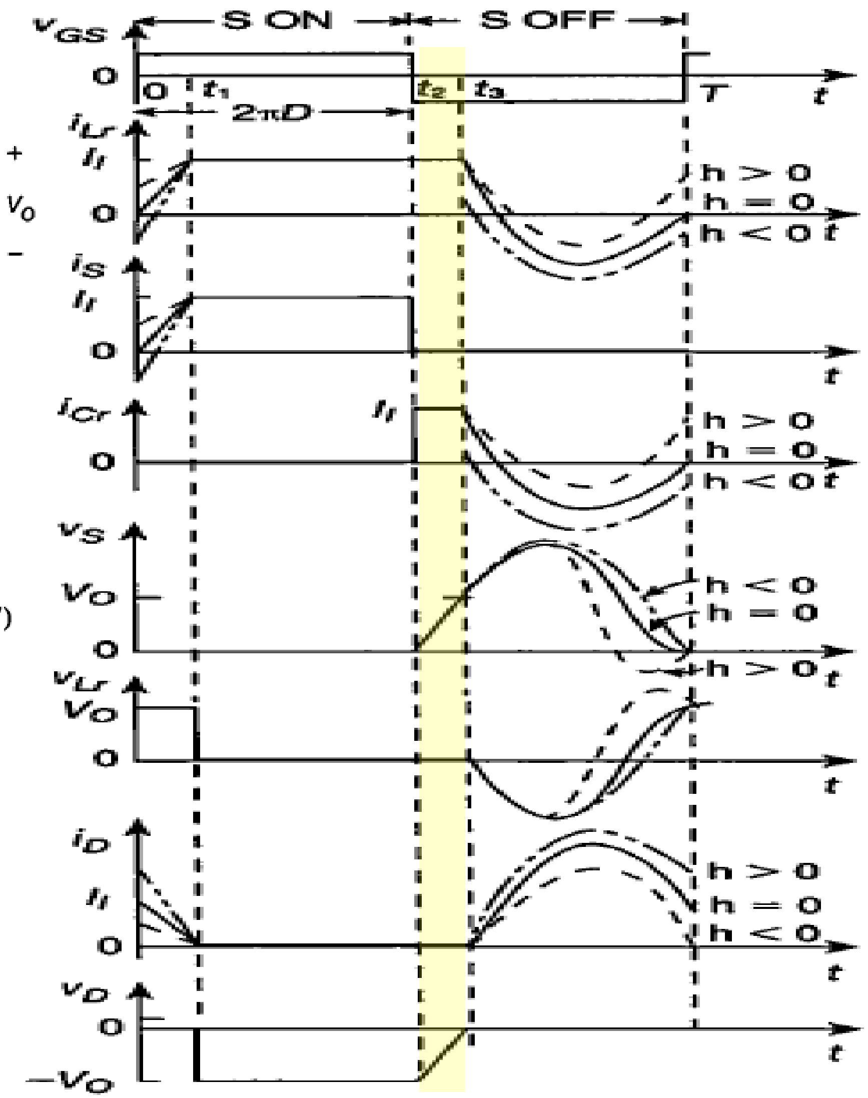
$$v_S = \frac{1}{\omega_s C_r}\int_{2\pi D}^{\omega_s t} v_{Cr}\, d(\omega_s t) + v_{Cr}(2\pi D) = \frac{1}{\omega_s C_r}\int_{2\pi D}^{\omega_s t} V_I\, d(\omega_s t) + v_{Cr}(2\pi D)$$
$$= \frac{I_I}{\omega_s C_r}(\omega_s t - 2\pi D). \qquad (22.67)$$

Because $I_I/(\omega_S C_r)=M_{VDC}V_O/(AQ)$ and $I_O = V_O/R_L$, we get

$$\frac{v_S}{V_O} = \frac{M_{VDC}}{AQ}(\omega_s t - 2\pi D) \qquad \frac{v_D}{V_O} = \frac{M_{VDC}}{AQ}(\omega_s t - 2\pi D) - 1.$$

The end of this time interval is determined by $v_D(\omega_S t_3) = 0$. Hence,

$$\omega_s t_3 = 2\pi D + \frac{AQ}{M_{VDC}}.$$



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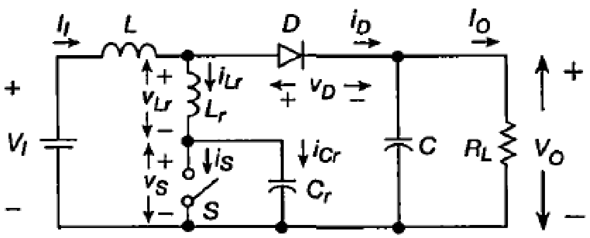
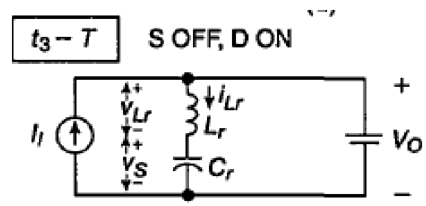
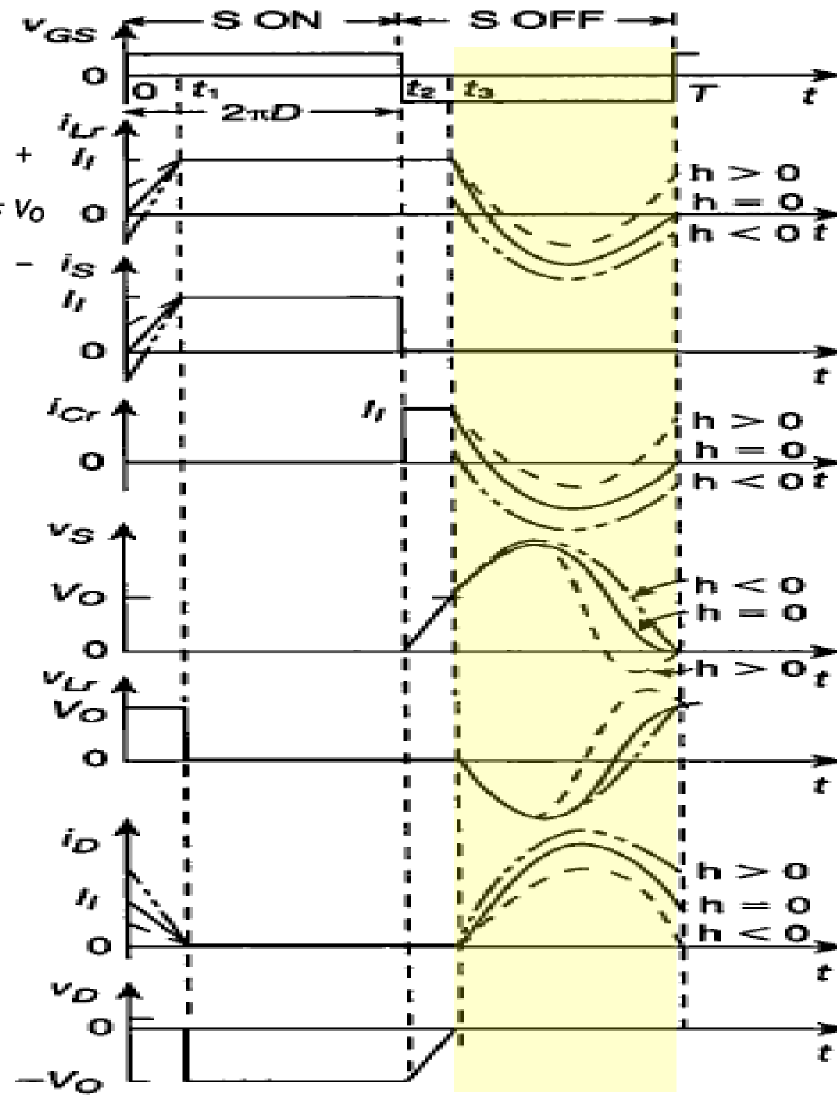
Quasi-Resonant Converter, QRC – $t_3 \sim t_4$







Resonant time interval $t_3 < t < T$:
The switch is OFF and the diode is ON. During this time interval, $i_S = 0$ and $v_D = 0$. The initial conditions are iLr($\omega_S t3$)=*Il and* vS($\omega_S t3$) = VI, and

$$\frac{i_{Lr}}{I_I} = \frac{i_{Cr}}{I_I} = \cos\frac{\omega_s t - \omega_s t_3}{A}.$$

The diode current waveform is

$$\frac{i_D}{I_I} = 1 - \cos\frac{\omega_s t - \omega_s t_3}{A}.$$

The switch voltage waveform is

$$\frac{v_S}{V_I} = \frac{M_{VDC}}{Q}\sin\frac{\omega_s t - \omega_s t_3}{A} + 1.$$

ZVS condition: $M_{VDC}/Q>=1$, depend on load condition

[Ref]: "RESONANT POWER CONVERTERS, Second Edition", A JOHN WILEY & SONS, INC., PUBLICATION, Marian K. Kazimierczuk; Dariusz Czarkowski.

Derivation of the duty cycle

For ZVS operation, $v_S(2\pi)=v_S(0)=0$. *Also,* $i_{Lr}(2\pi)=i_{Lr}(0)=hI_I$. Hence, the relationships among M_{VDC}, Q, and h are given by a set of equation

$$h = \cos\left[\frac{2\pi(1-D)}{A} - \frac{Q}{M_{VDC}}\right] \qquad \frac{Q}{M_{VDC}} = -\sin\left[\frac{2\pi(1-D)}{A} - \frac{Q}{M_{VDC}}\right].$$

This set of equations and trigonometric identity yield

$$\left(\frac{Q}{M_{VDC}}\right)^2 + h^2 = 1$$

Producing

$$\frac{Q}{M_{VDC}} = \sqrt{1-h^2} \qquad h = \pm\sqrt{1-\left(\frac{Q}{M_{VDC}}\right)^2}.$$

The duty cycle is given by

$$D = 1 - \frac{1}{2\pi}\left(\frac{f_s}{f_0}\right)\left[2\pi n - \arccos h + \sqrt{1-h^2}\right]$$
$$= 1 - \frac{1}{2\pi}\left(\frac{f_s}{f_0}\right)\left[2\pi n - \arccos\sqrt{1-\left(\frac{Q}{M_{VDC}}\right)^2} + \frac{Q}{M_{VDC}}\right]$$

For h = 0, *h = 0 means* $v_S(2\pi)=0$. *Also,* $i_{Lr}(2\pi)=i_{Lr}(0)=0$, *ZVS with main switch & ZCS with diode*

$$D = 1 - \frac{(4n-1)\pi+2}{4\pi}\left(\frac{f_s}{f_0}\right).$$

For n = 1,

$$D = 1 - \frac{3\pi+2}{4\pi}\left(\frac{f_s}{f_0}\right) = 1 - 0.9092\left(\frac{f_s}{f_0}\right).$$

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DC Voltage Transfer Function

The DC output current is

$$I_O = \frac{1}{2\pi}\int_0^{2\pi} i_D d(\omega_s t) = I_I\left[1 - D + \frac{(1-h^2)}{4\pi\sqrt{1-h^2)}}\right].$$

Assuming that the converter is lossless, fo $I_O V_O = I_I V_I$. Hence, the DC voltage transfer function is given by

$$M_{VDC} = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{1}{1 - D + \frac{A(1-h^2)}{4\pi\sqrt{1-h^2}}}$$

$$= \frac{2\pi}{A\left[2\pi n - \arccos\, h + \sqrt{1-h^2} + \frac{(1-h)^2}{2\sqrt{1-h^2}}\right]}.$$

Thus,

$$M_{VDC} = \frac{2\pi}{\left(\frac{f_s}{f_0}\right)\left\{(2n-1)\pi + \frac{Q}{2M_{VDC}} + \arccos\sqrt{1-\left(\frac{Q}{M_{VDC}}\right)^2} + \frac{M_{VDC}}{Q}\left[1+\sqrt{1-\left(\frac{Q}{M_{VDC}}\right)^2}\right]\right\}} \quad \text{for } h \le 0$$

$$M_{VDC} = \frac{2\pi}{\left(\frac{f_s}{f_0}\right)\left\{2n\pi + \frac{Q}{2M_{VDC}} - \arccos\sqrt{1-\left(\frac{Q}{M_{VDC}}\right)^2} + \frac{M_{VDC}}{Q}\left[1-\sqrt{1-\left(\frac{Q}{M_{VDC}}\right)^2}\right]\right\}} \quad \text{for } h \ge 0.$$

For h = 0,

$$M_{VDC} = \frac{1}{1-D} = \frac{4\pi}{[(4n-1)\pi + 2)]\left(\frac{f_s}{f_0}\right)}$$

which for n = 1 becomes

$$M_{VDC} = \frac{1}{1-D} = \frac{4\pi}{(3\pi+2)\left(\frac{f_s}{f_0}\right)} = \frac{1.1}{\left(\frac{f_s}{f_0}\right)}.$$

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Current and Voltage Stresses

The switch peak current and voltage are

$$I_{SM} = I_I = M_{VDC} I_O$$

and

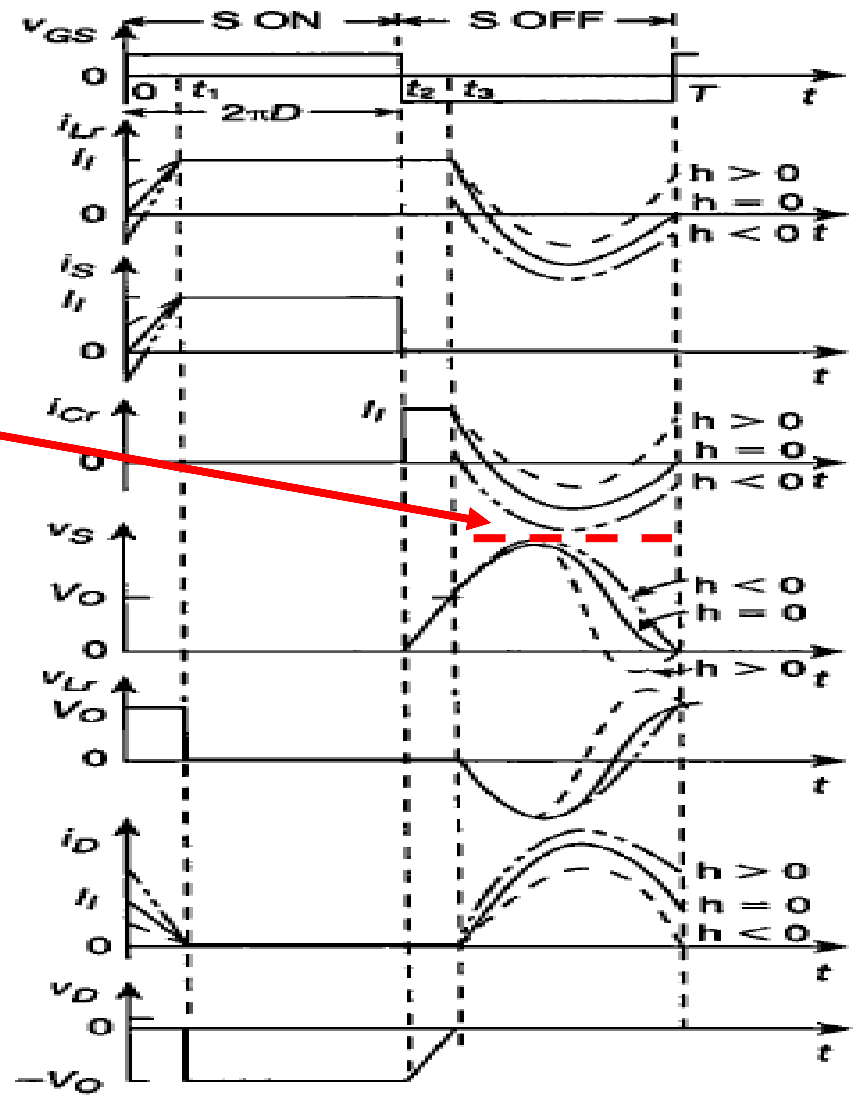
$$V_{SM} = \left(\frac{M_{VDC}}{Q} + 1\right) V_O = \left(\frac{Z_o M_{VDC}}{R_L} + 1\right) V_O.$$

The diode peak current and voltage are

$$I_{DM} = 2I_I = 2M_{VDC} I_O$$

and

$$V_{DM} = V_O.$$



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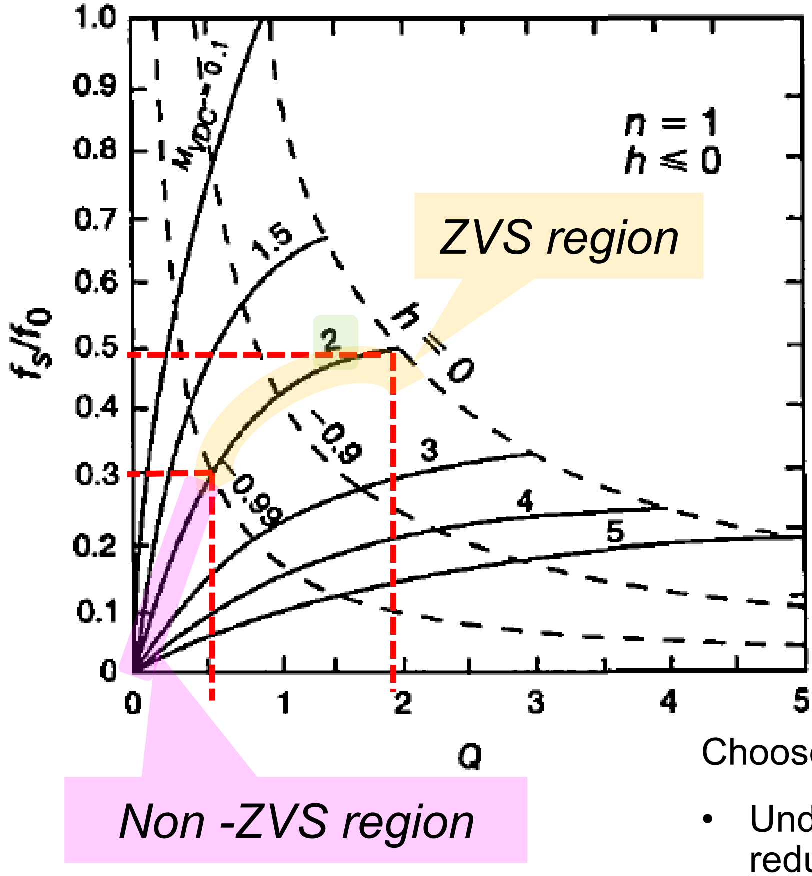
The relationship between voltage gain, switching frequency and load condition.



$$Q = \frac{R_L}{\omega_0 L_r} = \omega_0 C_r R_L = \frac{R_L}{\sqrt{\frac{L_r}{C_r}}} = \frac{AR_L}{\omega_s L_r} = \frac{\omega_s C_r R_L}{A}.$$

$$h = \pm\sqrt{1 - \left(\frac{Q}{M_{VDC}}\right)^2}.$$

ZVS condition: $M_{VDC}/Q>=1$, depend on load condition, Thus, h = -1~1

$$M_{VDC} = \frac{2\pi}{\left(\frac{f_s}{f_0}\right)\left\{(2n-1)\pi + \frac{Q}{2M_{VDC}} + \arccos\sqrt{1-\left(\frac{Q}{M_{VDC}}\right)^2} + \frac{M_{VDC}}{Q}\left[1+\sqrt{1-\left(\frac{Q}{M_{VDC}}\right)^2}\right]\right\}} \quad \text{for } h \le 0$$

$$M_{VDC} = \frac{1}{1-D} = \frac{4\pi}{(3\pi+2)\left(\frac{f_s}{f_0}\right)} = \frac{1.1}{\left(\frac{f_s}{f_0}\right)}.$$ *for h = 0*

Choose M_{VDC}=2 curve for example:

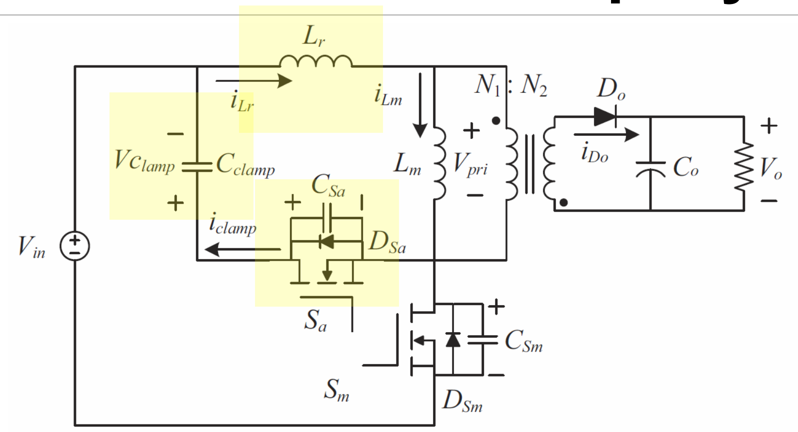
- Under the fixed voltage gain condition, the converter must reduce the switching frequency to meet the voltage regulation rate when the loading is increased.
- The load can only meet zero voltage switching within a specific range.

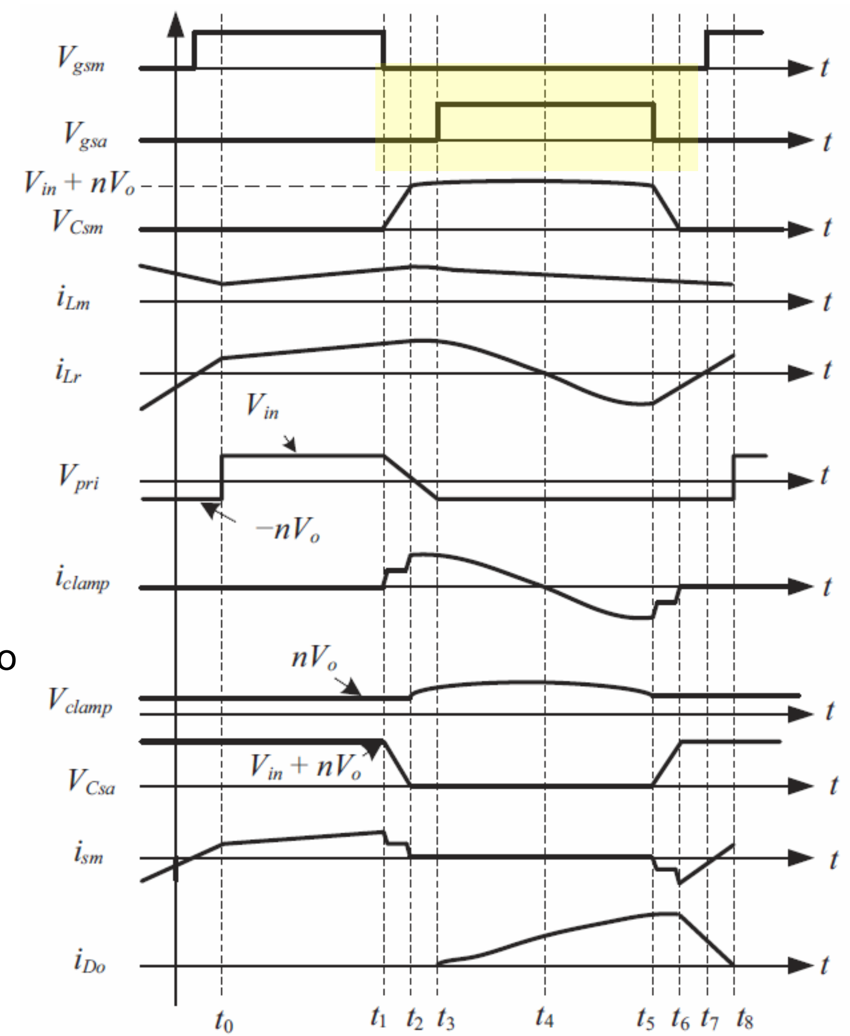
[Ref]: "RESONANT POWER CONVERTERS, Second Edition", A JOHN WILEY & SONS, INC., PUBLICATION, Marian K. Kazimierczuk; Dariusz Czarkowski.

Course outline – Week 5

- **Introduction of Zero Voltage Switching / Zero Current Switching technology**
  - Review the switching characteristics and the reasons for adopting ZVS or ZCS
  - The basic principle to realize ZVS
- **Common methods to implement ZVS**
  - Triangular Current Mode, TCM
  - Zero Voltage Transition, ZVT
  - Quasi-Resonant Converter, QRC
  - Active-Clamp
  - Resonant Converter
  - Dual Active Bridge, DAB
  - Phase-Shift Full Bridge, PSFB

Active-Clamp
(Choose Active-Clamp Flyback CCM for example)





Advantage:

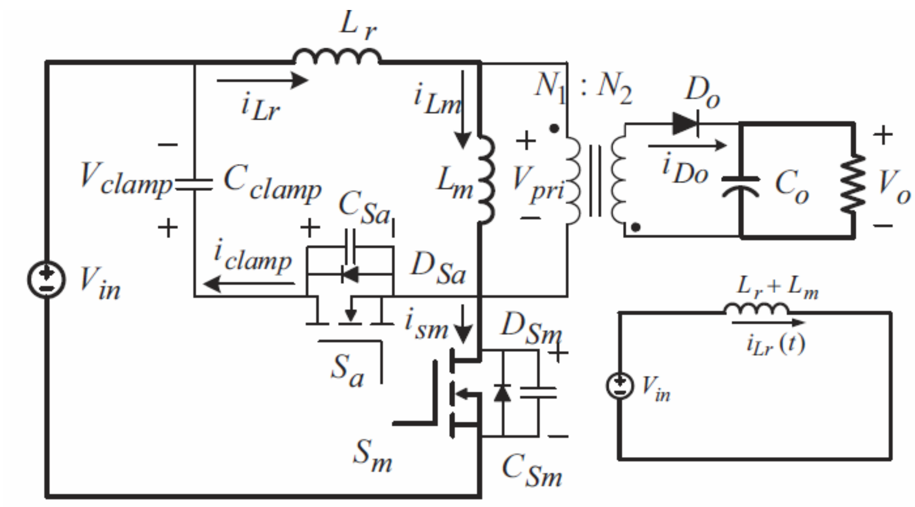
1. The auxiliary switch and the main switch are complementary, and the control signal of the auxiliary switch is simple to realize
2. Both the main switch and the auxiliary switch can achieve zero voltage conduction
3. Recovery of transformer leakage inductance energy to increase efficiency
4. Suppress the maximum cross voltage of the main switch (eliminate voltage spike)
5. Fixed switching frequency

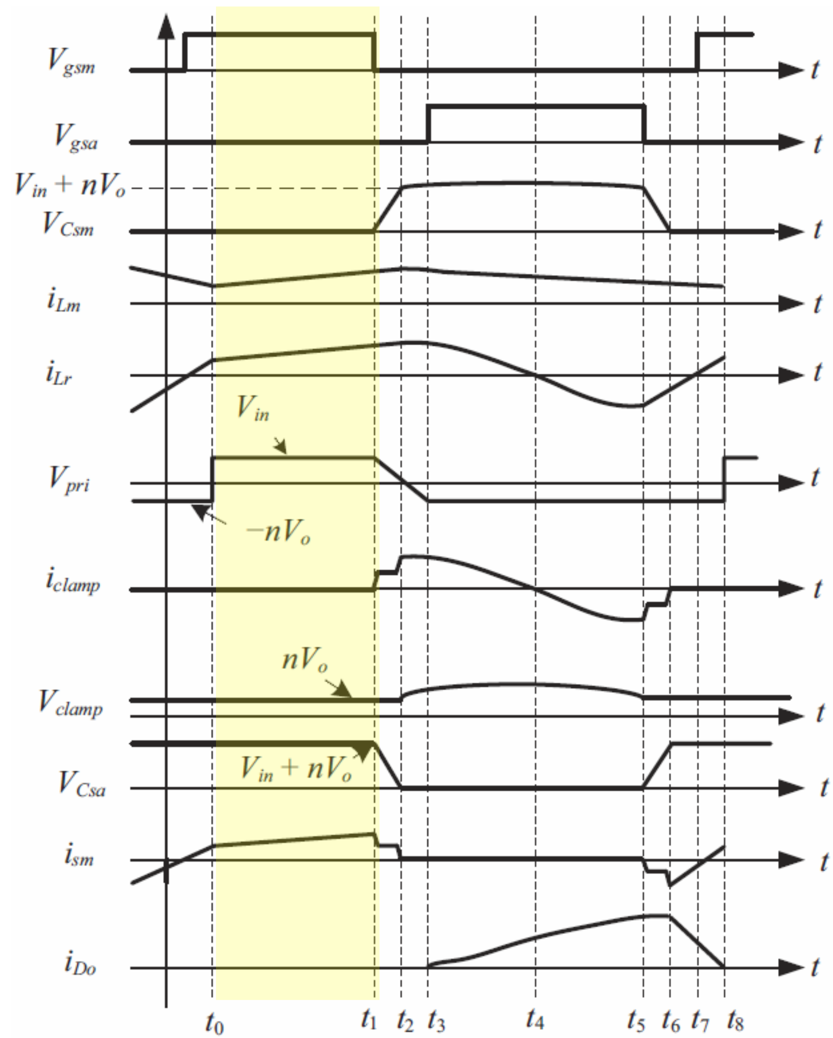
Shortcoming:

1. The peak current of the output diode increases
2. The zero voltage cut range is limited by the load condition and the magnitude of the resonance inductance

[Ref]: ANALYSIS AND IMPLEMENTATION OF SOFT SWITCHING FLYBACK CONVERTER WITH AN ACTIVE CLAMP CIRCUIT
Ching-Lung Chu* Chao-Chung Huang, Department of Electrical Engineering Southern Taiwan University of Science and Technology ,Tainan City, Taiwan 710, R.O.C

Active Clamp Flyback CCM - t_0~t_1





- **State 1(Linear charging interval):**
  - i_{Lr}=i_{Lm} current increase linearly.
  - V_{in}=$(L_m$+$L_r)$*di_{Lr}/dt

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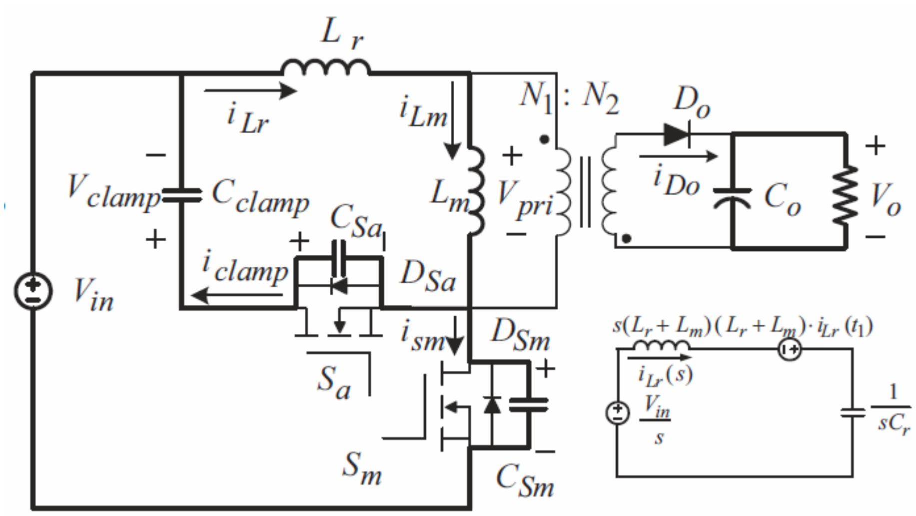
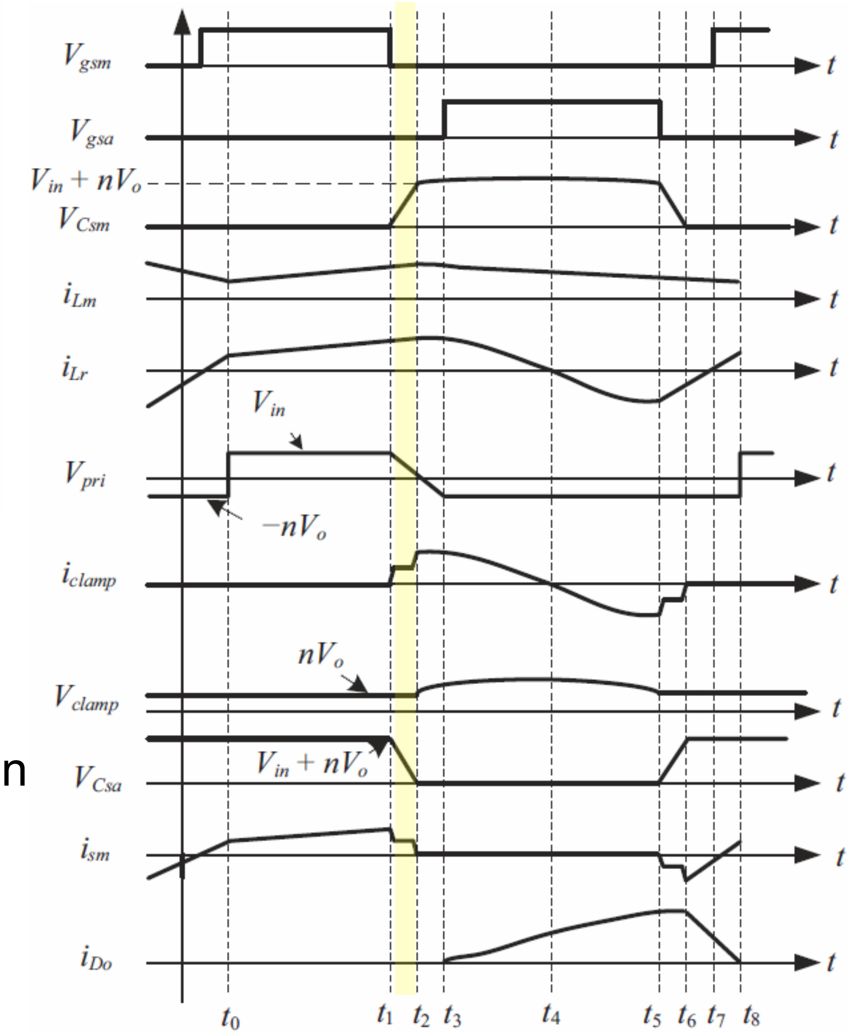
Active Clamp Flyback CCM – t_1~t_2





- **State 2(Resonant interval) :**
  - S_m turns off
  - L_r, L_m, C_{Sm}, C_{Sa}, C_{clamp} start to resonan
  - Interval ends with $V_{Csm} = V_{in}+V_{clamp}$

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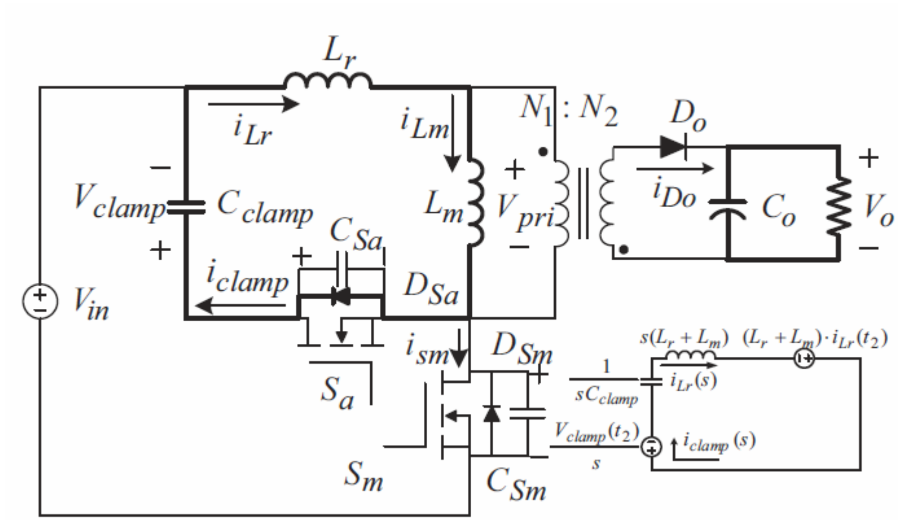
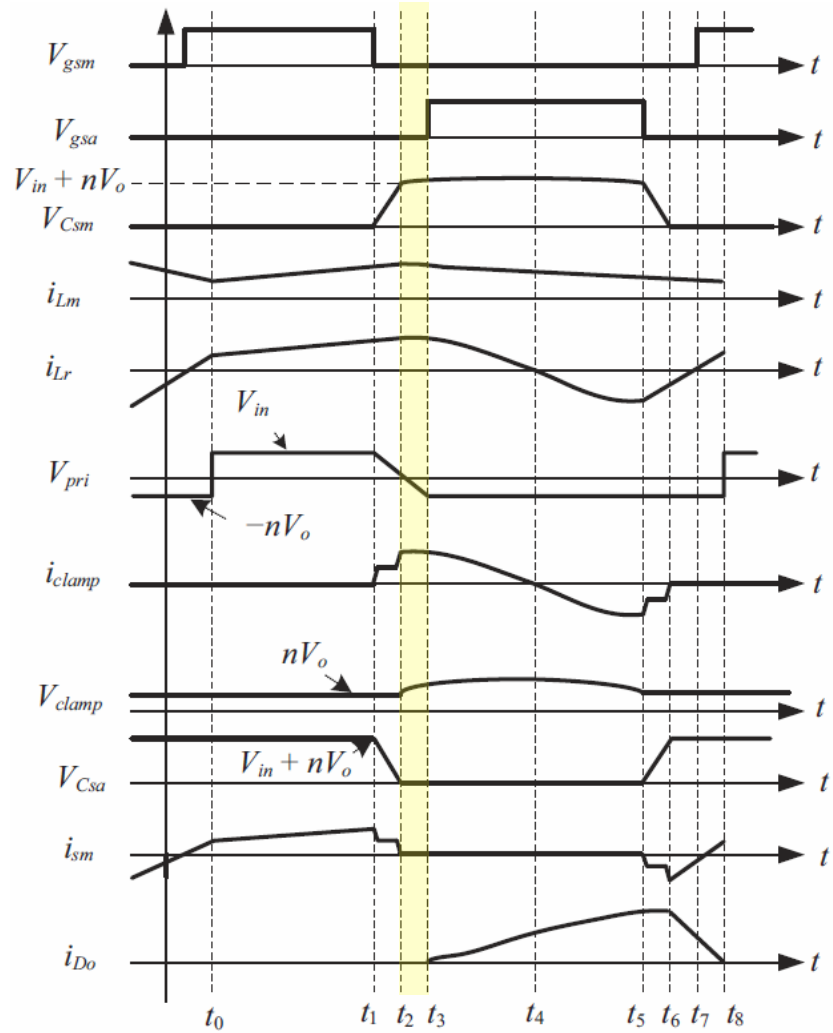
Active Clamp Flyback CCM – t_2~t_3





- **State 3:**
  - D_{Sa} conduct.
  - S_a ready for ZVS
  - C_{clamp} charging, V_{clamp} rising
  - $i_{Lm}=i_{Lr}$

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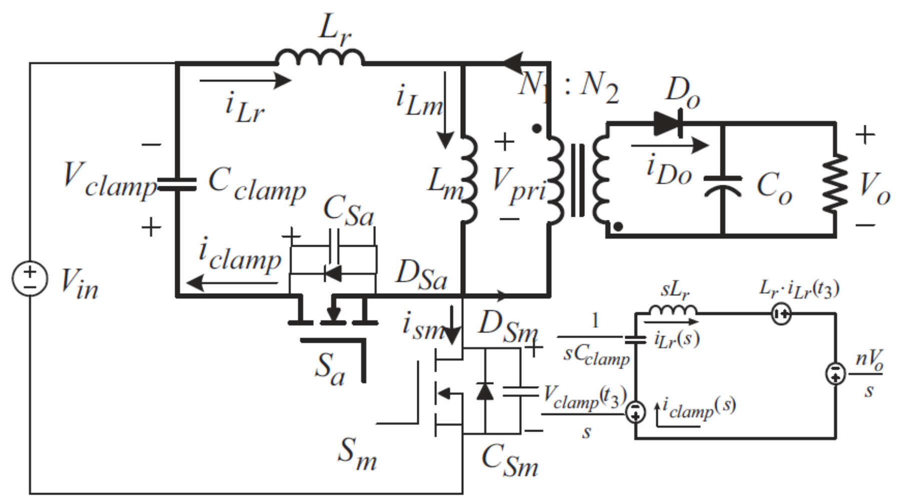
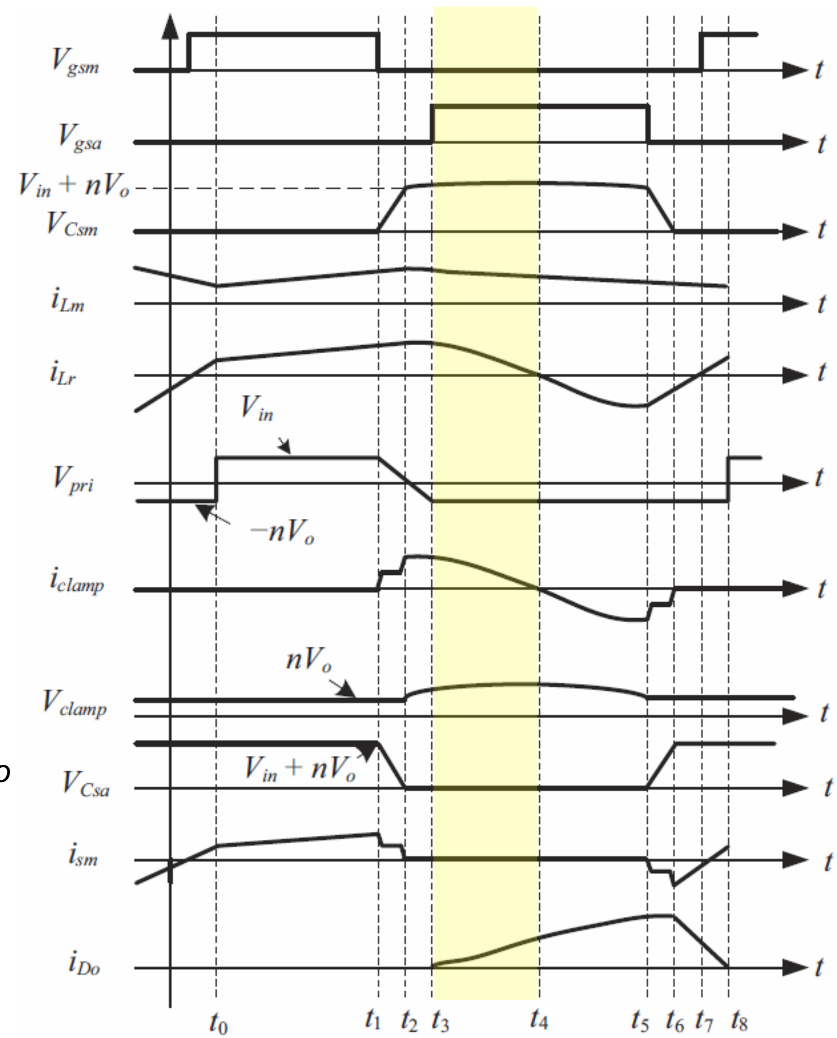
Active Clamp Flyback CCM – t_3~t_4





- **State 4 (Start power deliver interval):**
  - S_a conduct with ZVS
  - $i_{Lm} > i_{Lr} > 0$, $i_{clamp} > 0$, V_{clamp} rising
  - D_o conduct with $i_{Lm}-i_{Lr}>0, V_{Lm} = N_1/N_2 * V_o$
    L_r *resonant with* C_{clamp}
    Energy transfer to output
  - $i_{Do}=(i_{Lm}-i_{Lr})*N_1/N_2$

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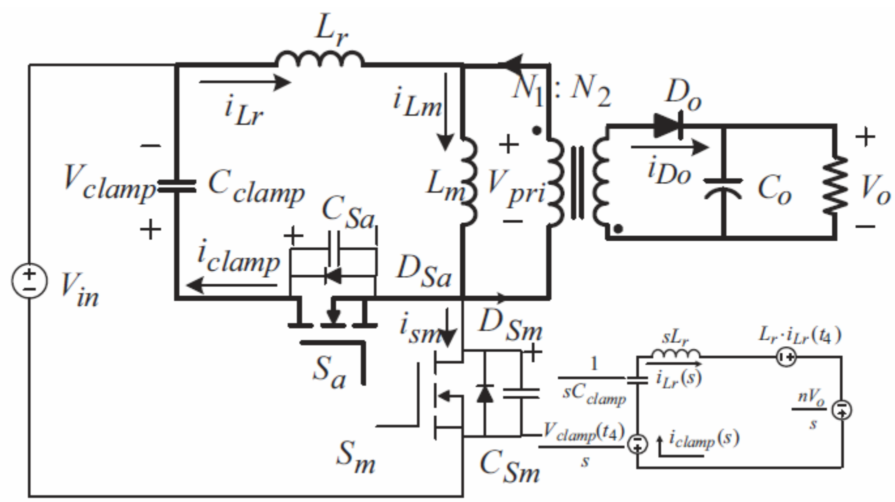
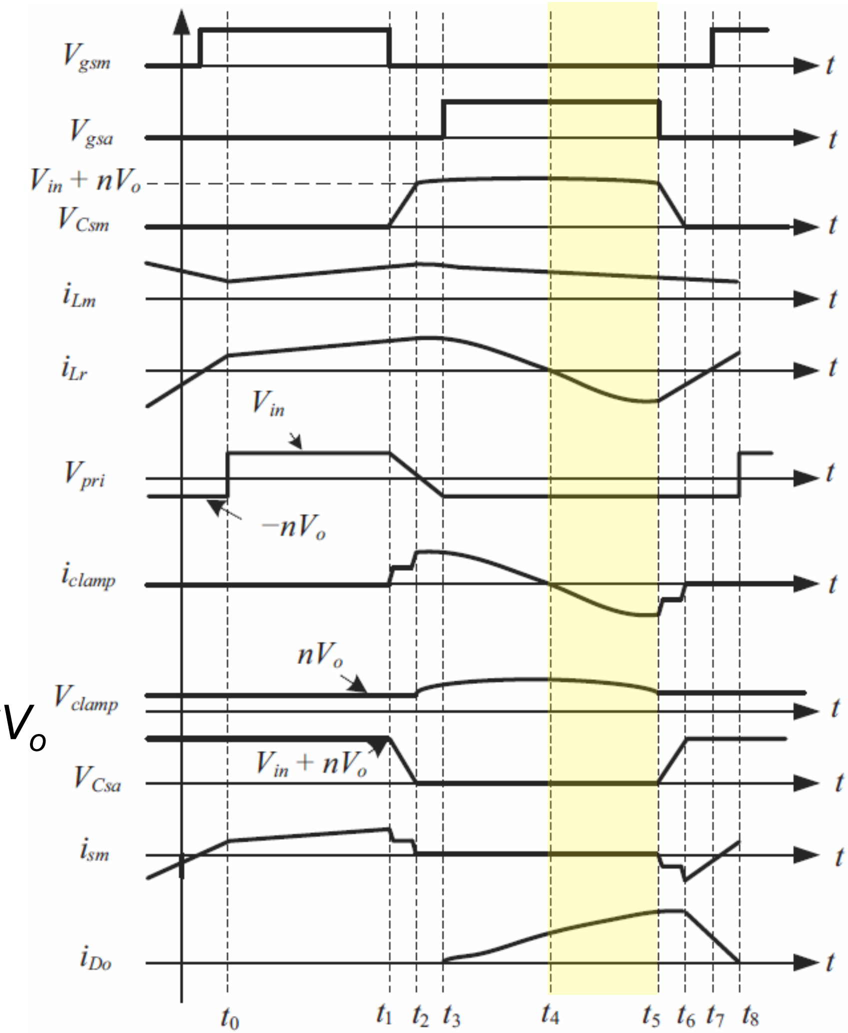
Active Clamp Flyback CCM – t_4~t_5





- **State 5 (Power deliver interval):**
  - $i_{Lm}>0>i_{Lr}$, $\boldsymbol{i_{Lr}<0}$, $i_{clamp}<0$, V_{clamp} falling
  - D_o conduct with $i_{Lm}-i_{Lr}>0, V_{Lm}=N_1/N_2*V_o$
    L_r resonant with C_{clamp}
    Energy transfer to output
  - $i_{Do}=(i_{Lm}-i_{Lr})*N_1/N_2$
  - *Notice the* $\boldsymbol{i_{Do}>=i_{Lm}*N_1/N_2}$

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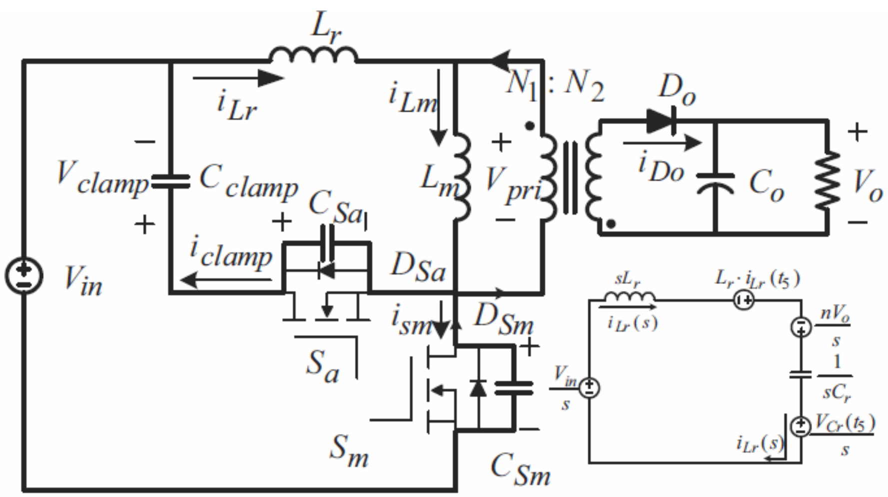
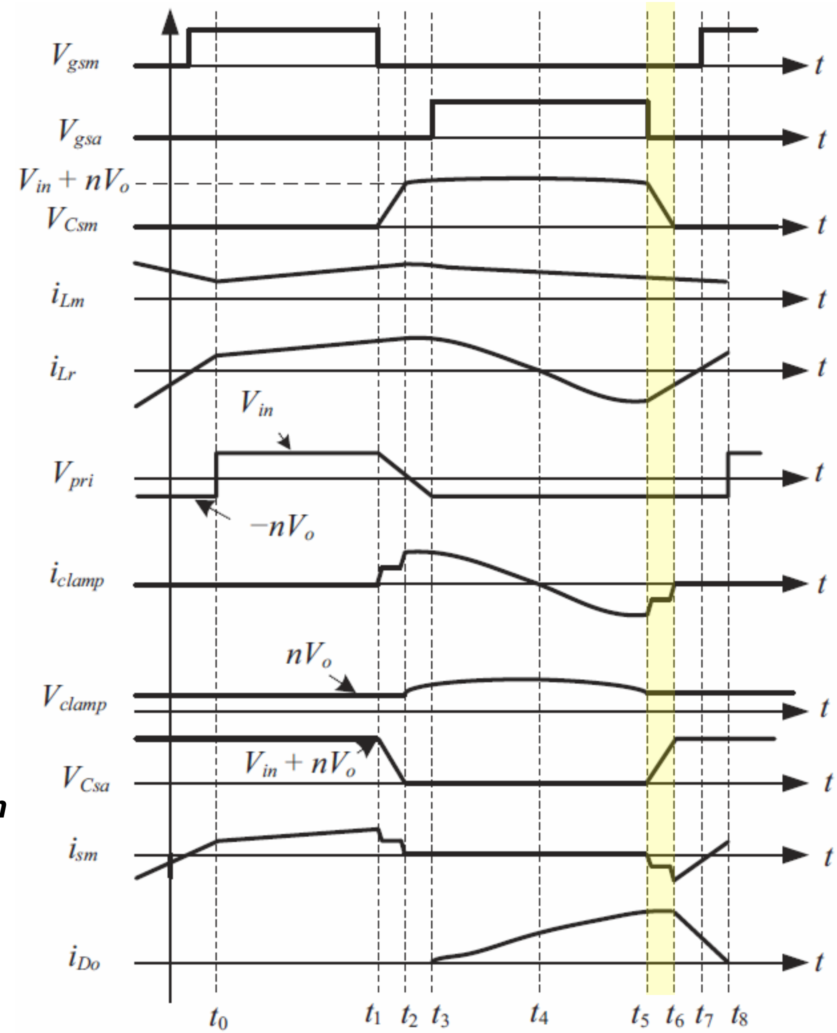
Ching-Lung Chu* Chao-Chung Huang, Department of Electrical Engineering Southern Taiwan University of Science and Technology ,Tainan City, Taiwan 710, R.O.C

Active Clamp Flyback CCM – t_5~t_6

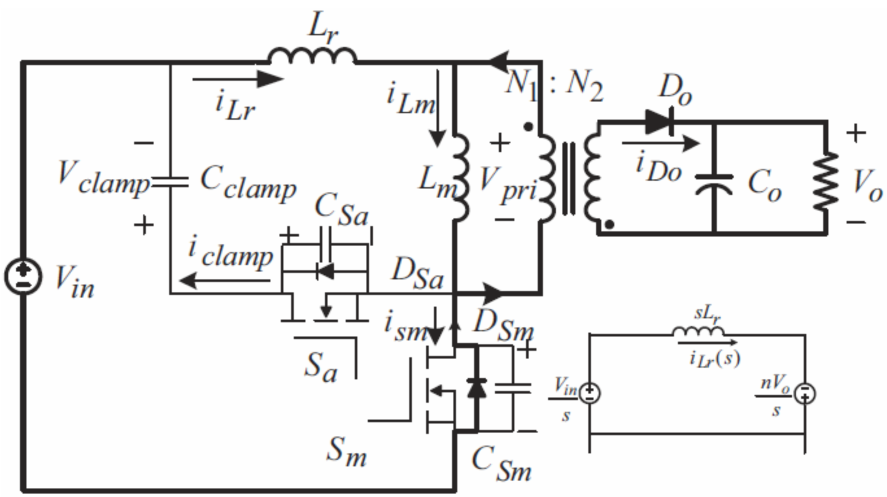


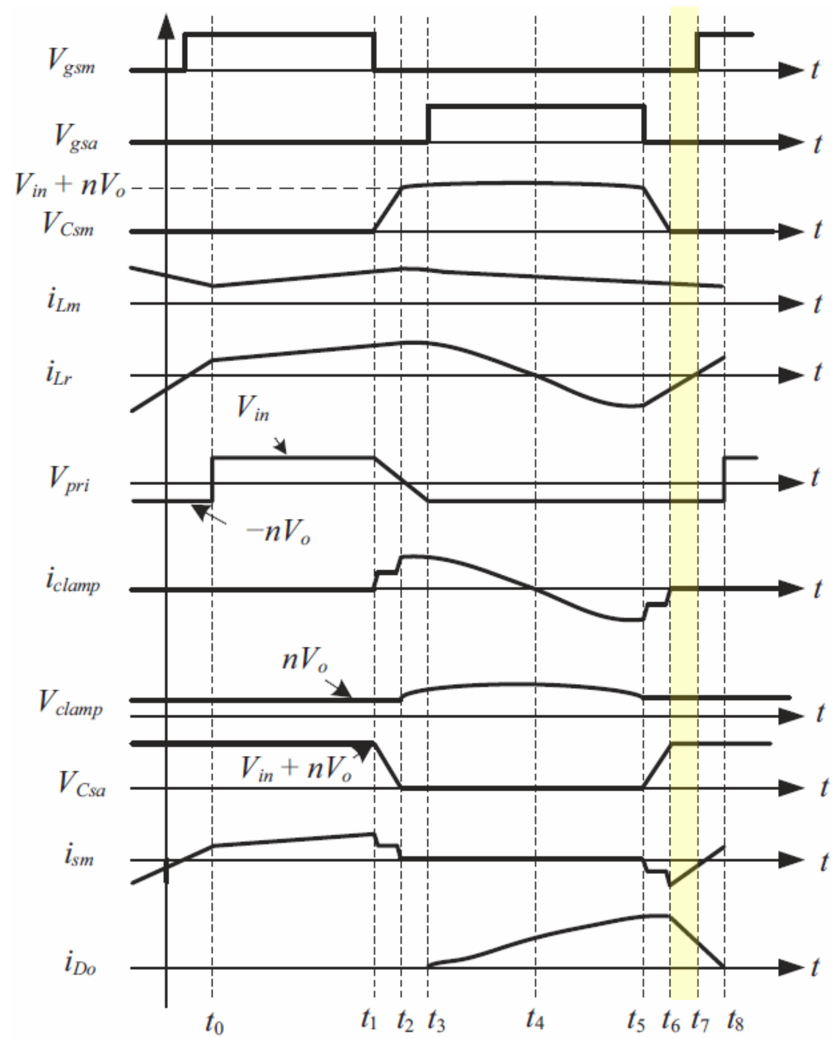


- **State 6 (Resonant interval):**
  - Sa turns off
  - L_r, C_{Sm}, C_{Sa}, C_{clamp} start to resonant.
  - $i_{Lm} > 0 > i_{Lr}$, ***$i_{Lr}<0$, $i_{sm}<0$, discharge C_{sm}***
  - Energy still deliver to output,
  - $i_{Do}=(i_{Lm}-i_{Lr})*N_1/N_2$

[Ref]: ANALYSIS AND IMPLEMENTATION OF SOFT SWITCHING FLYBACK CONVERTER WITH AN ACTIVE CLAMP CIRCUIT
Ching-Lung Chu* Chao-Chung Huang, Department of Electrical Engineering Southern Taiwan University of Science and Technology ,Tainan City, Taiwan 710, R.O.C

Active Clamp Flyback CCM – t_6~t_7

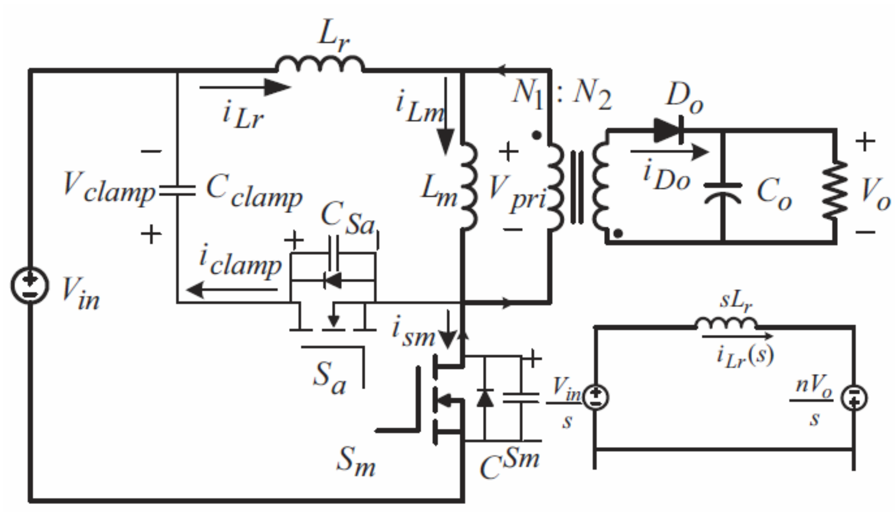


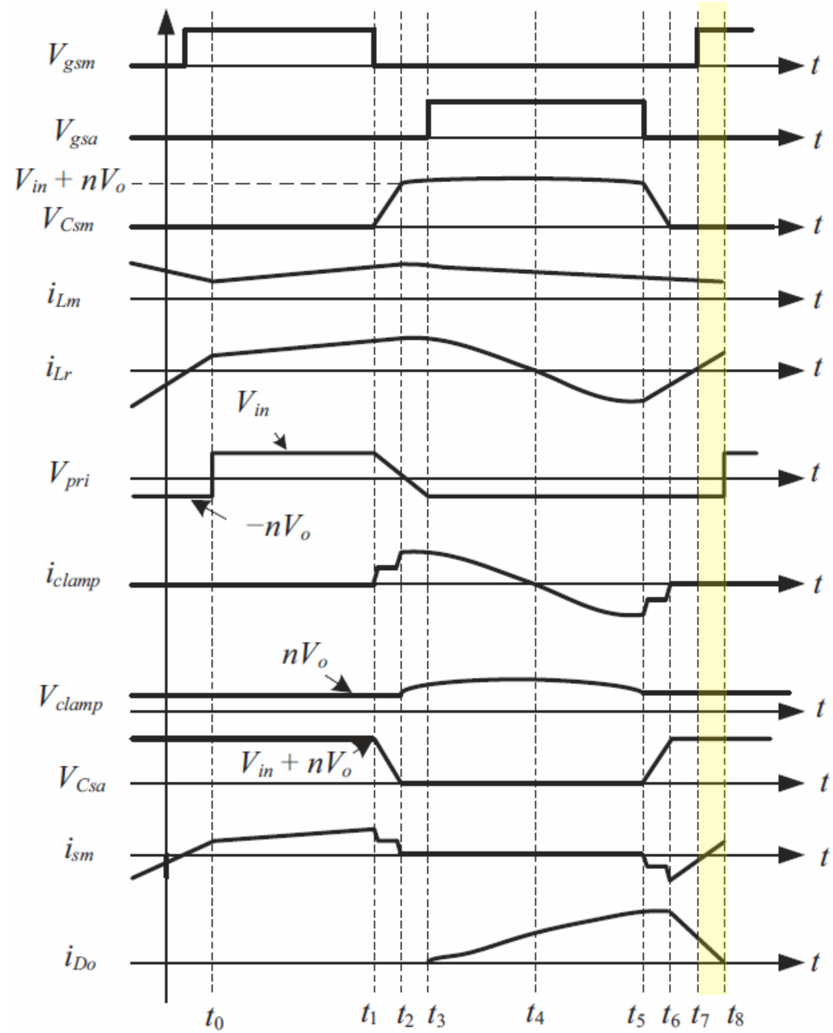


- **State 7 (ZVS interval):**
  - D_{Sm} conduct.
  - i_{Lr} increase rapidly, i_{Lm} still decrease
  - i_{Do}>0, D_o still conduct
  - Still transfer energy to output, but i_{Do} linearly decrease

[Ref]: ANALYSIS AND IMPLEMENTATION OF SOFT SWITCHING FLYBACK CONVERTER WITH AN ACTIVE CLAMP CIRCUIT
Ching-Lung Chu* Chao-Chung Huang, Department of Electrical Engineering Southern Taiwan University of Science and Technology ,Tainan City, Taiwan 710, R.O.C

Active Clamp Flyback CCM – t_7~t_8





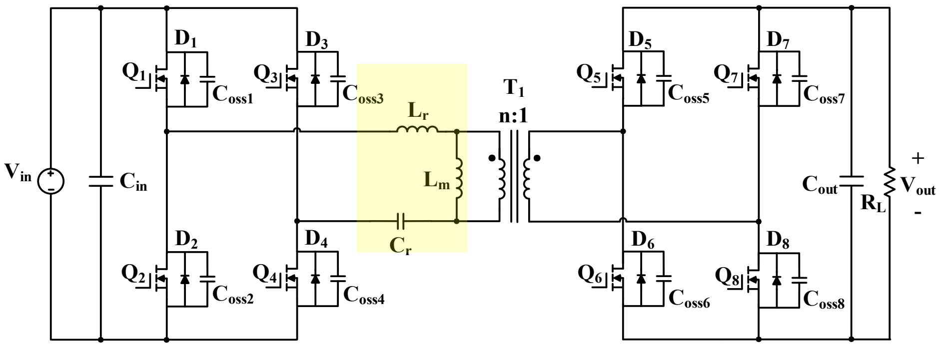
- State 8:
  - S_m conduct with ZVS
  - D_o turns off when $i_{Lr}=i_{Lm}$
  - $V_{in}-(N_1/N_2)V_o=L_r*di_{Lr}/dt$

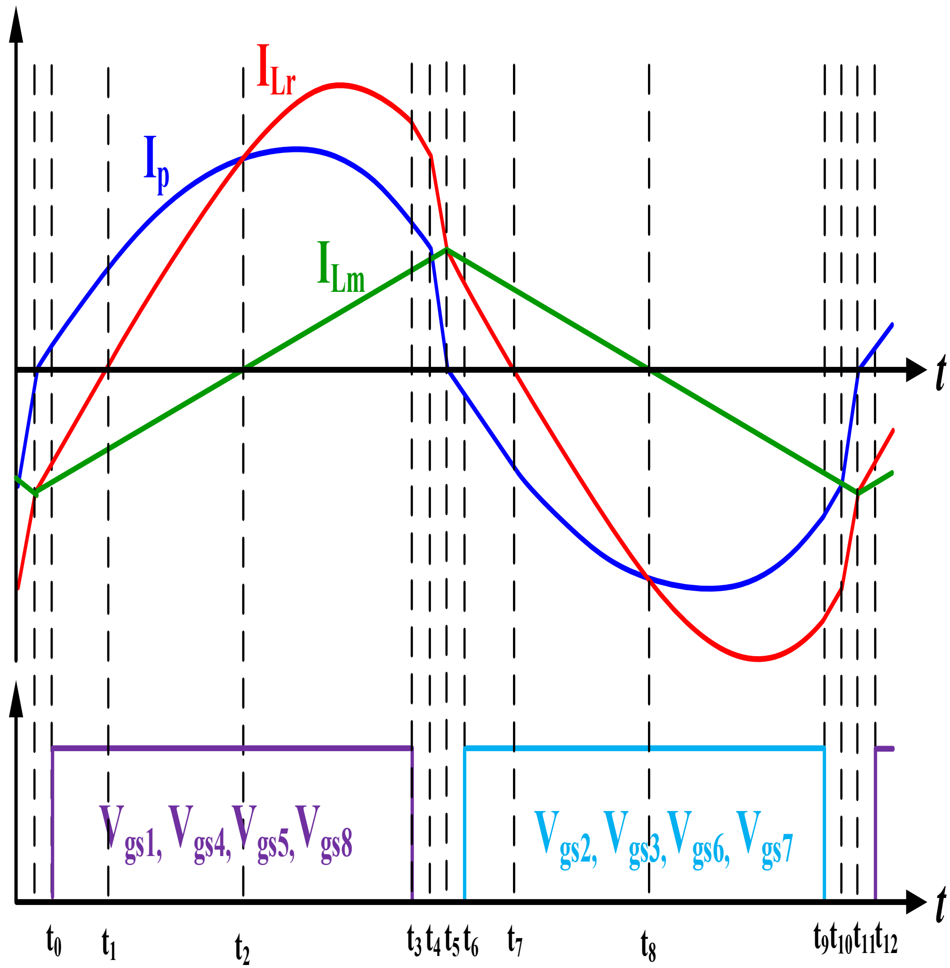
[Ref]: ANALYSIS AND IMPLEMENTATION OF SOFT SWITCHING FLYBACK CONVERTER WITH AN ACTIVE CLAMP CIRCUIT
Ching-Lung Chu* Chao-Chung Huang, Department of Electrical Engineering Southern Taiwan University of Science and Technology ,Tainan City, Taiwan 710, R.O.C

Course outline – Week 5

- **Introduction of Zero Voltage Switching / Zero Current Switching technology**
  - Review the switching characteristics and the reasons for adopting ZVS or ZCS
  - The basic principle to realize ZVS
- **Common methods to implement ZVS**
  - Triangular Current Mode, TCM
  - Zero Voltage Transition, ZVT
  - Quasi-Resonant Converter, QRC
  - Active-Clamp
  - Resonant Converter
  - Dual Active Bridge, DAB
  - Phase-Shift Full Bridge, PSFB

Resonant Converter
(Choose LLC converter for example)





Advantage:

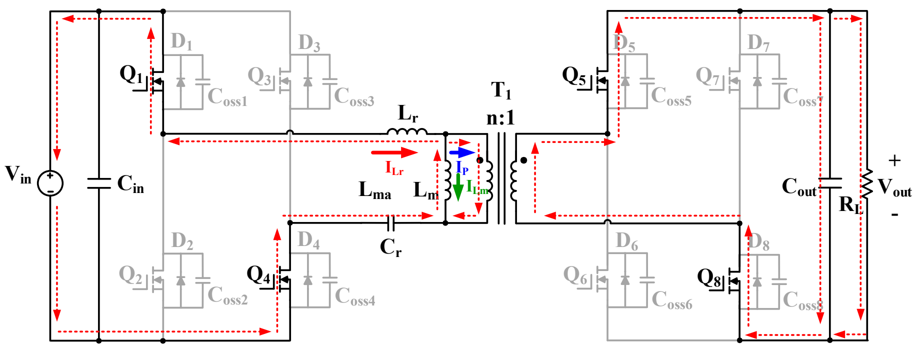
1. Switch with ZVS, rectifier with ZCS (LLC Mode), increase converter efficiency.
2. LLC converter can still maintain the switches ZVS at light load (LLC uses resonant inductor current to achieve zero voltage switching)

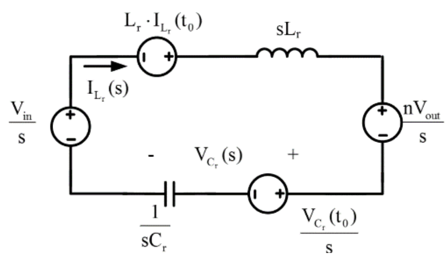
Shortcoming:

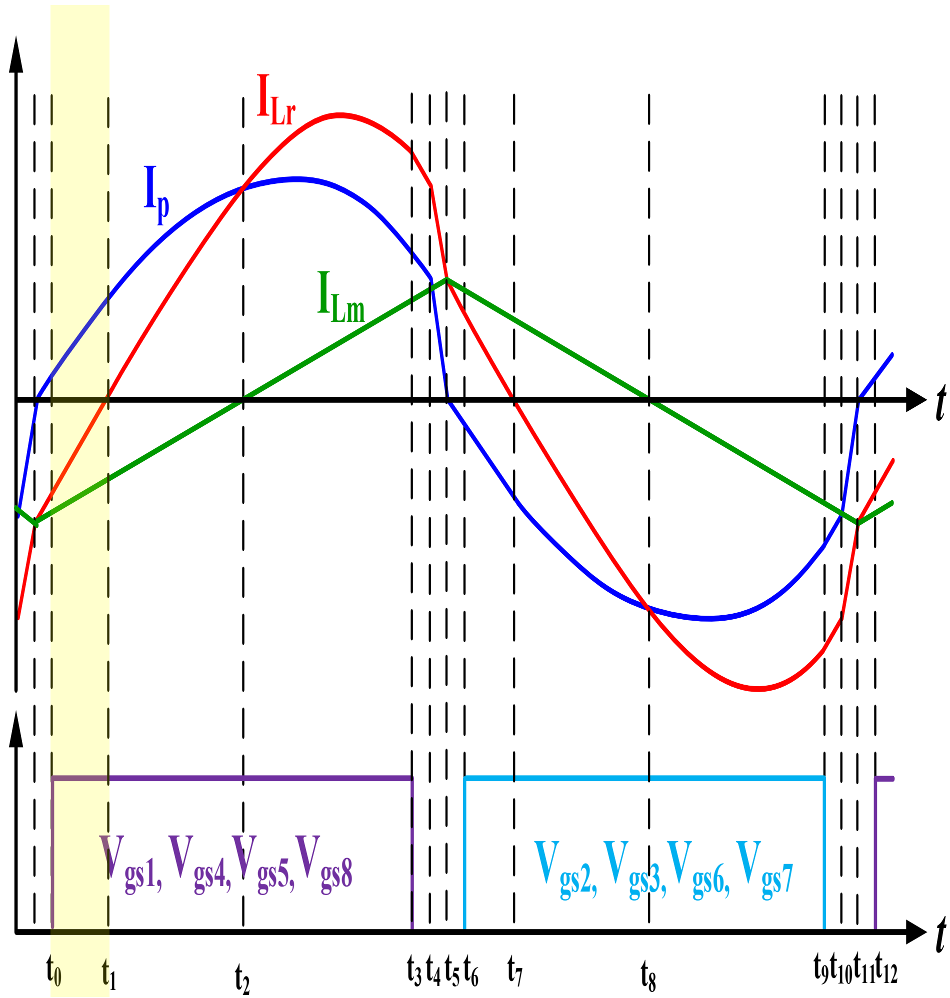
1. The characteristics of the converter are not easy to design in a wide range of input and output applications
2. The frequency conversion control is purely used, and the switching frequency needs to be increased at light load to reduce the converter efficiency
3. Controller must note that the converter must not enter the impedance range of the capacitor, and additional protection is required
4. The rectified current's peak and RMS values are higher, increasing the conduction loss and voltage ripple.
5. Variable frequency control

[Ref]:對稱諧振槽之18kW高功率密度雙向轉換器研製,蔡立勛, 台灣科技大學電子系, 108學年

LLC Converter – t_0~t_1





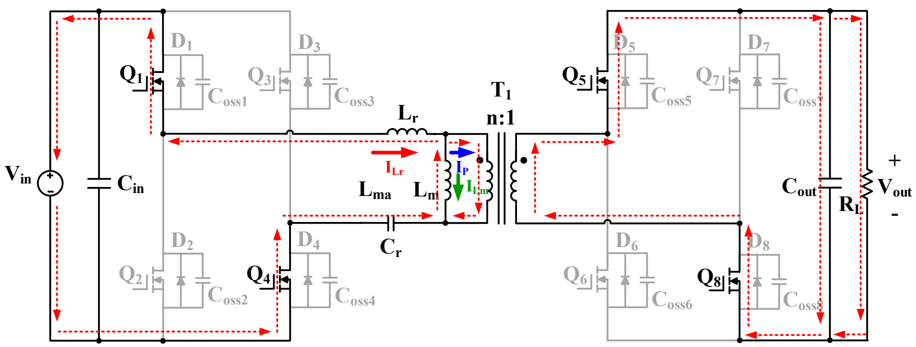


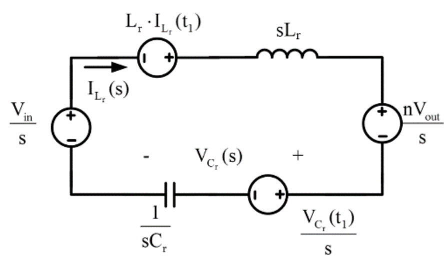
Interval 1 (t_0~t_1):

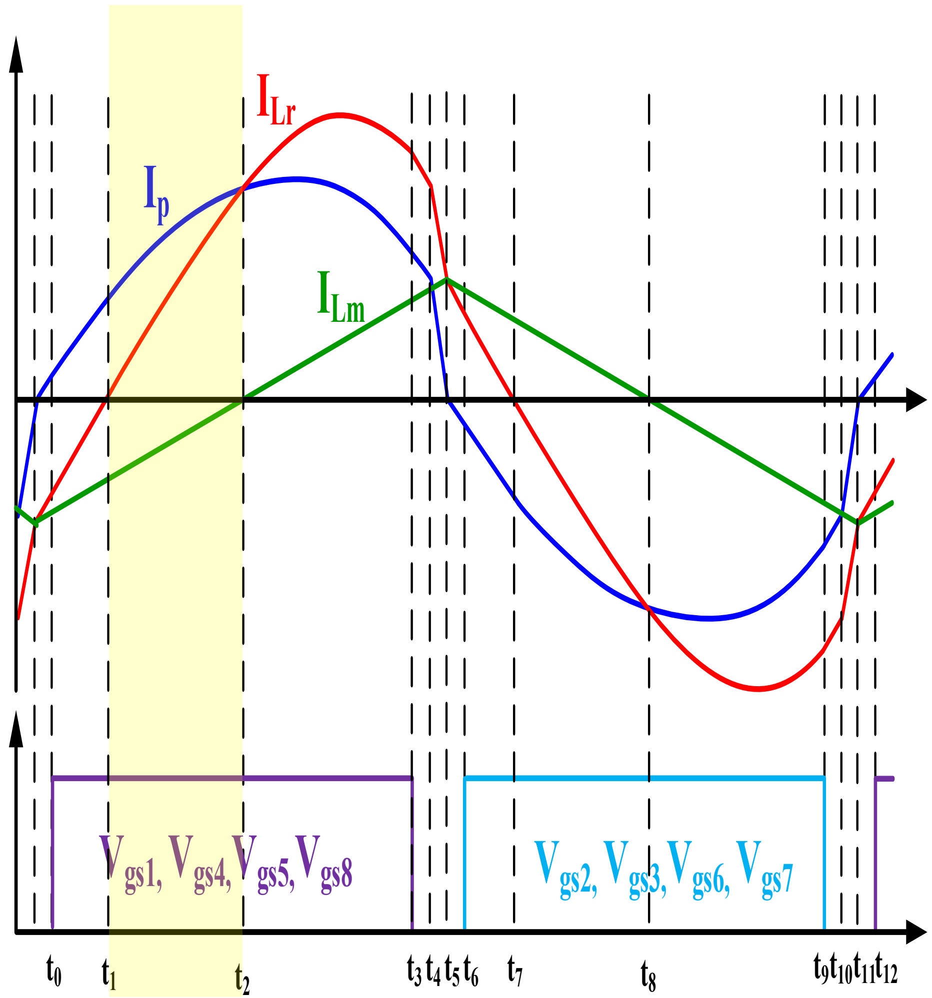
1. $i_{Lm}(t_0)=i_{Lr}(t_0)<0$
2. $v_{Lm}=nV_{out}$, $i_{Lm}(t)$ increase linearly
3. $i_p(t)=i_{Lr}(t)-i_{Lm}(t)$, power delivery

[Ref]:對稱諧振槽之18kW高功率密度雙向轉換器研製,蔡立勛, 台灣科技大學電子系, 108學年

LLC Converter – t_1~t_2





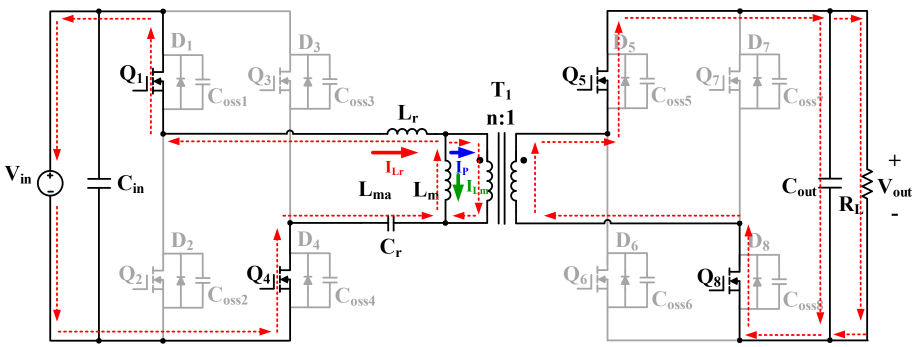


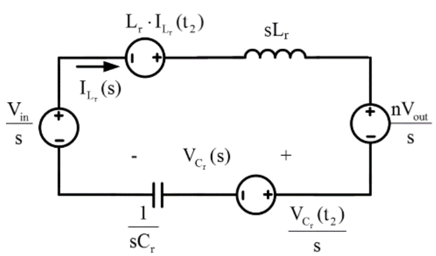
Interval 2 (t_1~t_2):

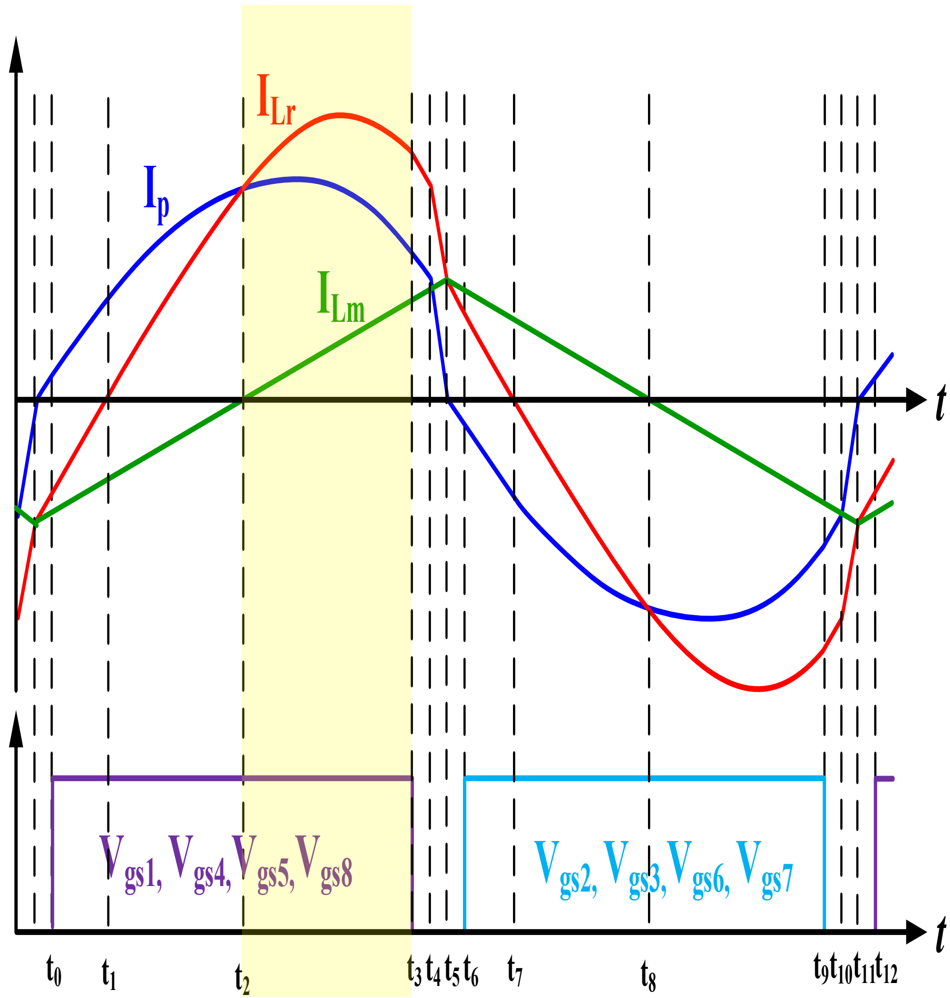
1. $i_{Lm}(t_1)<0,\ i_{Lr}(t_1)=0$
2. $v_{Lm}=nV_{out},\ i_{Lm}(t)$ increase linearly
3. $i_p(t)=i_{Lr}(t)-i_{Lm}(t)$, power delivery
4. $i_{Lm}(t_2)=0$, The polarity of i_{Lm} start to reverse

[Ref]:對稱諧振槽之18kW高功率密度雙向轉換器研製,蔡立勛, 台灣科技大學電子系, 108學年

LLC Converter – t_2~t_3





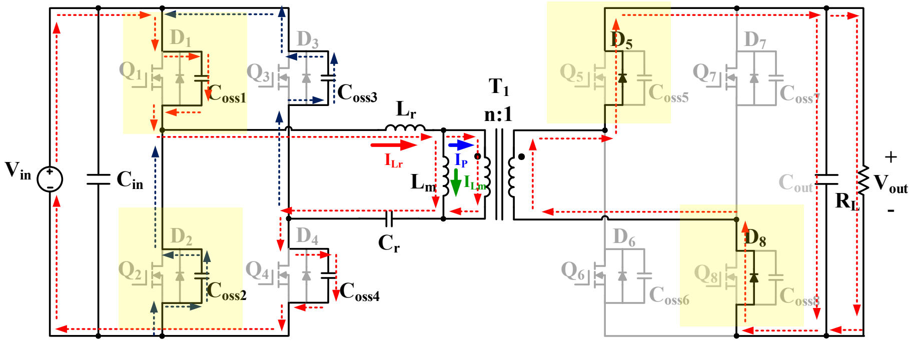


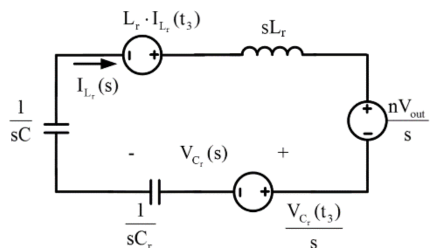
Interval 3 (t_2~t_3):

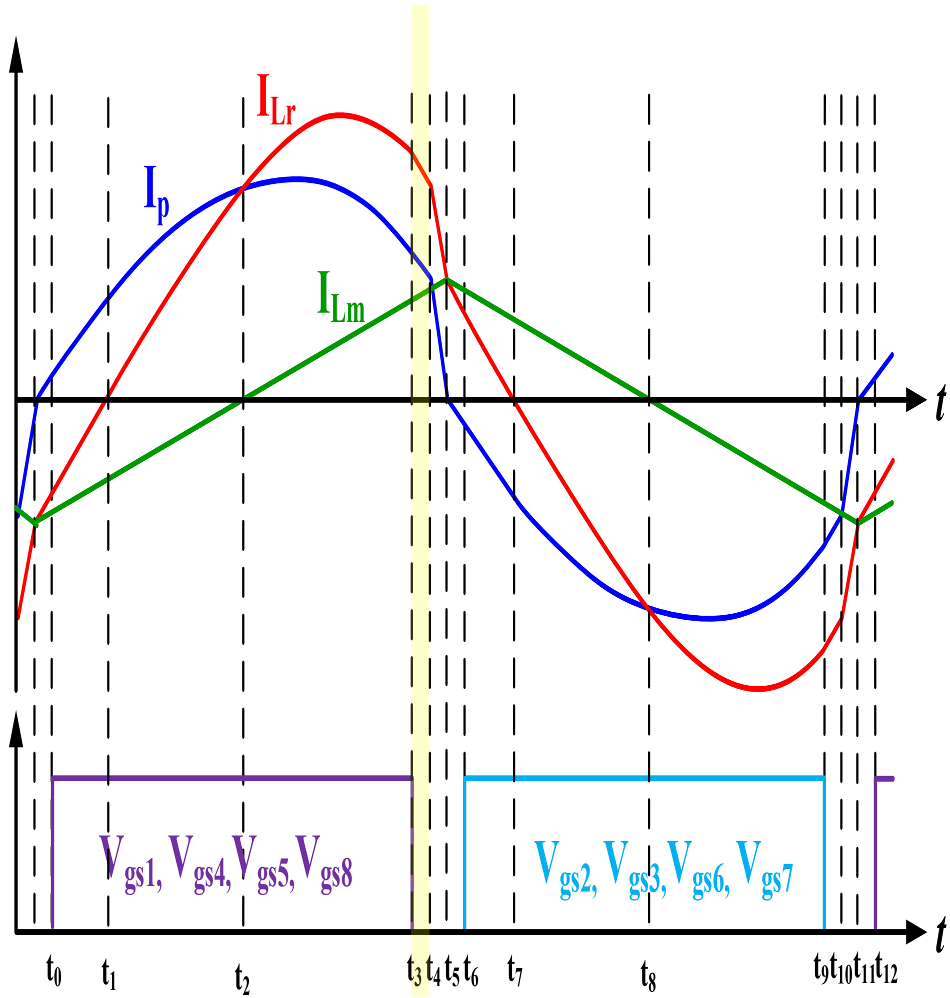
1. *PWM turns off @ $t=t_3$*
2. $v_{Lm}=nV_{out}$, $i_{Lm}(t)$ increase linearly
3. $i_p(t)=i_{Lr}(t)-i_{Lm}(t)$, power delivery

[Ref]:對稱諧振槽之18kW高功率密度雙向轉換器研製,蔡立勛, 台灣科技大學電子系, 108學年

LLC Converter – $t_3 \sim t_4$





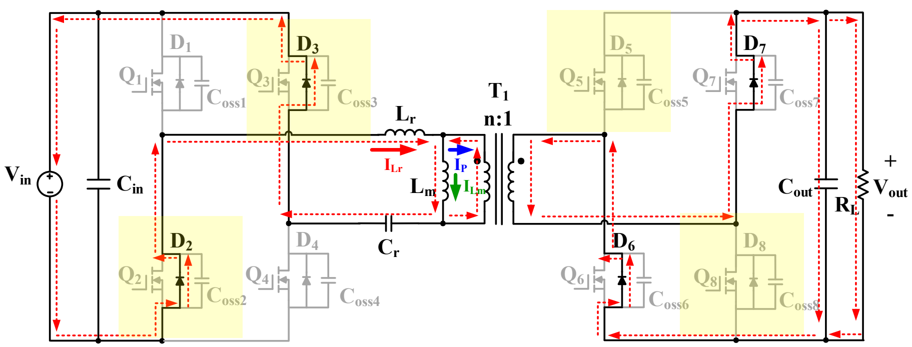


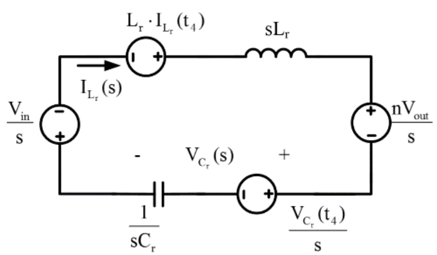
Interval 4 ($t_3 \sim t_4$):

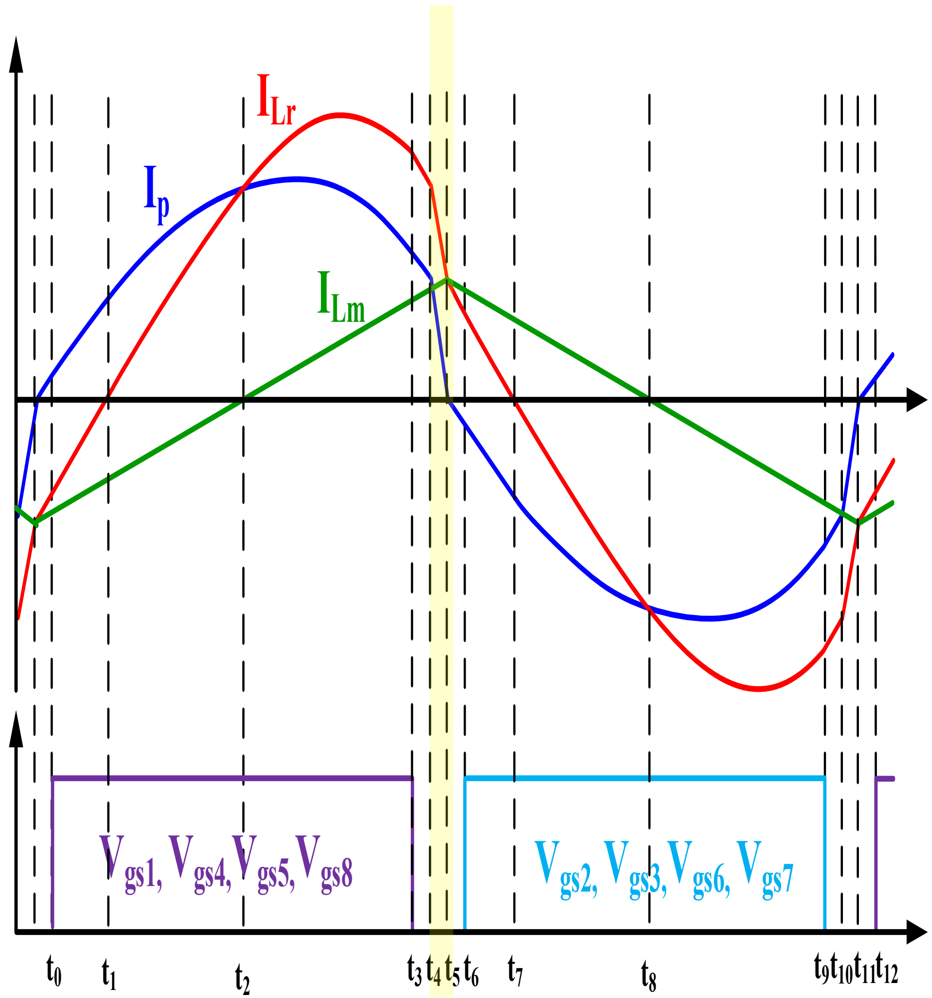
1. *PWM turns off @ $t=t_3$, dead time interval*
2. *$i_p(t)>0$, D_5,D_8 conduct naturally*
3. $v_{Lm}=nV_{out}$, $i_{Lm}(t)$ increase linearly
4. C_{oss}, L_r, C_r start resonant
5. *$i_{Lr}(t_3)>0$, Charge C_{oss1}, discharge C_{oss2}*

[Ref]:對稱諧振槽之18kW高功率密度雙向轉換器研製,蔡立勛, 台灣科技大學電子系, 108學年

LLC Converter – t_4~t_5





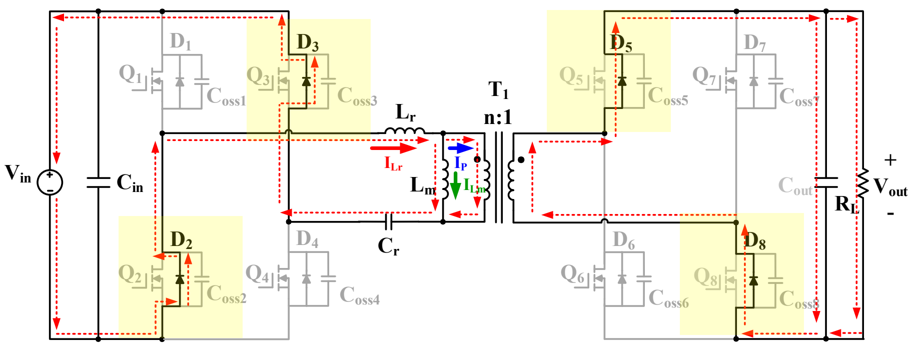


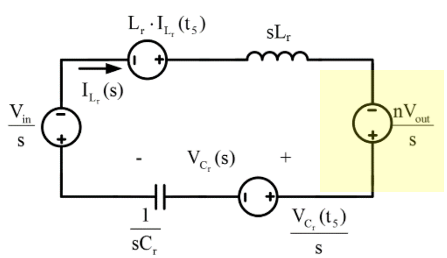
Interval 4 (t_4~t_5):

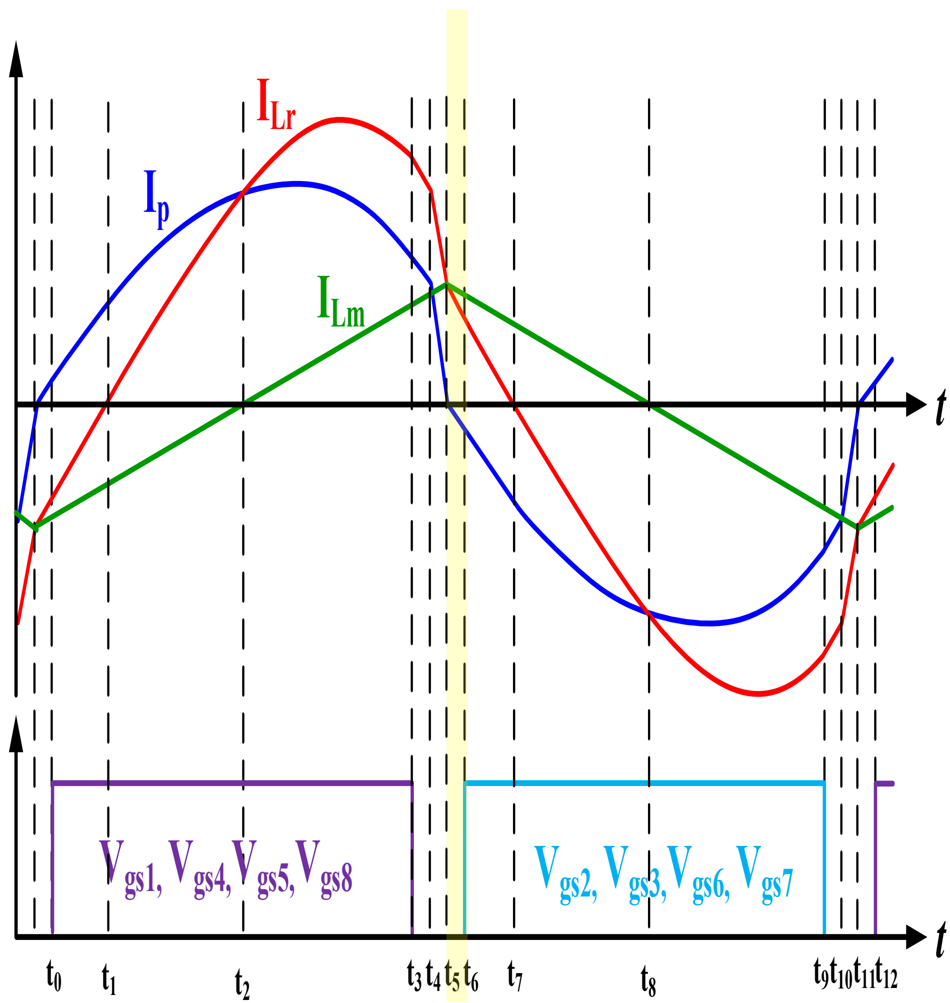
1. *Body diode D_2 D_3 conduct*
2. *Primary side resonant tank input voltage reverse*
3. *iLr(t) decreases significantly*
4. *$i_p(t)>0$, D_5,D_8 conduct naturally*
5. *$v_{Lm}=nV_{out}$, $i_{Lm}(t)$ increase linearly*
6. *Interval ends with $i_p(t_5)=0A$*

[Ref]:對稱諧振槽之18kW高功率密度雙向轉換器研製,蔡立勛, 台灣科技大學電子系, 108學年

LLC Converter – t_5~t_6





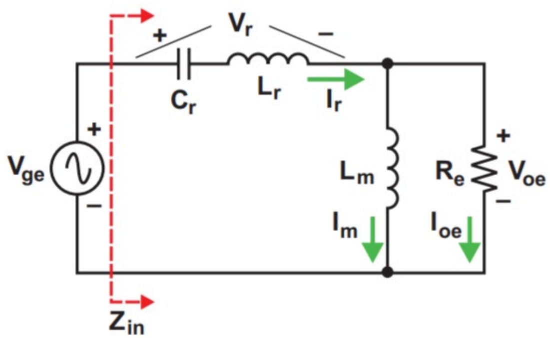


Interval 5 (t_5~t_6):

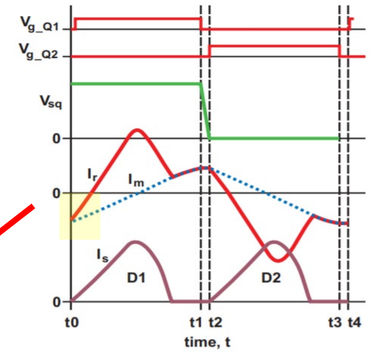
1. $i_{Lr}(t)<i_{Lm}(t)$, $i_P(t)<0$ (ignore $C_{oss5,6,7,8}$ resonant period)
2. Secondary side D_6 D_7 conduct naturally
3. $v_{Lm}= -nV_{out}$, $i_{Lm}(t)$ decrease linearly
4. $i_p(t)=i_{Lr}(t)-i_{Lm}(t)$, power delivery

[Ref]:對稱諧振槽之18kW高功率密度雙向轉換器研製,蔡立勳, 台灣科技大學電子系, 108學年

The relationship with ZVS & input impendence



a. Input impedance.

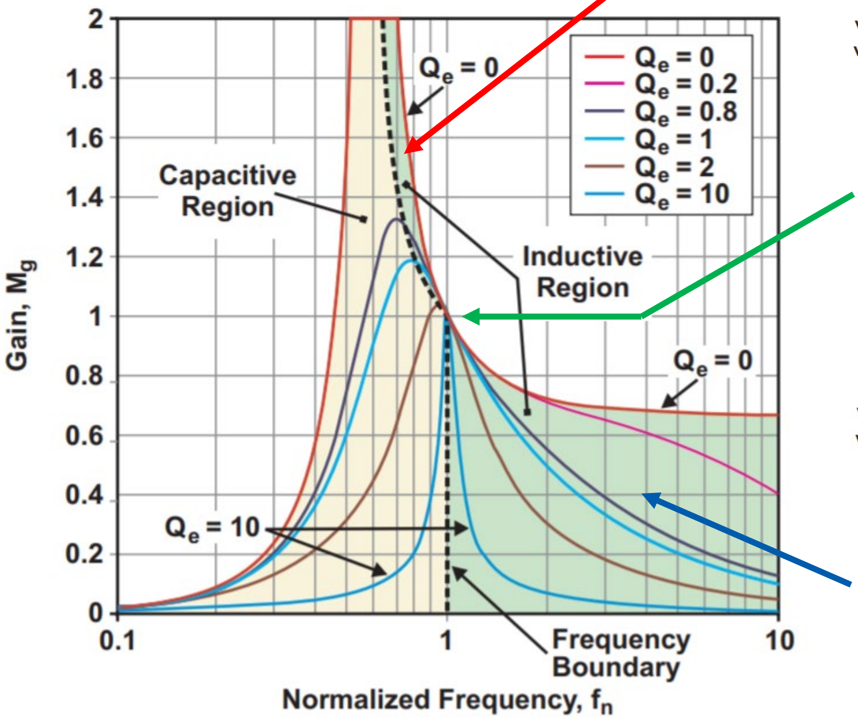


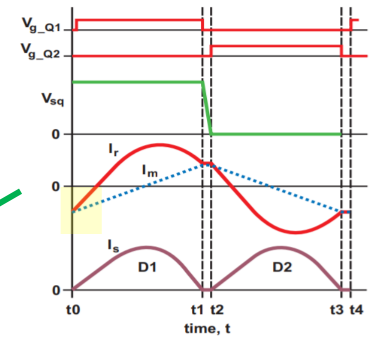
b. Below f_0.

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_e}.$$

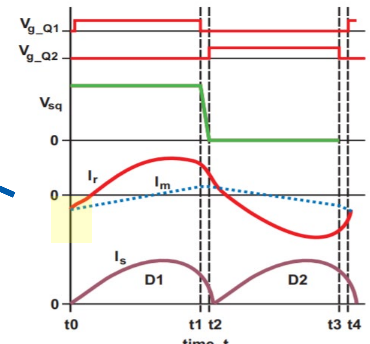
$$R_e = \frac{V_{oe}}{I_{oe}} = \frac{8\times n^2}{\pi^2}\times\frac{V_o}{I_o} = \frac{8\times n^2}{\pi^2}\times R_L.$$

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}.$$





a. At f_0.

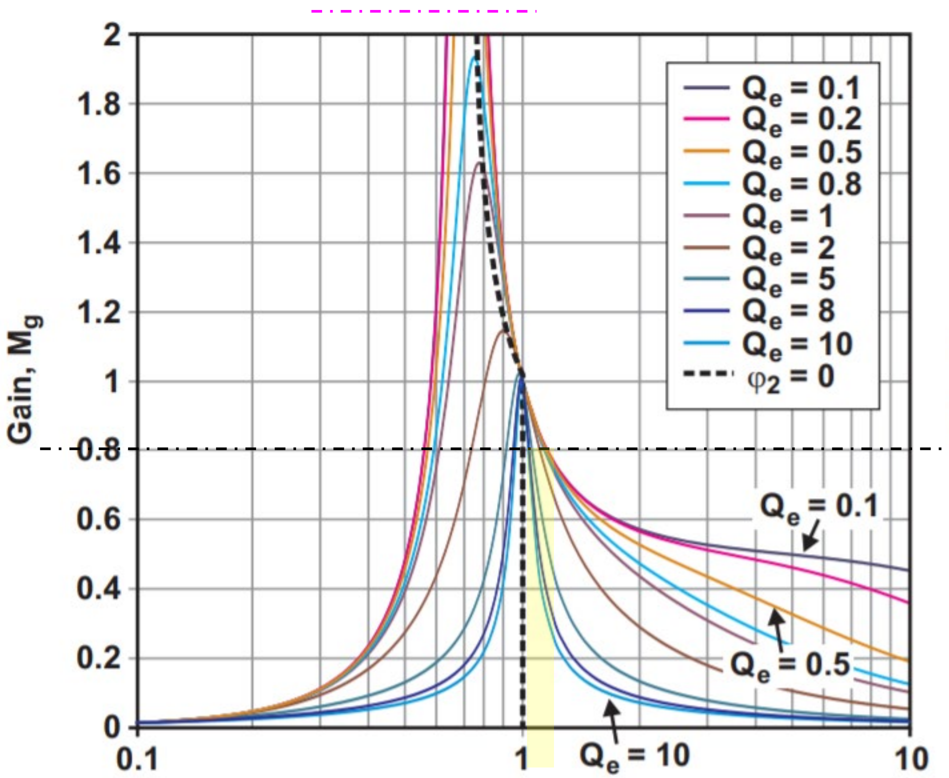


c. Above f_0.

- ZVS occur with inductance impendence
- Do not work@ capacitive region
- The more deviated from the resonance point, the conduction loss increases

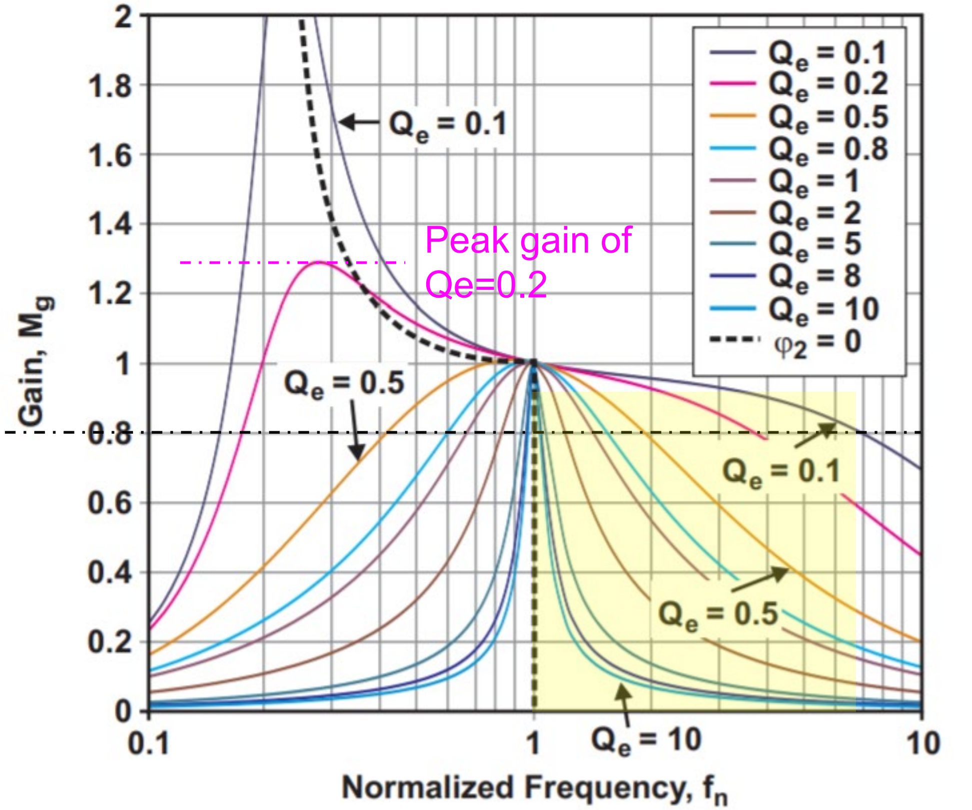
[Ref]: Designing an LLC Resonant Half-Bridge Power Converter, 2010 Texas Instruments Power Supply Design Seminar SEM1900, Topic 3, TI Literature Number: SLUP263

Interpretation of voltage gain curve



$$Q_e = \frac{\sqrt{L_r/C_r}}{R_e}. \quad L_n = \frac{L_m}{L_r}.$$

a. $L_n = 1$.



d. $L_n = 20$.

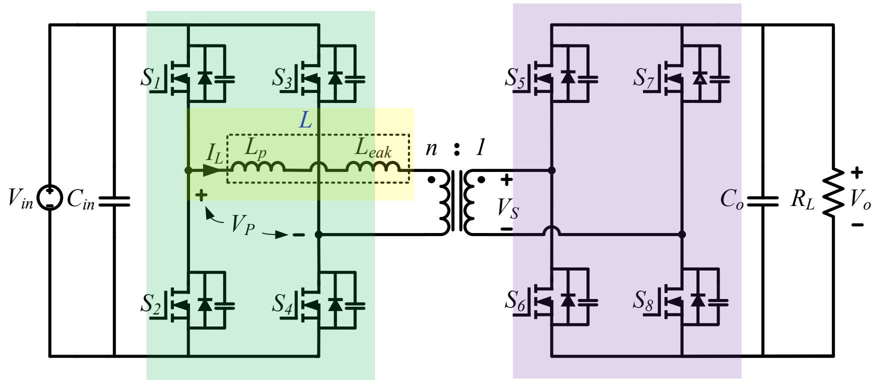
- The smaller the design of L_n, the greater the peak gain of the converter (hold up time requirement)
- The smaller the design of L_n, the narrower the converter's regulated frequency modulation range
- For conduction loss consideration, the greater the Lm, the lower the conduction loss. But for the ZVS range and peak gain of converter requirement, the maximum L_m value should be limited.

[Ref]: Designing an LLC Resonant Half-Bridge Power Converter, 2010 Texas Instruments Power Supply Design Seminar SEM1900, Topic 3, TI Literature Number: SLUP263

Course outline – Week 5

- **Introduction of Zero Voltage Switching / Zero Current Switching technology**
  - Review the switching characteristics and the reasons for adopting ZVS or ZCS
  - The basic principle to realize ZVS
- **Common methods to implement ZVS**
  - Critical conduction Mode, CrM
  - Zero Voltage Transition, ZVT
  - Quasi-Resonant Converter, QRC
  - Active-Clamp
  - Resonant Converter
  - Dual Active Bridge, DAB
  - Phase-Shift Full Bridge, PSFB

Dual Active Bridge Converter, DAB
(Choose Single Phase Shift control for example)

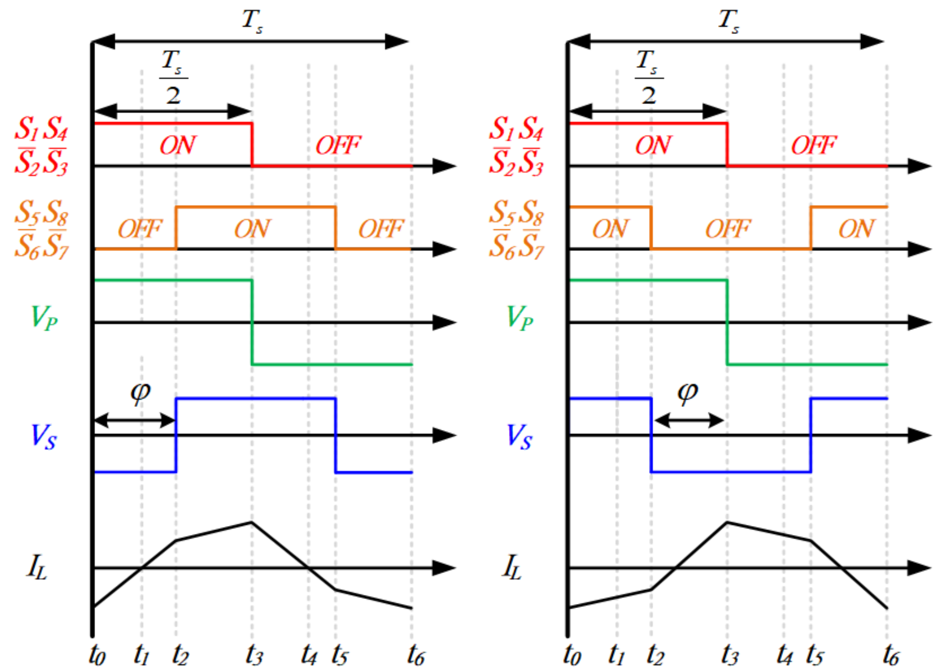


Advantage:

1. Easy bi-directional power flow control
2. Achieve ZVS, but still has the limitation of zero voltage switching conditions
3. Change the phase shift angle to adjust the voltage regulation, and the converter operates at a fixed frequency
4. The RMS value of the switching current is smaller than that of the resonant converter

Shortcoming:

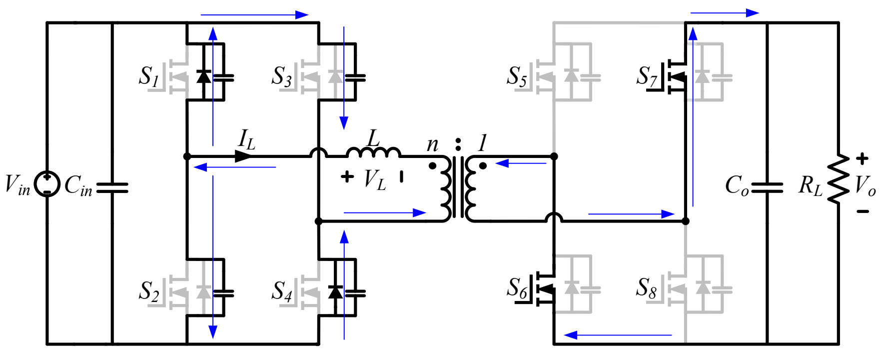
1. Compared with the resonant converter, the rectifier test switch does not have the characteristic of ZCS turns off
2. The cut-off current of the switch is more significant than that of the resonant converter, and the turn off loss is higher
3. When the switch turns off with hard switching, the switch's v_{DS} spike and the interference to the surrounding circuits are relatively large.
4. Zero voltage switching (SPS) is not possible when the voltage conversion ratio is 1.

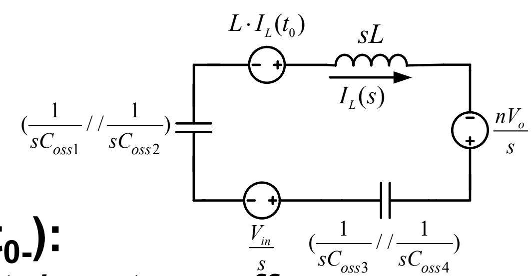


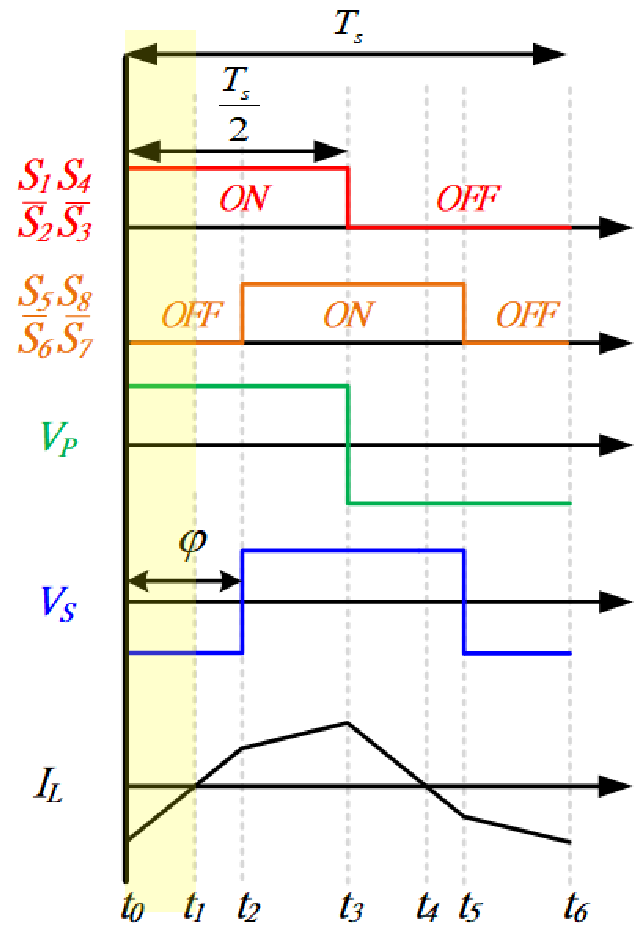
(a) 正功率潮流　　(b) 負功率潮流

[Ref]:應用於車輛之雙主動全橋式轉換器研製,王嘉丞, 台灣科技大學電子系, 109學年

SPS DAB Converter – t_0~t_1







(a) 正功率潮流

Resonant period ($t=t_{0-}$):

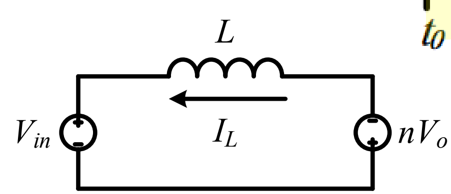
1. *Primary side 4 switches turn off*
2. *$i_{Lr}(t_{0-})<0$, discharge C_{oss} and make body diode conduct.*

ZVS period ($t=t_{0+}$):

1. *S_1, S_4 turn on with ZVS*

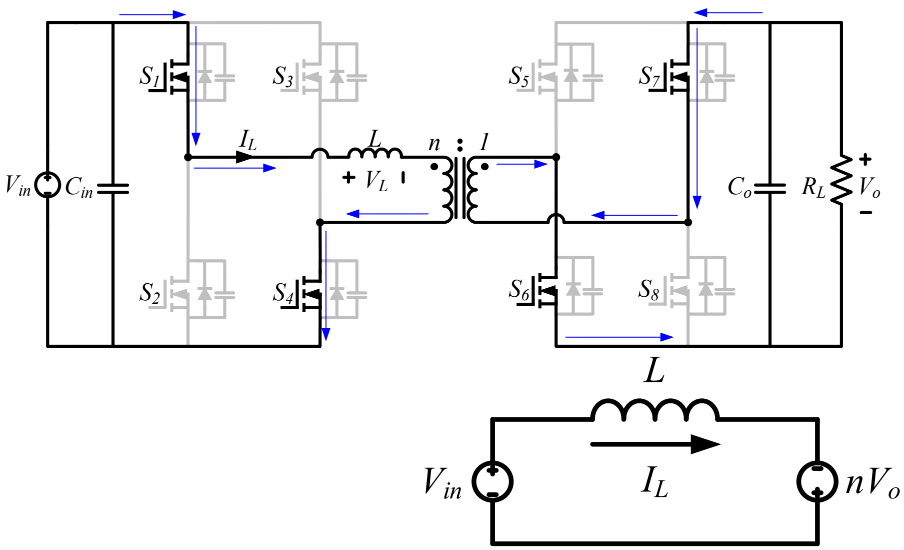
Reactive power period ($t=t_{0+}$~t_1):

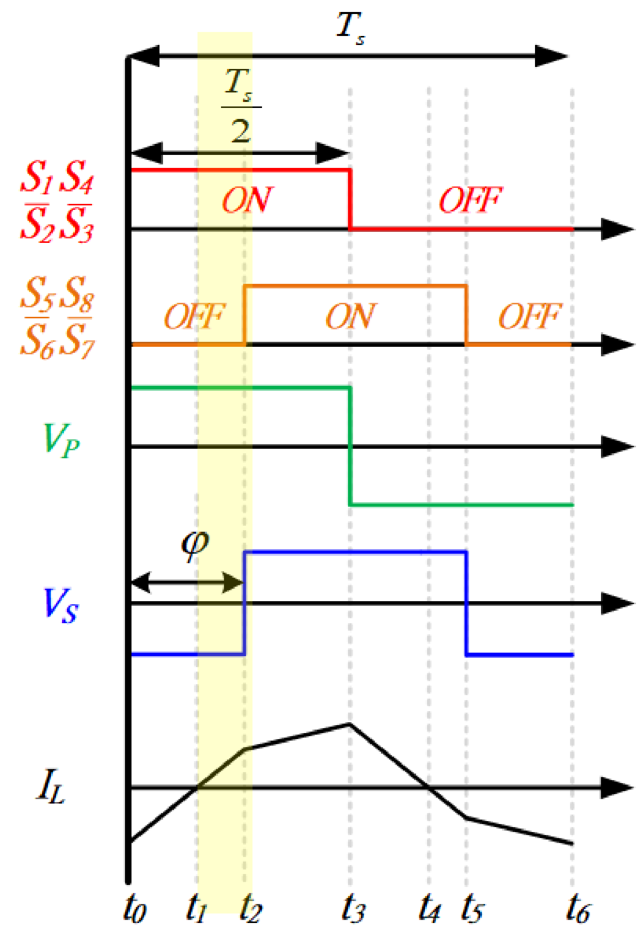
1. *$i_{Lr}(t)<0$, $V_p>0$ ➔ Reactive power*
2. *$V_L=V_{in}+nV_o$, $i_{Lr}(t)$ increase linearly*



[Ref]:應用於車輛之雙主動全橋式轉換器研製,王嘉丞, 台灣科技大學電子系, 109學年

SPS DAB Converter – t_1~t_2





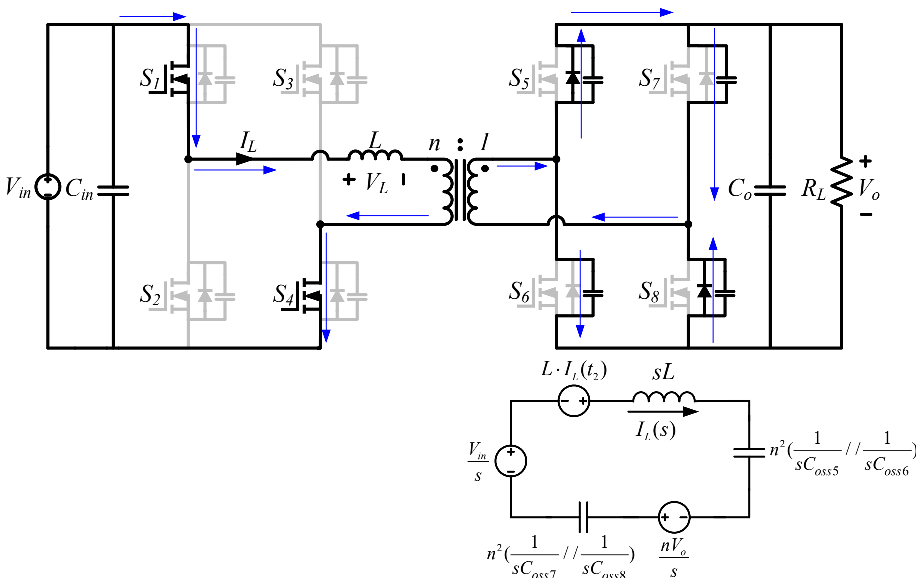
(a) 正功率潮流

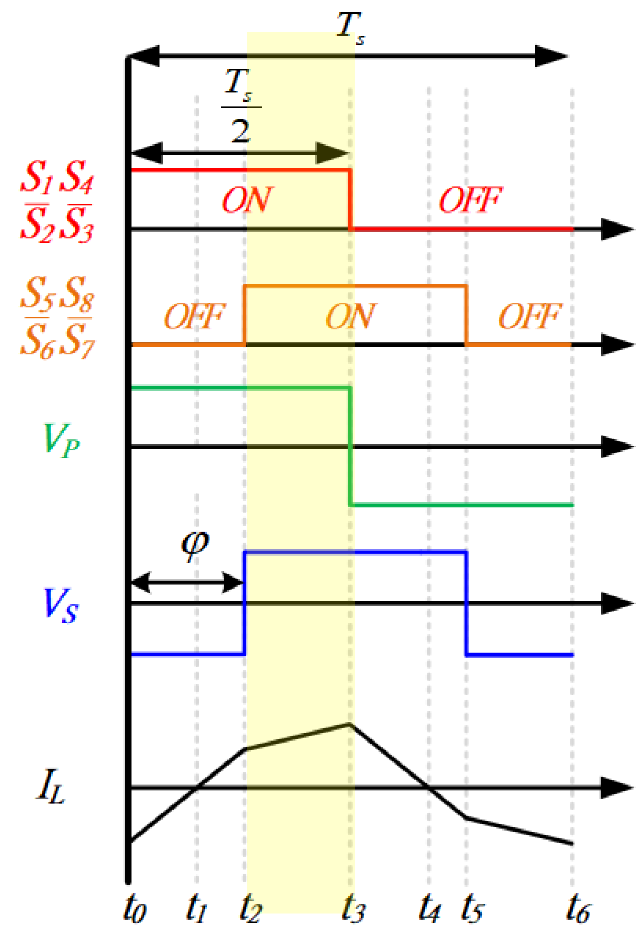
Power delivery period (t_1~t_2):

1. $i_{Lr}(t)>0$, $V_p>0$ ➔ *Real power*
2. $V_L=V_{in}+nV_o$, *$i_{Lr}(t)$ increase linearly*

[Ref]:應用於車輛之雙主動全橋式轉換器研製,王嘉丞, 台灣科技大學電子系, 109學年

SPS DAB Converter – t_2~t_3





(a) 正功率潮流

Resonant period ($t=t_{2-}$):

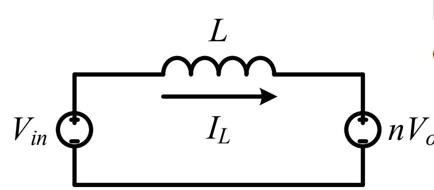
1. *Secondary side 4 switches turn off*
2. *$i_{Lr}(t_{2-})<0$, discharge C_{oss} and make body diode conduct.*

ZVS period ($t=t_{2+}$):

1. *S_5, S_8 turn on with ZVS*

Power delivery period (t_2~t_3):

1. *$i_{Lr}(t)>0$, $V_p>0$ ➔ Real power*
2. *$V_L=V_{in}-nV_o$, $i_{Lr}(t)$ increase linearly*



[Ref]:應用於車輛之雙主動全橋式轉換器研製,王嘉丞, 台灣科技大學電子系, 109學年

The relationship of output power, phase shift angle and proportion of real, reactive power

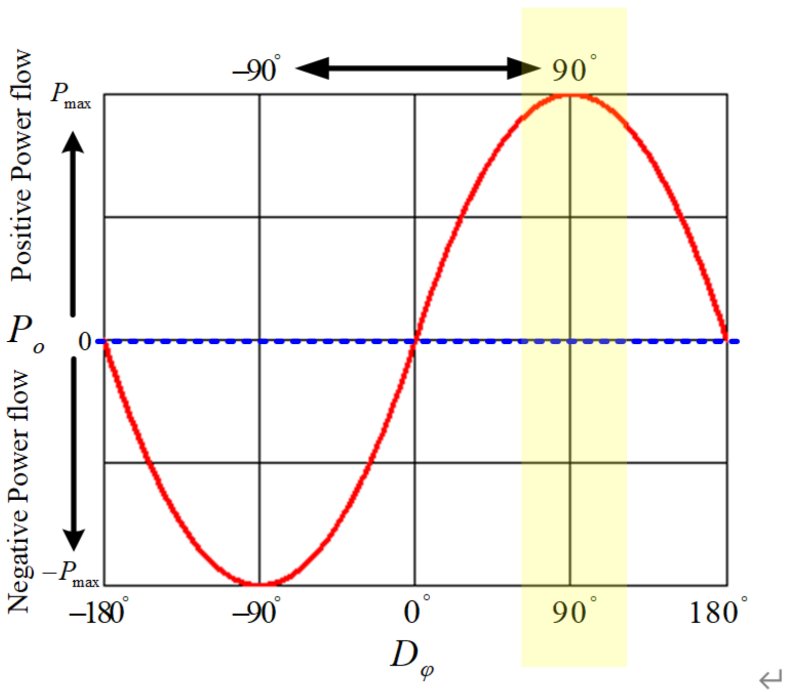


圖 2-7 單相移之輸出功率與相移角度關係圖

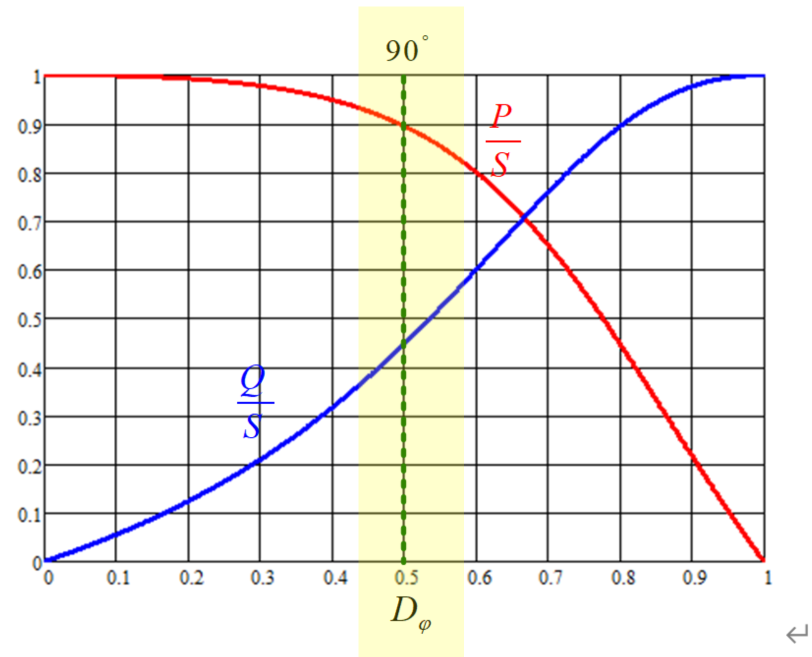


圖 2-8 虛功(Q)、實功(P)與視在功率(S)占比及相移角關係圖

[Ref]:三重相移控制之寬範圍雙主動全橋式電路研製,陳怡瑄, 台灣科技大學電子系, 110學年

Course outline – Week 5

- **Introduction of Zero Voltage Switching / Zero Current Switching technology**
  - Review the switching characteristics and the reasons for adopting ZVS or ZCS
  - The basic principle to realize ZVS
- **Common methods to implement ZVS**
  - Critical conduction Mode, CrM
  - Zero Voltage Transition, ZVT
  - Quasi-Resonant Converter, QRC
  - Active-Clamp
  - Resonant Converter
  - Dual Active Bridge, DAB
  - Phase-Shift Full Bridge, PSFB

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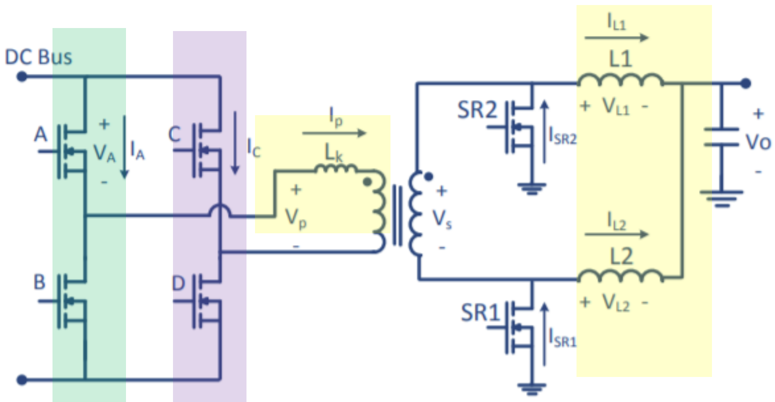
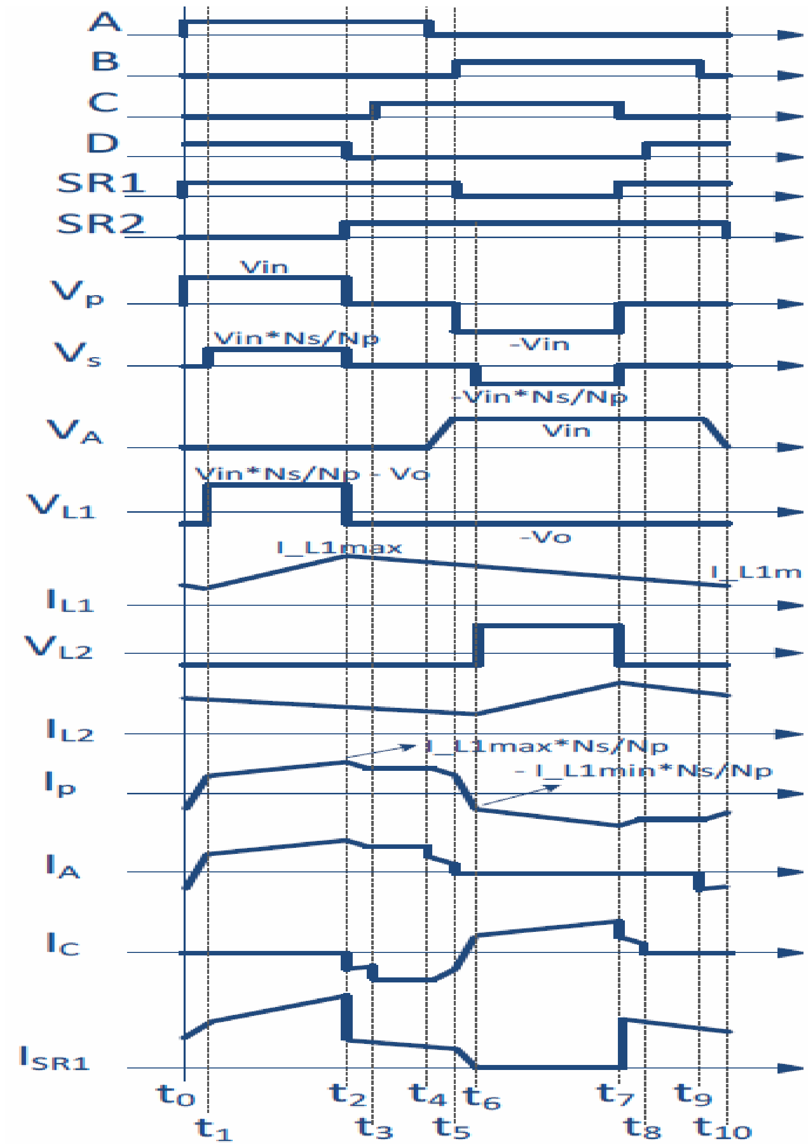
Phase Shift Full Bridge Converter





Advantage:

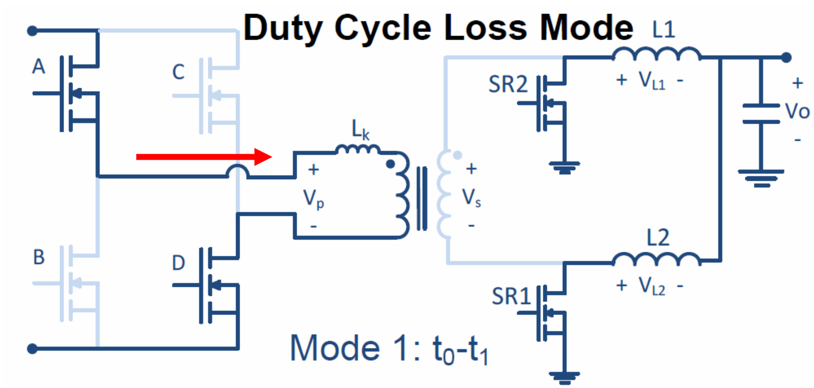
1. The output contains inductance, so the output voltage and current ripple are small
2. ZVS can be achieved but limited by the loading conditions
3. Change the phase shift angle to adjust the voltage regulation, and the converter operates at a fixed frequency
4. The RMS value of the switching current is smaller than that of the resonant converter and DAB converter

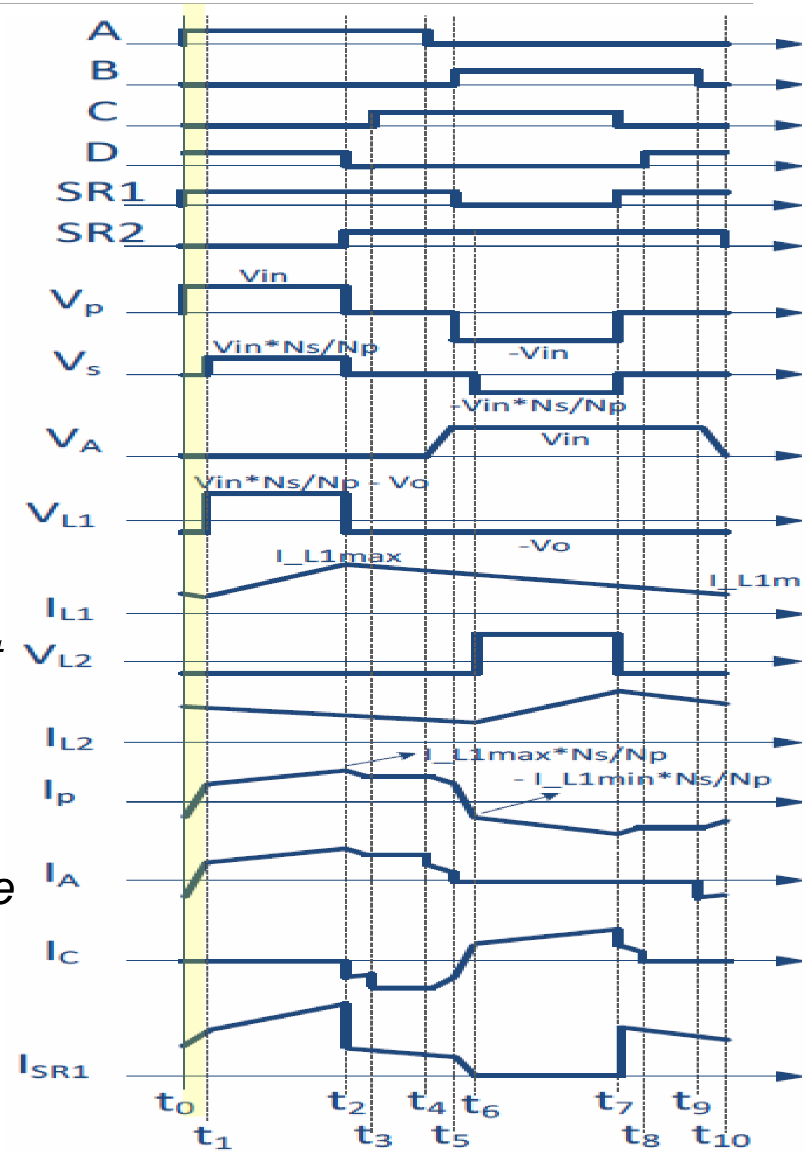
Shortcoming:

1. Compared with the resonant converter, the rectifier test switch does not have the characteristic of zero current switching
2. The cut-off current of the switch is more significant than that of the resonant converter, and the cut-off loss is higher
3. When the switch turns off with hard switching, the switch's v_{DS} spike and the interference to the surrounding circuits are relatively large.
4. The zero voltage switching conditions of the leading arm and the lagging arm are different
5. Trade-off between duty cycle loss and zero voltage switching conditions

[Ref]: Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier, Sam Abdel-Rahman, Infineon Technologies North America (IFNA) Corp Design Note DN 2013-01 V1.0 January 2013

Phase Shift Full Bridge Converter – t_0~t_1



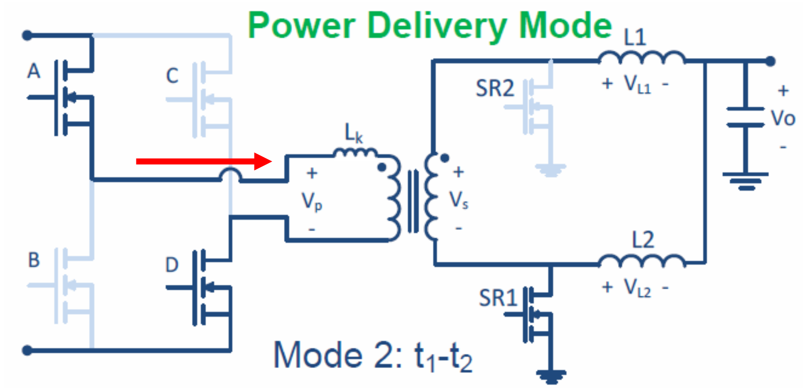


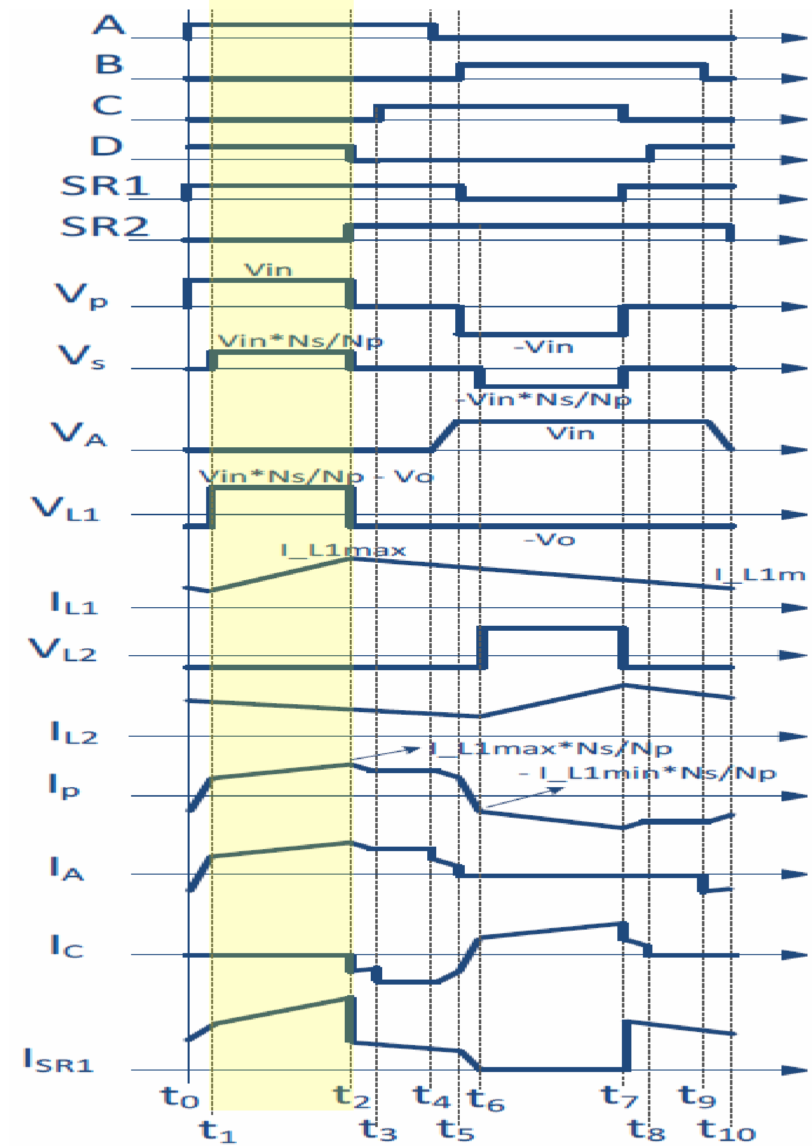
Duty cycle loss interval (t_0~t_1):

1. *$i_{Lk}(t_{0-})<0$, let body diode of switch A,D conduct*
   ➔ZVS turns on
2. *$i_{Lk}(t_{1-})<n*i_{L1}$➔ transformer decouple*
3. *$V_{L1}=V_{L2}=-V_o$, i_{L1}, i_{L2} decrease linearly*
4. *Input power doesn't transfer to secondary side*
   ➔Duty cycle loss

[Ref]: Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier, Sam Abdel-Rahman, Infineon Technologies North America (IFNA) Corp Design Note DN 2013-01 V1.0 January 2013

Phase Shift Full Bridge Converter – t_1~t_2



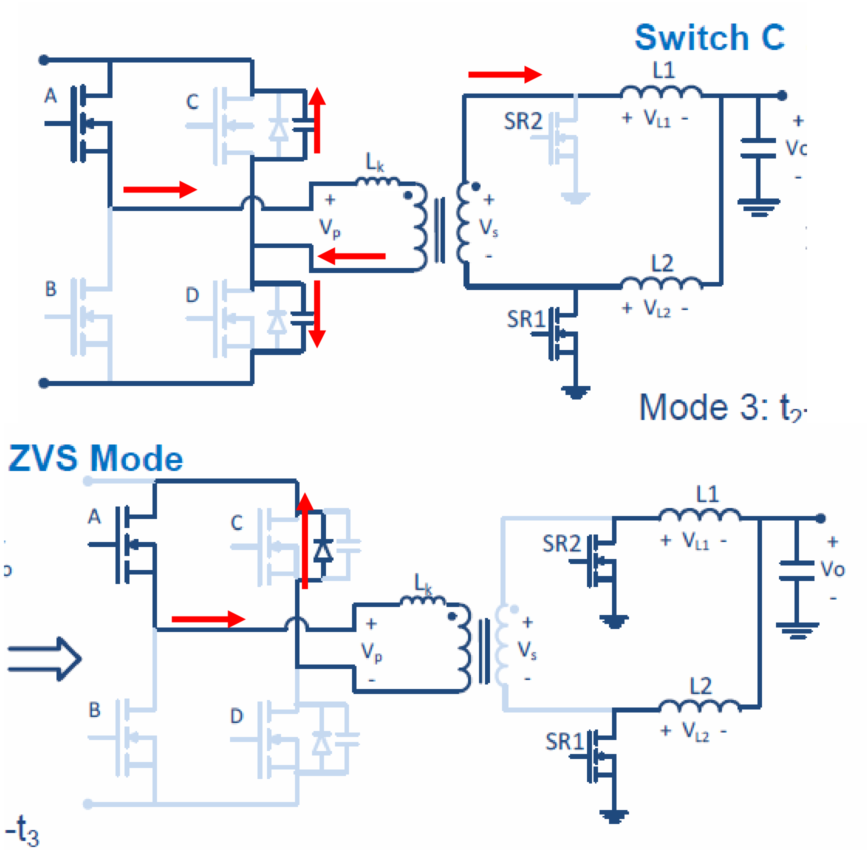


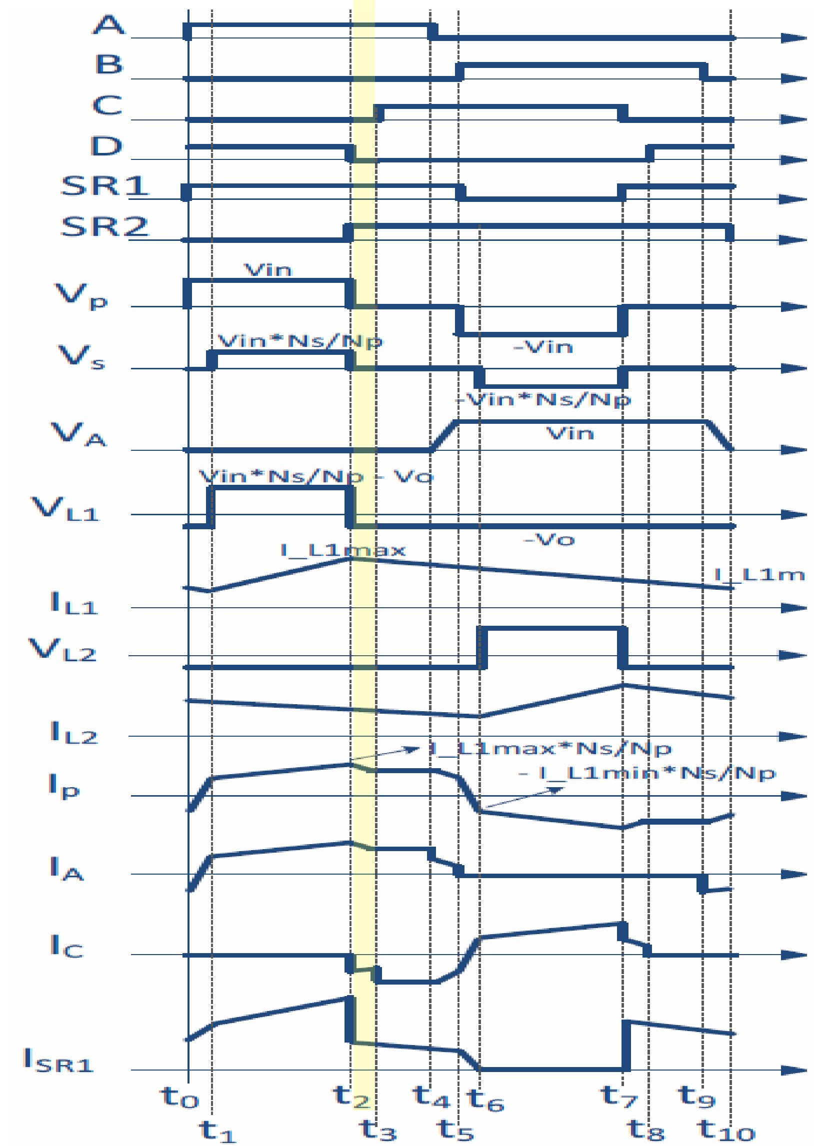
Power delivery interval (t_1~t_2):

1. *$i_{Lk}(t_{1+})=1/n*i_{L1}$ ➔ body diode of SR2 turns off ➔ transformer coupling*
2. *$V_{L1}=1/n*Vin-V_o$, i_{L1} increase linearly*
3. *Power delivery from primary side*

[Ref]: Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier, Sam Abdel-Rahman, Infineon Technologies North America (IFNA) Corp Design Note DN 2013-01 V1.0 January 2013

Phase Shift Full Bridge Converter – t_2~t_3



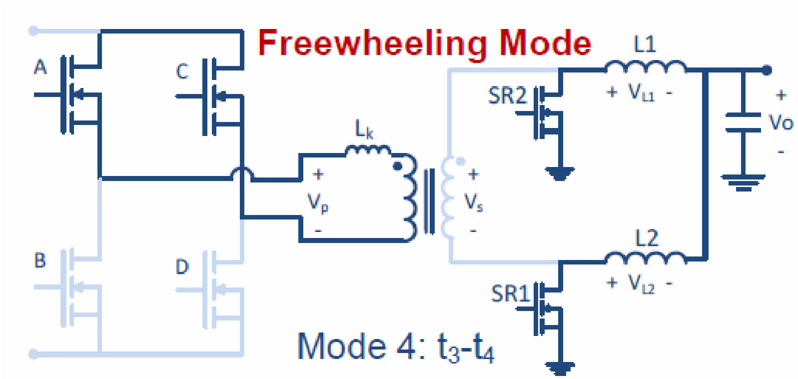


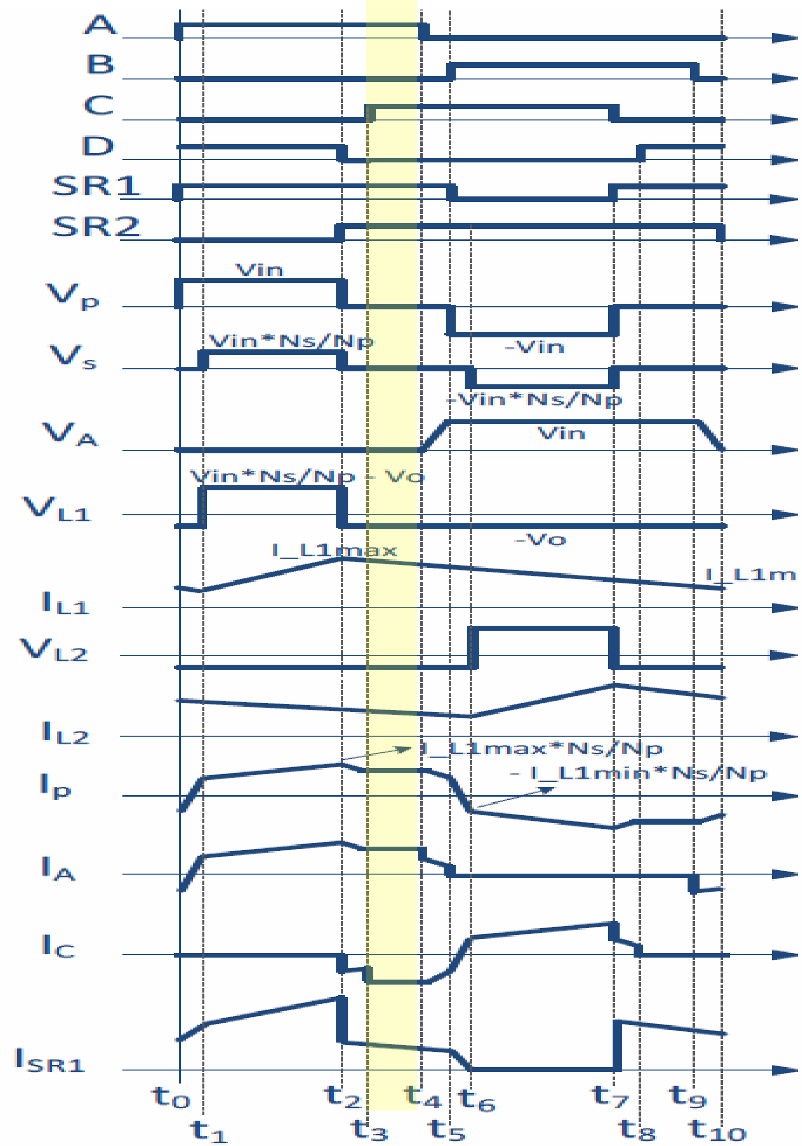
Switch C resonant interval (t_2~t_3):

1. $i_{Lk}(t_{2+})>0$ ➔ C_{oss} *of switch C discharge*
2. *Switch's body diode conduct*
3. *Vp = 0V*
4. *Transformer decouple*

[Ref]: Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier, Sam Abdel-Rahman, Infineon Technologies North America (IFNA) Corp Design Note DN 2013-01 V1.0 January 2013

Phase Shift Full Bridge Converter – t_3~t_4



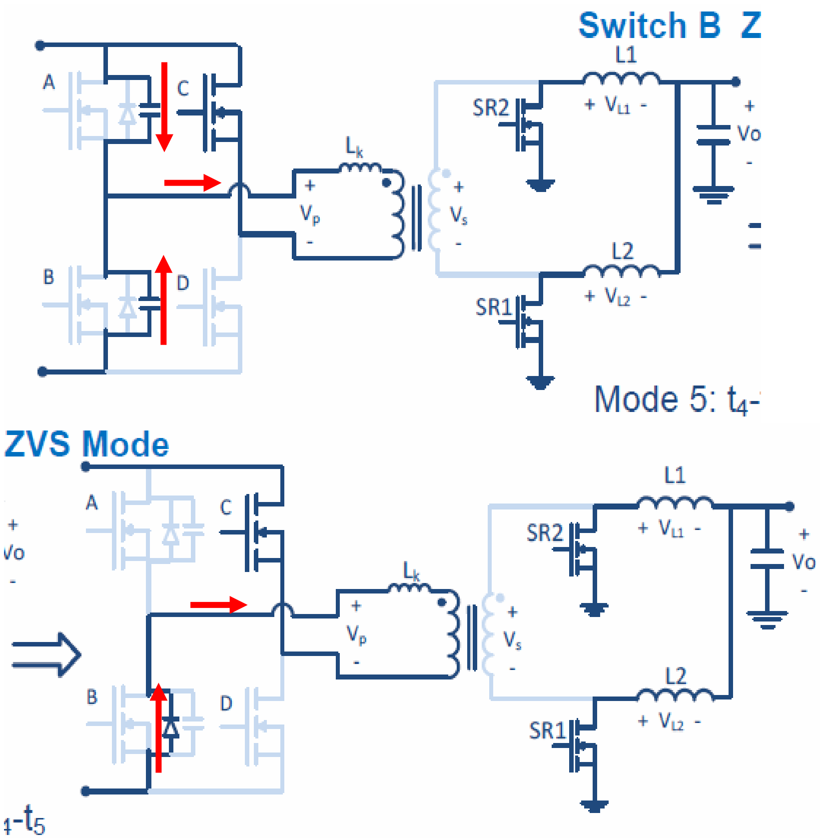


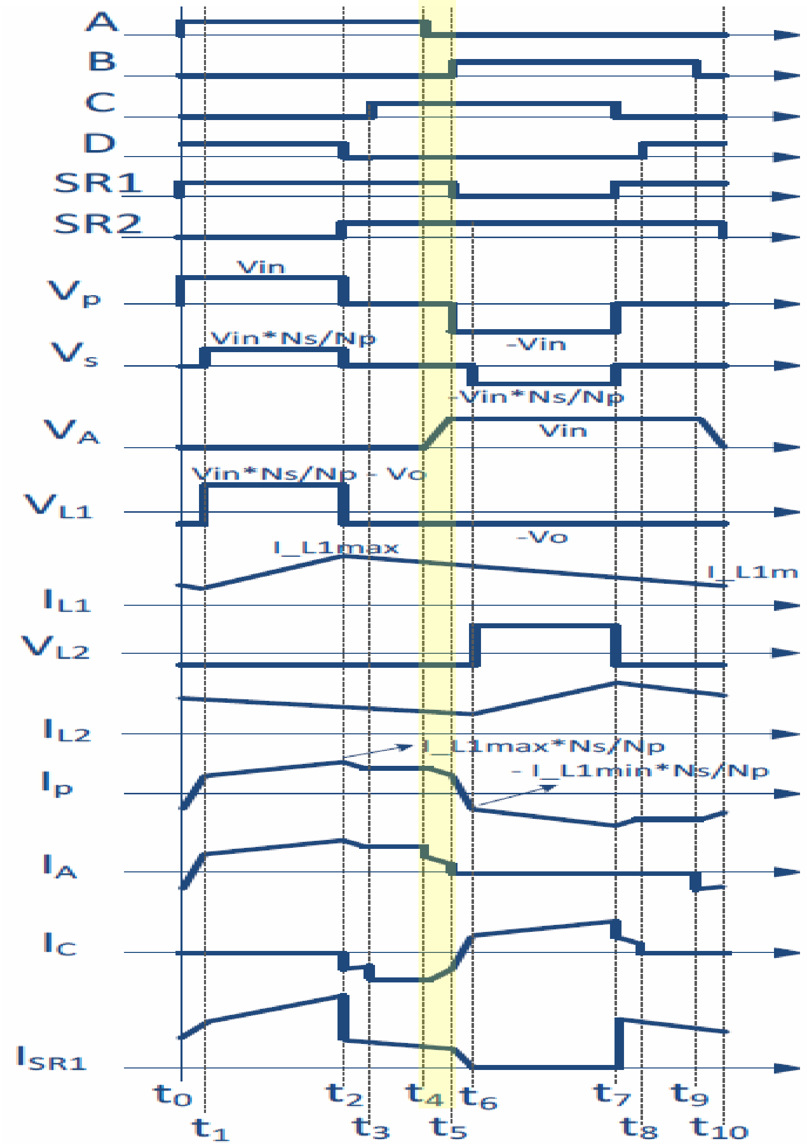
Switch C ZVS interval (t_3~t_4):

1. *Switch C turns on with ZVS*
2. *Vp = 0V, i_{Lk} freewheeling*
3. *Transformer decouple, i_{L1}, i_{L2} freewheeling*

[Ref]: Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier, Sam Abdel-Rahman, Infineon Technologies North America (IFNA) Corp Design Note DN 2013-01 V1.0 January 2013

Phase Shift Full Bridge Converter – t_4~t_5



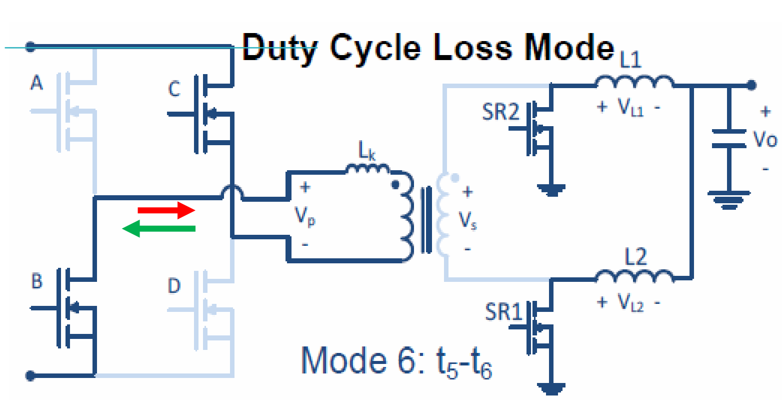


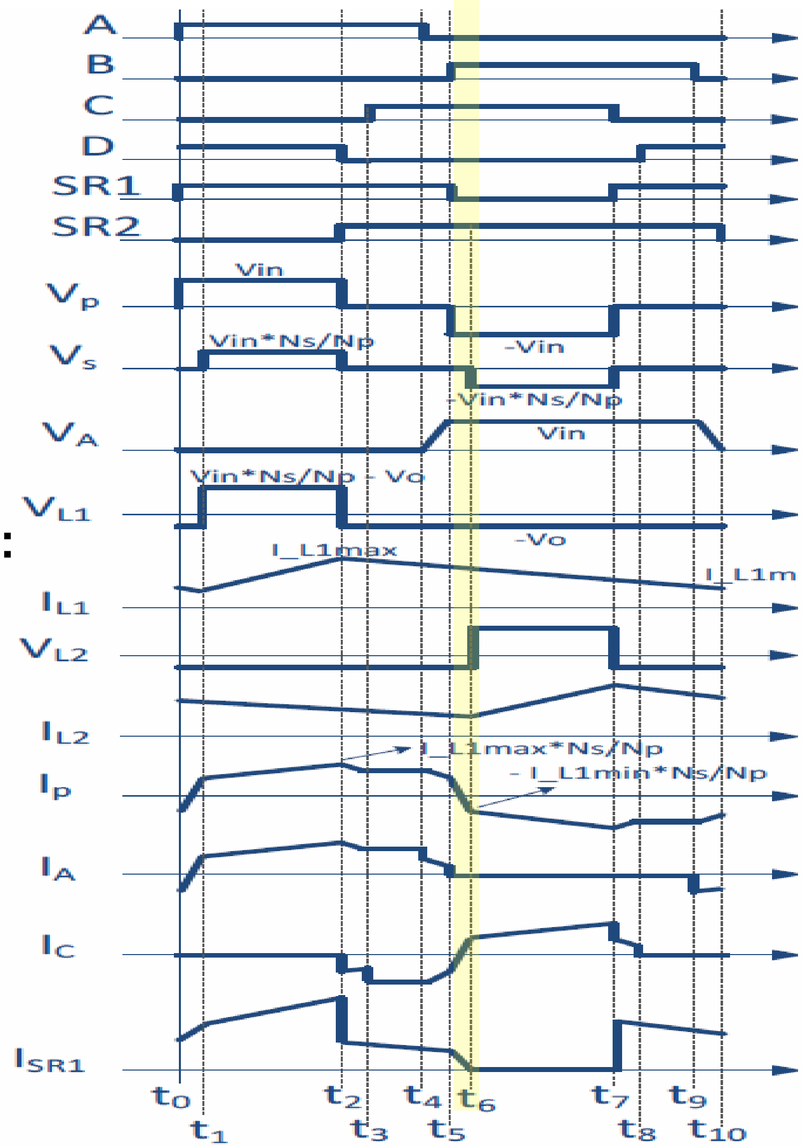
Switch B resonant interval (t_4~t_5):

1. *$i_{Lk}(t_{4+})>0$ ➔ C_{oss} of switch B discharge*
2. *Vp from 0V to –Vin ➔*
   i_{Lk} decrease linearly after switch B's body diode conduct

[Ref]: Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier, Sam Abdel-Rahman, Infineon Technologies North America (IFNA) Corp
Design Note DN 2013-01 V1.0 January 2013

Phase Shift Full Bridge Converter – t_5~t_6



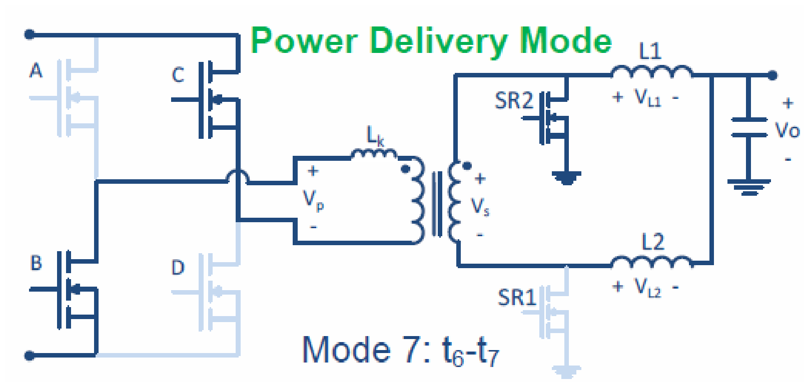


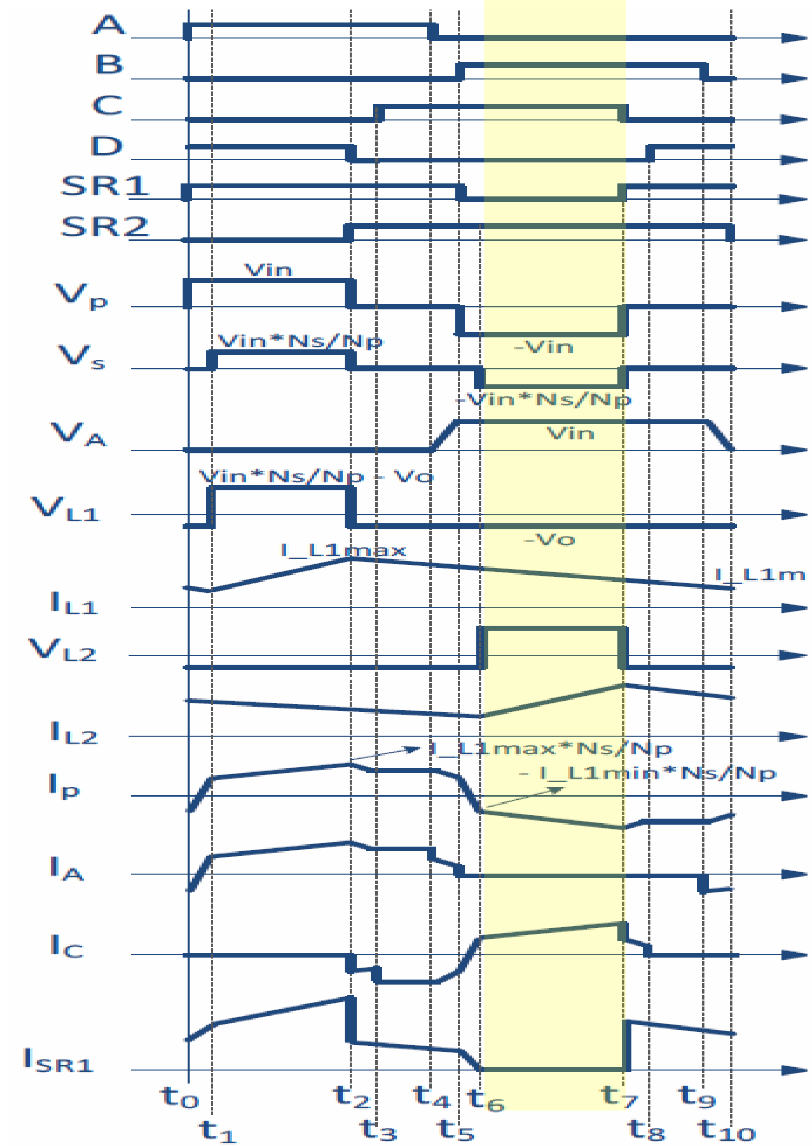
Switch B ZVS & Duty cycle loss interval (t_5~t_6):

1. *Switch B turns on @t=t_5 and $i_{Lk}(t_5)$>0, ZVS turn on*
2. *i_{Lk} decrease from positive to negative until it reach $-i_{L1}$*1/n*
3. *Transformer decouple*

[Ref]: Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier, Sam Abdel-Rahman, Infineon Technologies North America (IFNA) Corp Design Note DN 2013-01 V1.0 January 2013

Phase Shift Full Bridge Converter – t_6~t_7



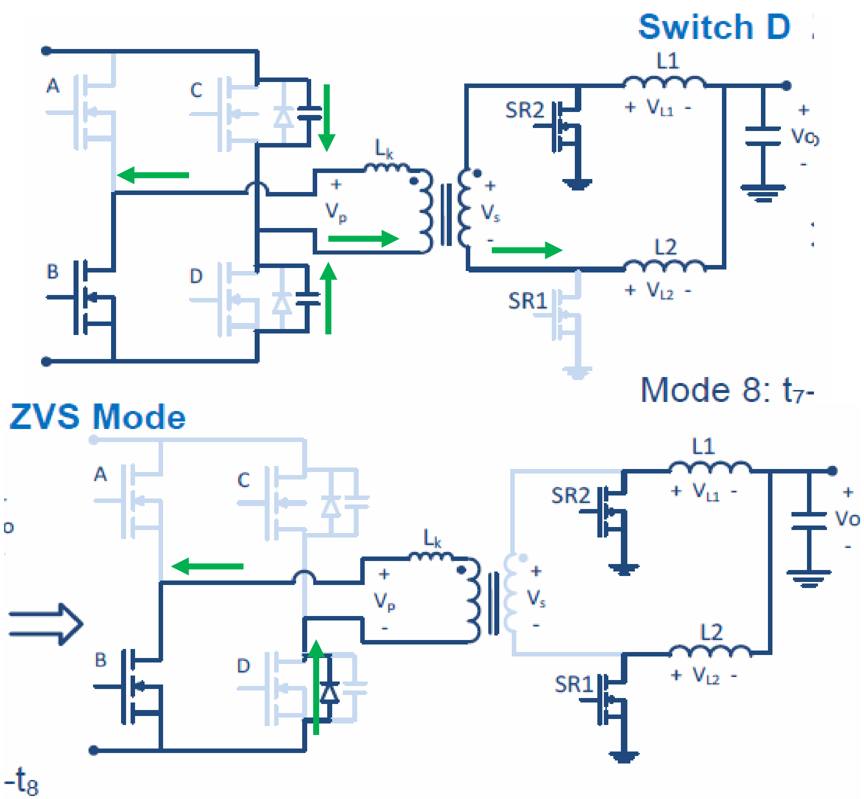


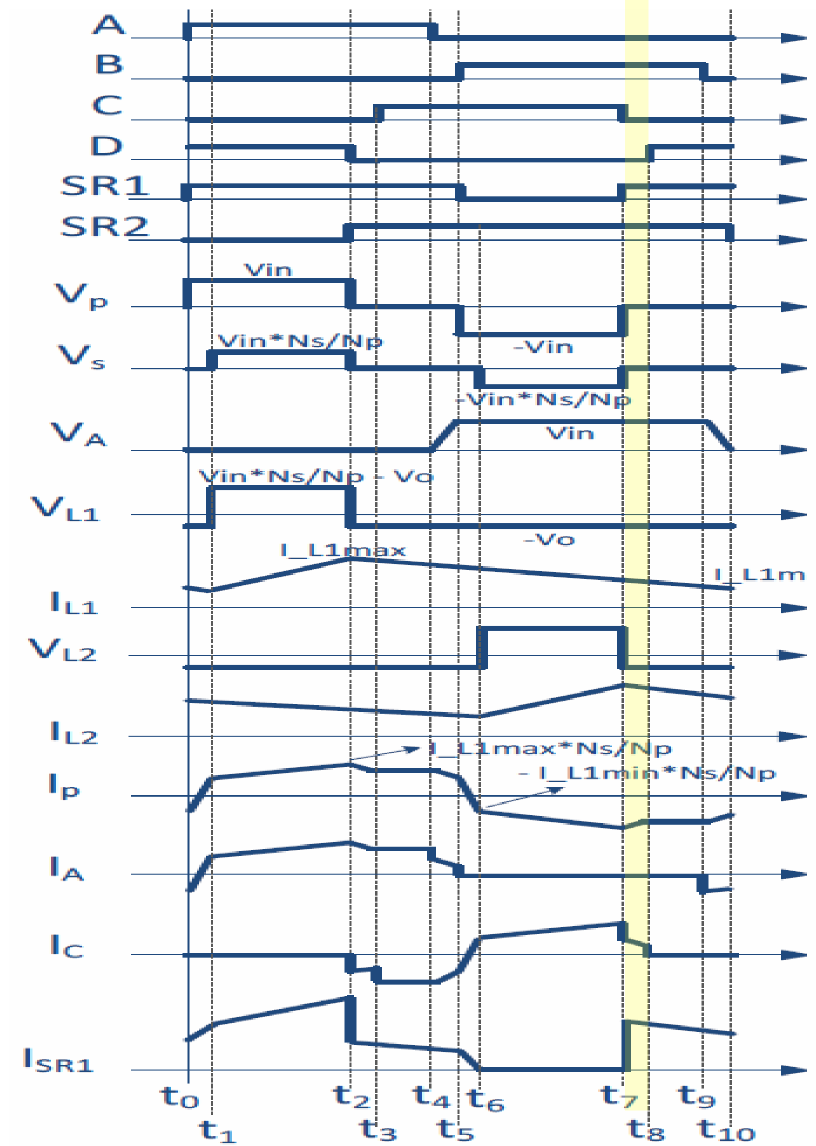
Power delivery interval (t_6~t_7):

1. *$i_{Lk}(t_{6+})=1/n*i_{L1}$ ➔ body diode of SR1 turns off ➔ transformer coupling*
2. *$V_{L2}=1/n*Vin-V_o$, i_{L2} increase linearly*
3. *Power delivery from primary side*

[Ref]: Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier, Sam Abdel-Rahman, Infineon Technologies North America (IFNA) Corp Design Note DN 2013-01 V1.0 January 2013

Phase Shift Full Bridge Converter – t_7~t_8



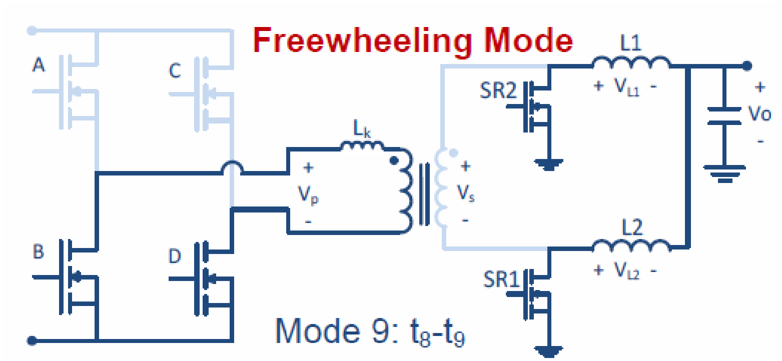


Switch D resonant interval (t_7~t_8):

1. $i_{Lk}(t_{7+})<0 \rightarrow C_{oss}$ *of switch D discharge*
2. *Switch's body diode conduct*
3. *Vp = 0V*
4. *Transformer decouple*

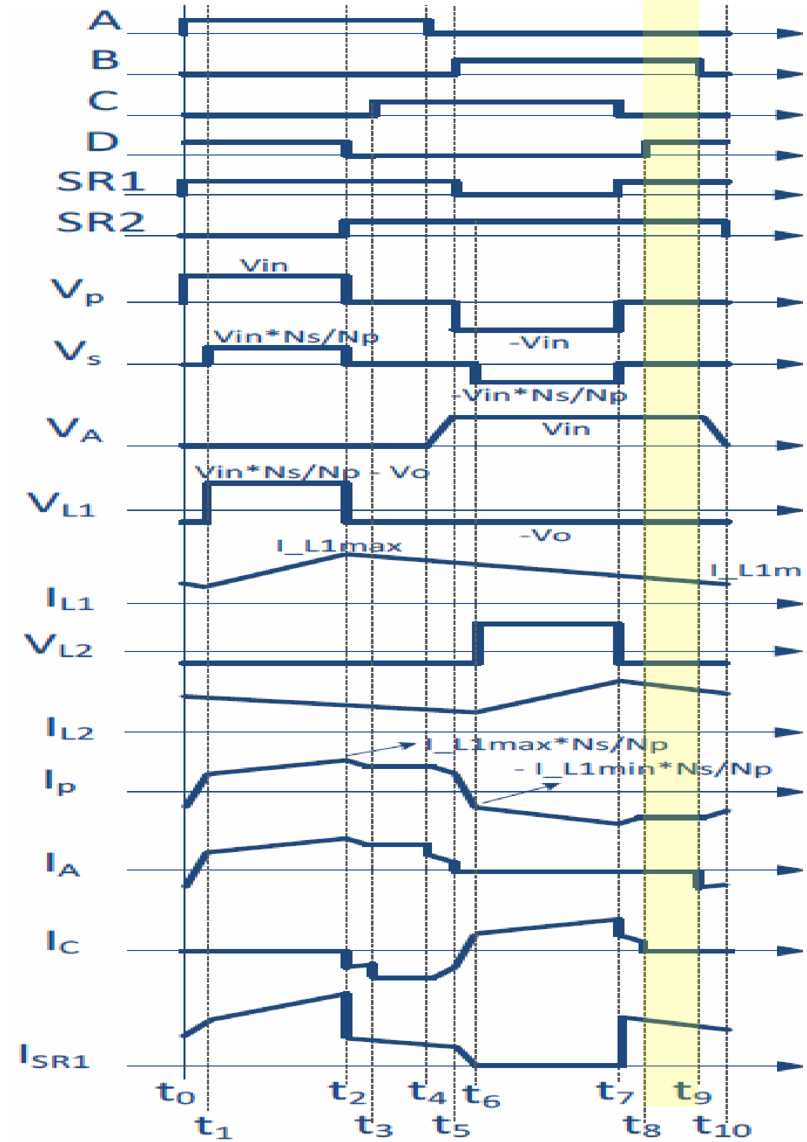
[Ref]: Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier, Sam Abdel-Rahman, Infineon Technologies North America (IFNA) Corp. Design Note DN 2013-01 V1.0 January 2013

Phase Shift Full Bridge Converter – t_8~t_9



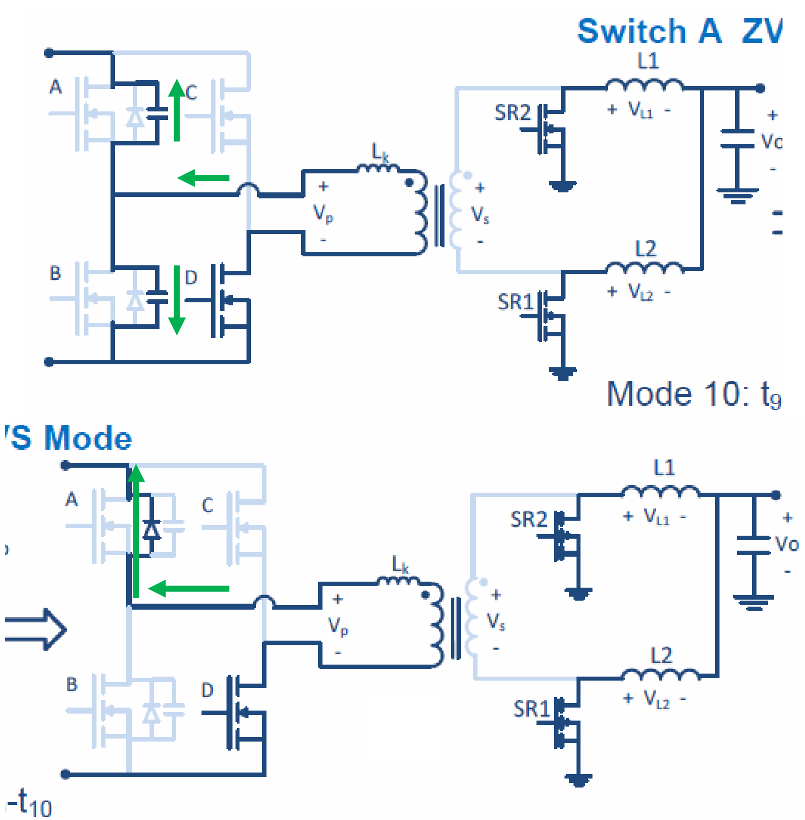
Switch D ZVS interval (t_8~t_9):

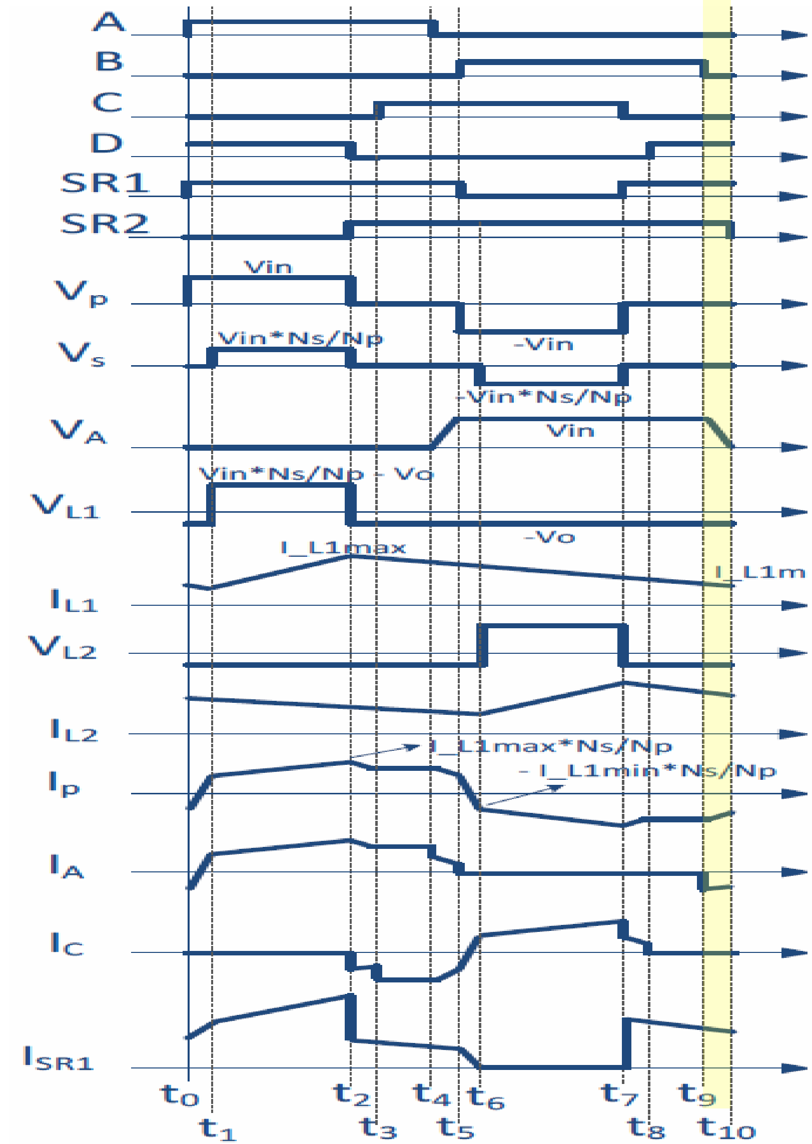
1. *Switch D turns on with ZVS*
2. *Vp = 0V, i_{Lk} freewheeling*
3. *Transformer decouple, i_{L1}, i_{L2} freewheeling*



[Ref]: Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier, Sam Abdel-Rahman, Infineon Technologies North America (IFNA) Corp. Design Note DN 2013-01 V1.0 January 2013

Phase Shift Full Bridge Converter – t_8~t_9





Switch A resonant interval (t_4~t_5):

1. *$i_{Lk}(t_{9+})>0$ ➔ C_{oss} of switch A discharge*
2. *Vp from 0V to Vin ➔*
   i_{Lk} increase linearly after switch A's body diode conduct

THANK YOU