Final Project – Sobel Filter

Group4

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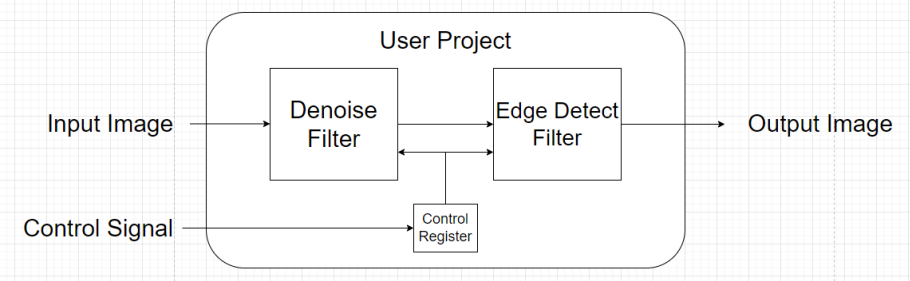
一、目標應用:

- System block diagram



- Goal

  Denoise Filter: Bypass、Gaussian Filter、Medium Filter

  EdgeDetect Filter: Bypass、Sobel Filter、Laplacian Filter

二、HLS 的 code 內容:

EdgeDetect

```
#pragma hls_design top
class EdgeDetect_Top
{
  //instances
  Denoise_IP Denoise_inst;
  EdgeDetect_Filter EdgeDetect_Filter_inst;
  ac_channel<pixelType>   dat_noise_out;

public:
  EdgeDetect_Top() {}

  //----------------------------------------------------------------------
  // Function: run
  //   Top interface for data in/out of class. Combines vertical and
  //   horizontal derivative and magnitude/angle computation.
  #pragma hls_design interface
  void CCS_BLOCK(run)(ac_channel<pixelType>   &dat_in,
                      maxWType                &widthIn,
                      maxHType                &heightIn,
                      ac_channel<pixelType>   &dat_out,
                      uint2       &ctrl_denoise,
                      uint2       &ctrl_edgedect
                      )
  {

    // Denoise
    Denoise_inst.run(dat_in, widthIn, heightIn, dat_noise_out, ctrl_denoise);
    // EdgeDetect
    EdgeDetect_Filter_inst.run(dat_noise_out, widthIn, heightIn, dat_out, ctrl_edgedect);
  }
};

}
```

由 Dataflow 的方式來傳遞 Data。

Denoise Inst 透過 ac_channel<pixelType> dat_noise_out; 傳遞完成 Denoise 的資料到 EdgeDetect Inst 進行處理，最後再輸出出去 dat_out。

Operation

1. Gaussian Filter、Sobel Filter、Laplacian Filter
   都是透過 3X3 的 Kernel 來實現，只要更換其中 Kernel 的值即可完成該算法的運算。

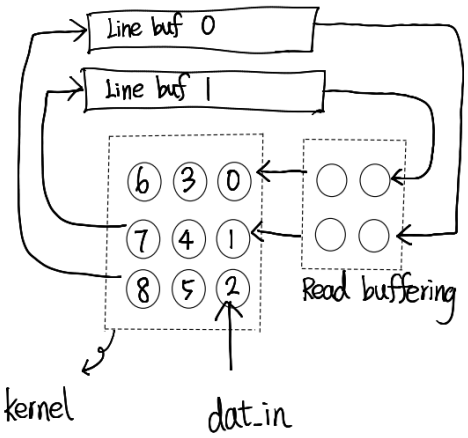
2. Medium Filter

```
// Medium Filter
for(i=0; i<9; i++){
  tmp_pix[i] = pix[i];
}

pix_result = 0;
for(j=0; j<5; j++){
  max_val = tmp_pix[j];
  max_i = j;
  for(i=j+1; i<9; i++){
    if(tmp_pix[i] > max_val){
      max_val = tmp_pix[i];
      max_i = i;
    }
  }
  tmp_pix[max_i] = tmp_pix[j];
}
pix_result = max_val;
```

   1. jth 中作為起始值，尋找 j+1 ~ END 中的最大值
   2. 尋找完畢時，將最大值的位置與 jth 交換，以確保 j+1~END 中的值小於 jth 的值(由於 0~jth 的值不會用到，因此就不必再對 jth 賦值)
   3. 經過五輪尋找後，最大值就會是數組的中間值。

3. Pixel 位移架構 (Denoise、EdgeDetect_Filter 各有一套 Pixel 位移)



第一步 載入第一行的值 pix0, pix1, pix2

```
// Read Pixel // For uint_pix[0]
if (x == 0 || x == 1) {
    pix[0] = pix[0];
} else {
    if ((x & 1) == 0) { // even 2, 4, 6, ...
        pix[0] = rdbuf1_pix.slc<8>(0);
    } else { // odd 3, 5, 7, ...
        pix[0] = rdbuf1_pix.slc<8>(8);
    }
}

// For uint_pix[1]
if (x == 0 || x == 1) {
    pix[1] = pix[1];
} else {
    if ((x & 1) == 0) { // even 2, 4, 6, ...
        pix[1] = rdbuf0_pix.slc<8>(0);
    } else { // odd 3, 5, 7, ...
        pix[1] = rdbuf0_pix.slc<8>(8);
    }
}
```

```
// Read dat_in into pix[2]
if (y <= heightIn-1 && x <= widthIn-1) {
  pix[2] = dat_in.read(); // Read streaming interface
}
```

第二步 對 Line Buffer 進行存取

X=0 時，需要將讀取到的資料存放在 pix3 pix0 pix4 pix1

X=1, 3, 5, … 將讀取到的資料存放在 Read Buffering

X=2, 4, 6, … 將 Kernel 內的資料(pix4, pix7, pix5, pix8)寫回 Write Buffer

```
// LineBuffer Access
// first col
if(x==0){
  rdbuf0_pix = line_buf0[x/2];
  rdbuf1_pix = line_buf1[x/2];

  pix[4] = rdbuf0_pix.slc<8>(0);
  pix[1] = rdbuf0_pix.slc<8>(8);

  pix[3] = rdbuf1_pix.slc<8>(0);
  pix[0] = rdbuf1_pix.slc<8>(8);
}else{
  if ( (x&1)==1 ) {
  // ReadLineBuffer in x=1, x=3, ... x=odd
    rdbuf0_pix = line_buf0[(x+1)/2];
    rdbuf1_pix = line_buf1[(x+1)/2];
  } else {
  // WriteLineBuffer in x=2, x=4, ... x=even
    if(y==0){    // first row => write into buf1
      line_buf0[(x/2)-1] = wrbuf0_pix;
    }else{
      line_buf0[(x/2)-1] = wrbuf0_pix;
      line_buf1[(x/2)-1] = wrbuf1_pix;
    }
  }
```

第三步 對每個邊界進行 Padding

```
// Padding
if(y==1 && x==1){
}else if(y == heightIn && x == 1){
}else if(y == 1 && x == widthIn){
}else if(y == heightIn && x == widthIn){
}else if(x==1){
}else if(y == heightIn){
}else if(y==1){
}else if(x == widthIn){
}
```

第四步 依照 Control Signal 進行相對應的計算

```
// Calculate with Gaussian_kernel
if(ctrl_signal == 0){
  // Bypass Mode
  pix_result = pix[4];
}else if(ctrl_signal == 1){
  // Gaussian Filter
  pix_result = (pix[6]*Gaussian_kernel[0])/16 + (pix[3]*Gaussian_kernel[1])/16 + (pix[0]*Gaussian_kernel
               (pix[7]*Gaussian_kernel[3])/16 + (pix[4]*Gaussian_kernel[4])/16 + (pix[1]*Gaussian_kernel
               (pix[8]*Gaussian_kernel[6])/16 + (pix[5]*Gaussian_kernel[7])/16 + (pix[2]*Gaussian_kernel
}else if(ctrl_signal == 2){
  // Medium Filter
  for(i=0; i<9; i++){
    tmp_pix[i] = pix[i];
  }

  pix_result = 0;
  for(j=0; j<5; j++){
    max_val = 0;
    for(i=0; i<9; i++){
      if(tmp_pix[i] > max_val){
```

第五步 將計算結果輸出出去

```
// Output dat_out
if (y!=0 && x!=0) {
  // Saturation
  //printf(" ======== pix_result ========= \n"
  //printf(" ======== x=%u, y=%u ========= \n"
  //printf(" ======== pix_result_sat=%2d, pix_
  pix_result_sat = pix_result;
  dat_out.write(pix_result_sat.slc<8>(2));
}
```

第六步 將 Kernel 的值進行位移

```
// Pixel Shift
pix[6] = pix[3]; pix[7] = pix[4]; pix[8] = pix[5];
if(x==0){
  // maintain
  pix[3] = pix[3]; pix[4] = pix[4];
}else{
  // shift
  pix[3] = pix[0]; pix[4] = pix[1];
}
pix[5] = pix[2];
```

第七步 更新 Write Buffer 內的值

```
// WriteLineBuffer
wrbuf0_pix.set_slc(0,pix[8]);
wrbuf0_pix.set_slc(8,pix[5]);
wrbuf1_pix.set_slc(0,pix[7]);
wrbuf1_pix.set_slc(8,pix[4]);
```

第八步 循環上面的步驟 x=0~WidthIn, y=0~heightIn

```
    // programmable width exit condition
    if (x ==  maxWType(widthIn)) { // cast to maxWType for RTL code coverage
      break;
    }
  }
  // programmable height exit condition
  if (y == heightIn) {
    break;
  }
```

Result

Image with Gaussian noise

After Gaussian Filter

Image with Salt and Pepper

After Medium Filter

Image with large edge variation

After Sobel Filter

Image with small edge variation

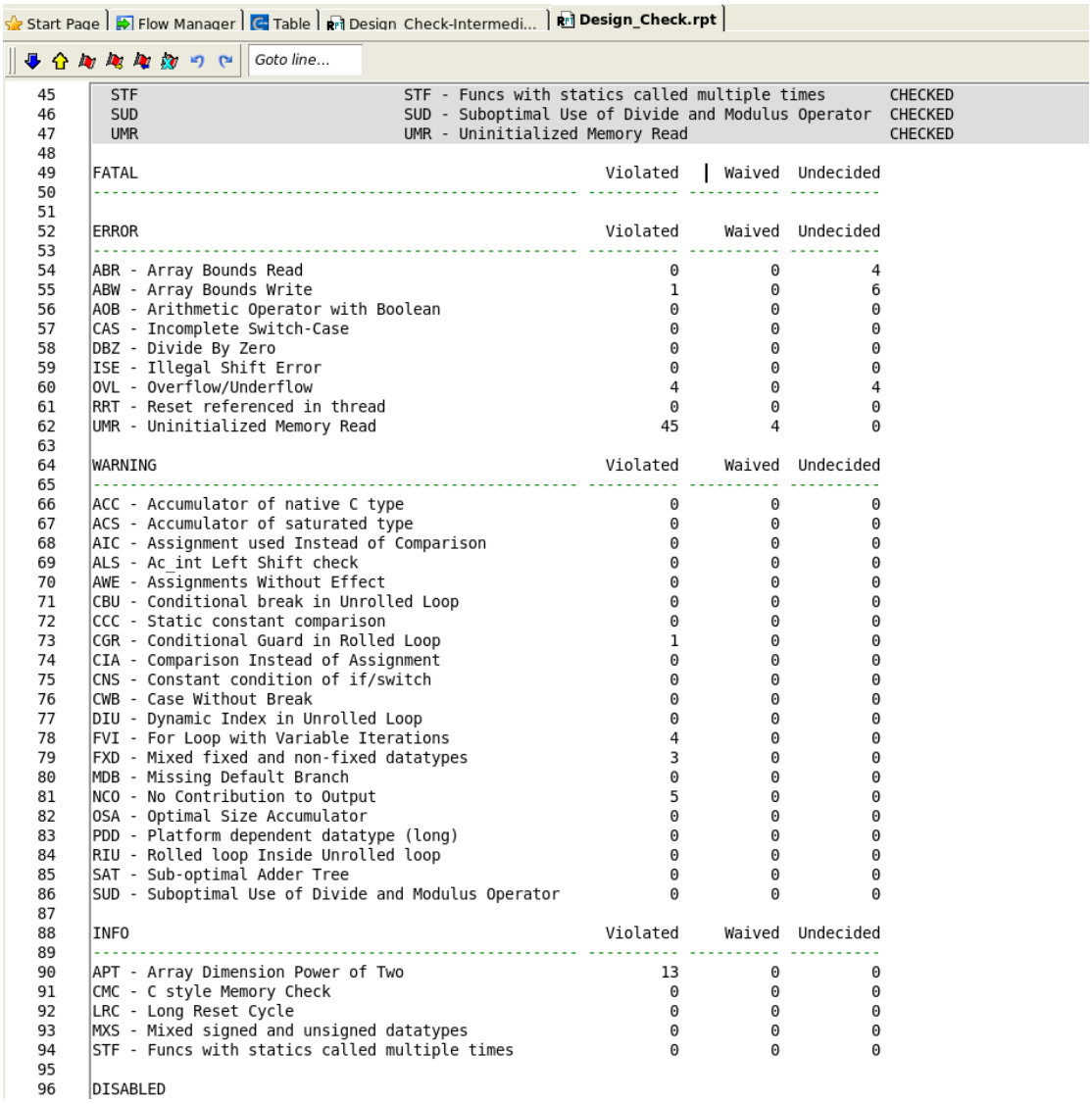
After Laplacian Filter

實作的流程:

一、Catapult Flow

Catapult 的部分大致上與 Lab2 無太大差異，就是照著老師提供的講義去完成。

1. CDesignChecker




```
  STF                              STF - Funcs with statics called multiple times       CHECKED
  SUD                              SUD - Suboptimal Use of Divide and Modulus Operator  CHECKED
  UMR                              UMR - Uninitialized Memory Read                      CHECKED

FATAL                                                 Violated  | Waived  Undecided
------------------------------------------------------ --------- --------- ----------

ERROR                                                 Violated    Waived  Undecided
------------------------------------------------------ --------- --------- ----------
ABR - Array Bounds Read                                      0         0          4
ABW - Array Bounds Write                                     1         0          6
AOB - Arithmetic Operator with Boolean                       0         0          0
CAS - Incomplete Switch-Case                                 0         0          0
DBZ - Divide By Zero                                         0         0          0
ISE - Illegal Shift Error                                    0         0          0
OVL - Overflow/Underflow                                     4         0          4
RRT - Reset referenced in thread                             0         0          0
UMR - Uninitialized Memory Read                             45         4          0

WARNING                                               Violated    Waived  Undecided
------------------------------------------------------ --------- --------- ----------
ACC - Accumulator of native C type                           0         0          0
ACS - Accumulator of saturated type                          0         0          0
AIC - Assignment used Instead of Comparison                  0         0          0
ALS - Ac_int Left Shift check                                0         0          0
AWE - Assignments Without Effect                             0         0          0
CBU - Conditional break in Unrolled Loop                     0         0          0
CCC - Static constant comparison                             0         0          0
CGR - Conditional Guard in Rolled Loop                       1         0          0
CIA - Comparison Instead of Assignment                       0         0          0
CNS - Constant condition of if/switch                        0         0          0
CWB - Case Without Break                                     0         0          0
DIU - Dynamic Index in Unrolled Loop                         0         0          0
FVI - For Loop with Variable Iterations                      4         0          0
FXD - Mixed fixed and non-fixed datatypes                    3         0          0
MDB - Missing Default Branch                                 0         0          0
NCO - No Contribution to Output                              5         0          0
OSA - Optimal Size Accumulator                               0         0          0
PDD - Platform dependent datatype (long)                     0         0          0
RIU - Rolled loop Inside Unrolled loop                       0         0          0
SAT - Sub-optimal Adder Tree                                 0         0          0
SUD - Suboptimal Use of Divide and Modulus Operator          0         0          0

INFO                                                  Violated    Waived  Undecided
------------------------------------------------------ --------- --------- ----------
APT - Array Dimension Power of Two                          13         0          0
CMC - C style Memory Check                                   0         0          0
LRC - Long Reset Cycle                                       0         0          0
MXS - Mixed signed and unsigned datatypes                    0         0          0
STF - Funcs with statics called multiple times               0         0          0

DISABLED
```

2. Generate RTL

Start Page | Flow Manager | Table | Constraint Editor | rtl.v

Goto line...

```
13  // ------------------------------------------------------------------
14
15
16  module EdgeDetect_IP_EdgeDetect_Top (
17    clk, rst, arst_n, dat_in_rsc_dat, dat_in_rsc_vld, dat_in_rsc_rdy, widthIn, heightIn,
18        dat_out_rsc_dat, dat_out_rsc_vld, dat_out_rsc_rdy, ctrl_denoise_rsc_dat, ctrl_denoise_triosy_lz,
19        ctrl_edgedect_rsc_dat, ctrl_edgedect_triosy_lz, line_buf0_rsc_Denoise_inst_en,
20        line_buf0_rsc_Denoise_inst_q, line_buf0_rsc_Denoise_inst_we, line_buf0_rsc_Denoise_inst_d,
21        line_buf0_rsc_Denoise_inst_adr, line_buf1_rsc_Denoise_inst_en, line_buf1_rsc_Denoise_inst_q,
22        line_buf1_rsc_Denoise_inst_we, line_buf1_rsc_Denoise_inst_d, line_buf1_rsc_Denoise_inst_adr,
23        line_buf0_rsc_EdgeDetect_Filter_inst_en, line_buf0_rsc_EdgeDetect_Filter_inst_q,
24        line_buf0_rsc_EdgeDetect_Filter_inst_we, line_buf0_rsc_EdgeDetect_Filter_inst_d,
25        line_buf0_rsc_EdgeDetect_Filter_inst_adr, line_buf1_rsc_EdgeDetect_Filter_inst_en,
26        line_buf1_rsc_EdgeDetect_Filter_inst_q, line_buf1_rsc_EdgeDetect_Filter_inst_we,
27        line_buf1_rsc_EdgeDetect_Filter_inst_d, line_buf1_rsc_EdgeDetect_Filter_inst_adr
28  );
29    input clk;
30    input rst;
31    input arst_n;
32    input [7:0] dat_in_rsc_dat;
33    input dat_in_rsc_vld;
34    output dat_in_rsc_rdy;
35    input [10:0] widthIn;
36    input [9:0] heightIn;
37    output [7:0] dat_out_rsc_dat;
38    output dat_out_rsc_vld;
39    input dat_out_rsc_rdy;
40    input [1:0] ctrl_denoise_rsc_dat;
41    output ctrl_denoise_triosy_lz;
42    input [1:0] ctrl_edgedect_rsc_dat;
43    output ctrl_edgedect_triosy_lz;
44    output line_buf0_rsc_Denoise_inst_en;
45    input [15:0] line_buf0_rsc_Denoise_inst_q;
46    output line_buf0_rsc_Denoise_inst_we;
47    output [15:0] line_buf0_rsc_Denoise_inst_d;
48    output [9:0] line_buf0_rsc_Denoise_inst_adr;
49    output line_buf1_rsc_Denoise_inst_en;
50    input [15:0] line_buf1_rsc_Denoise_inst_q;
51    output line_buf1_rsc_Denoise_inst_we;
52    output [15:0] line_buf1_rsc_Denoise_inst_d;
53    output [9:0] line_buf1_rsc_Denoise_inst_adr;
54    output line_buf0_rsc_EdgeDetect_Filter_inst_en;
55    input [15:0] line_buf0_rsc_EdgeDetect_Filter_inst_q;
56    output line_buf0_rsc_EdgeDetect_Filter_inst_we;
57    output [15:0] line_buf0_rsc_EdgeDetect_Filter_inst_d;
58    output [9:0] line_buf0_rsc_EdgeDetect_Filter_inst_adr;
59    output line_buf1_rsc_EdgeDetect_Filter_inst_en;
60    input [15:0] line_buf1_rsc_EdgeDetect_Filter_inst_q;
61    output line_buf1_rsc_EdgeDetect_Filter_inst_we;
62    output [15:0] line_buf1_rsc_EdgeDetect_Filter_inst_d;
63    output [9:0] line_buf1_rsc_EdgeDetect_Filter_inst_adr;
64
65
66    // Interconnect Declarations
67    wire [7:0] dat_out_rsc_dat_n_Denoise_inst;
68    wire line_buf0_rsc_en_n_Denoise_inst;
69    wire [15:0] line_buf0_rsc_d_n_Denoise_inst;
70    wire [9:0] line_buf0_rsc_adr_n_Denoise_inst;
71    wire line_buf1_rsc_en_n_Denoise_inst;
72    wire [15:0] line_buf1_rsc_d_n_Denoise_inst;
73    wire [9:0] line_buf1_rsc_adr_n_Denoise_inst;
74    wire [7:0] dat_out_rsc_dat_n_EdgeDetect_Filter_inst;
75    wire line_buf0_rsc_en_n_EdgeDetect_Filter_inst;
76    wire [15:0] line_buf0_rsc_d_n_EdgeDetect_Filter_inst;
77    wire [9:0] line_buf0_rsc_adr_n_EdgeDetect_Filter_inst;
78    wire line_buf1_rsc_en_n_EdgeDetect_Filter_inst;
79    wire [15:0] line_buf1_rsc_d_n_EdgeDetect_Filter_inst;
80    wire [9:0] line_buf1_rsc_adr_n_EdgeDetect_Filter_inst;
81    wire dat_in_rsc_rdy_n_Denoise_inst_bud;
82    wire dat_out_rsc_vld_n_Denoise_inst_bud;
83    wire dat_in_rsc_rdy_n_EdgeDetect_Filter_inst_bud;
84    wire ctrl_signal_triosy_lz_n_Denoise_inst_bud;
85    wire line_buf0_rsc_we_n_Denoise_inst_bud;
86    wire line_buf1_rsc_we_n_Denoise_inst_bud;
87    wire dat_out_rsc_vld_n_EdgeDetect_Filter_inst_bud;
88    wire ctrl_signal_triosy_lz_n_EdgeDetect_Filter_inst_bud;
89    wire line_buf0_rsc_we_n_EdgeDetect_Filter_inst_bud;
90    wire line_buf1_rsc_we_n_EdgeDetect_Filter_inst_bud;
```

3. Synthesis Report

Area

```
Start Page | Flow Manager | Table | Constraint Editor | rtl.v | rtl.rpt
Goto line...

Design Input Files Specified
  $PROJECT_HOME/../final_project/Final_prj/hls_c/inc/EdgeDetect.h
    $PROJECT_HOME/../final_project/Final_prj/hls_c/inc/EdgeDetect_defs.h
      $MGC_HOME/shared/include/ac_int.h
      $MGC_HOME/shared/include/ac_fixed.h
      $MGC_HOME/shared/include/ac_channel.h
      $MGC_HOME/shared/include/ac_math/ac_sqrt_pwl.h
        $MGC_HOME/shared/include/ac_float.h
        $MGC_HOME/shared/include/ac_complex.h
        $MGC_HOME/shared/include/ac_math/ac_shift.h
        $MGC_HOME/shared/include/ac_math/ac_normalize.h
      $MGC_HOME/shared/include/ac_math/ac_atan2_cordic.h
    $PROJECT_HOME/../final_project/Final_prj/hls_c/inc/Denoise_IP.h
      $MGC_HOME/shared/include/mc_scverify.h
    $PROJECT_HOME/../final_project/Final_prj/hls_c/inc/EdgeDetect_Filter.h
      $MGC_HOME/shared/include/mc_scverify.h
  $PROJECT_HOME/../final_project/Final_prj/hls_c/src/EdgeDetect_tb.cpp
  $PROJECT_HOME/../final_project/Final_prj/bmpUtil/src/bmp_io.cpp

Processes/Blocks in Design
  Process Real Operation(s) count Latency Throughput Reset Length II Comments
  ------- --------------------- ------- ---------- ------------ -- --------

Bill Of Materials (Datapath)
  Component Name                     Area Score Delay Post Alloc Post Assign
  ---------------------------------- ---------- ----- ---------- -----------
  [Lib: Catapult_16]
  EdgeDetect_IP::Denoise_IP.v1         5643.128 0.000          0           1
  EdgeDetect_IP::EdgeDetect_Filter.v1  3284.785 0.000          0           1

  TOTAL AREA (After Assignment):       8927.914

Area Scores
                    Post-Scheduling   Post-DP & FSM Post-Assignment
  ----------------- --------------- --------------- ---------------
  Total Area Score:   7929.1          8791.1          8927.9
  Total Reg:          4431.6  (56%)   3020.9  (34%)   3020.9  (34%)

  DataPath:           7929.1 (100%)   8745.1  (99%)   8880.8  (99%)
    MUX:              1986.7  (25%)   3181.0  (36%)   3109.0  (35%)
    FUNC:             1381.1  (17%)   1445.0  (17%)    977.0  (11%)
    LOGIC:             129.8   (2%)   1140.2  (13%)   1815.9  (20%)
    BUFFER:              0.0             0.0             0.0
    MEM:                 0.0             0.0             0.0
    ROM:                 0.0             0.0             0.0
    REG:              4431.6  (56%)   2978.9  (34%)   2978.9  (34%)


  FSM:                   0.0            46.0   (1%)     47.1   (1%)
    FSM-REG:             0.0            42.0  (91%)     42.0  (89%)
    FSM-COMB:            0.0             4.0   (9%)      5.1  (11%)
```

Timing

```
Start Page | Flow Manager | Table | Constraint Editor | rtl.v | rtl.rpt
Goto line...


  (MUX = multiplexers; FUNC = datapath logic (e.g. add/mult); LOGIC = control logic)

Register-to-Variable Mappings
  Register Size(bits) Gated Register CG Opt Done Variables
  -------- ---------- -------------- ---------- ---------------------------------------------------

  Total:           0              0          0 (Total Gating Ratio: 0.00, CG Opt Gating Ratio: 0.00)

Timing Report
  Critical Path
    Max Delay:  3.719621
    Slack:      6.280379

    Path                                                 Startpoint                                           Endpoint                                        Delay  Slack
    ---------------------------------------------------- ---------------------------------------------------- ----------------------------------------------- ------ ------ ----------------
    1                                                    EdgeDetect_IP::EdgeDetect_Top/clk                    EdgeDetect_IP::EdgeDetect_Top/EdgeDetect_Filter_inst 3.7196 6.2804

      Instance                                           Component                                                                                            Delta  Delay  [MIN, MAX]
      --------                                           ---------                                                                                            -----  -----  ----------------
      EdgeDetect_IP::EdgeDetect_Top/clk                                                                                                                       0.0000 0.0000
      EdgeDetect_IP::EdgeDetect_Top/EdgeDetect_Filter_inst EdgeDetect_IP::EdgeDetect_Filter                                                                   3.7196 3.7196

    2                                                    EdgeDetect_IP::EdgeDetect_Top/widthIn                EdgeDetect_IP::EdgeDetect_Top/EdgeDetect_Filter_inst 3.6136 6.3864

      Instance                                           Component                                                                                            Delta  Delay  [MIN, MAX]
      --------                                           ---------                                                                                            -----  -----  ----------------
      EdgeDetect_IP::EdgeDetect_Top/widthIn                                                                                                                   0.0000 0.0000
      EdgeDetect_IP::EdgeDetect_Top/EdgeDetect_Filter_inst EdgeDetect_IP::EdgeDetect_Filter(widthIn=>clk)                                                     3.6136 3.6136

    3                                                    EdgeDetect_IP::EdgeDetect_Top/heightIn               EdgeDetect_IP::EdgeDetect_Top/EdgeDetect_Filter_inst 3.6094 6.3906

      Instance                                           Component                                                                                            Delta  Delay  [MIN, MAX]
      --------                                           ---------                                                                                            -----  -----  ----------------
      EdgeDetect_IP::EdgeDetect_Top/heightIn                                                                                                                  0.0000 0.0000
      EdgeDetect_IP::EdgeDetect_Top/EdgeDetect_Filter_inst EdgeDetect_IP::EdgeDetect_Filter(heightIn=>clk)                                                    3.6094 3.6094
```