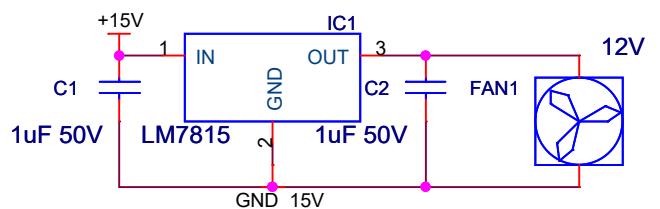
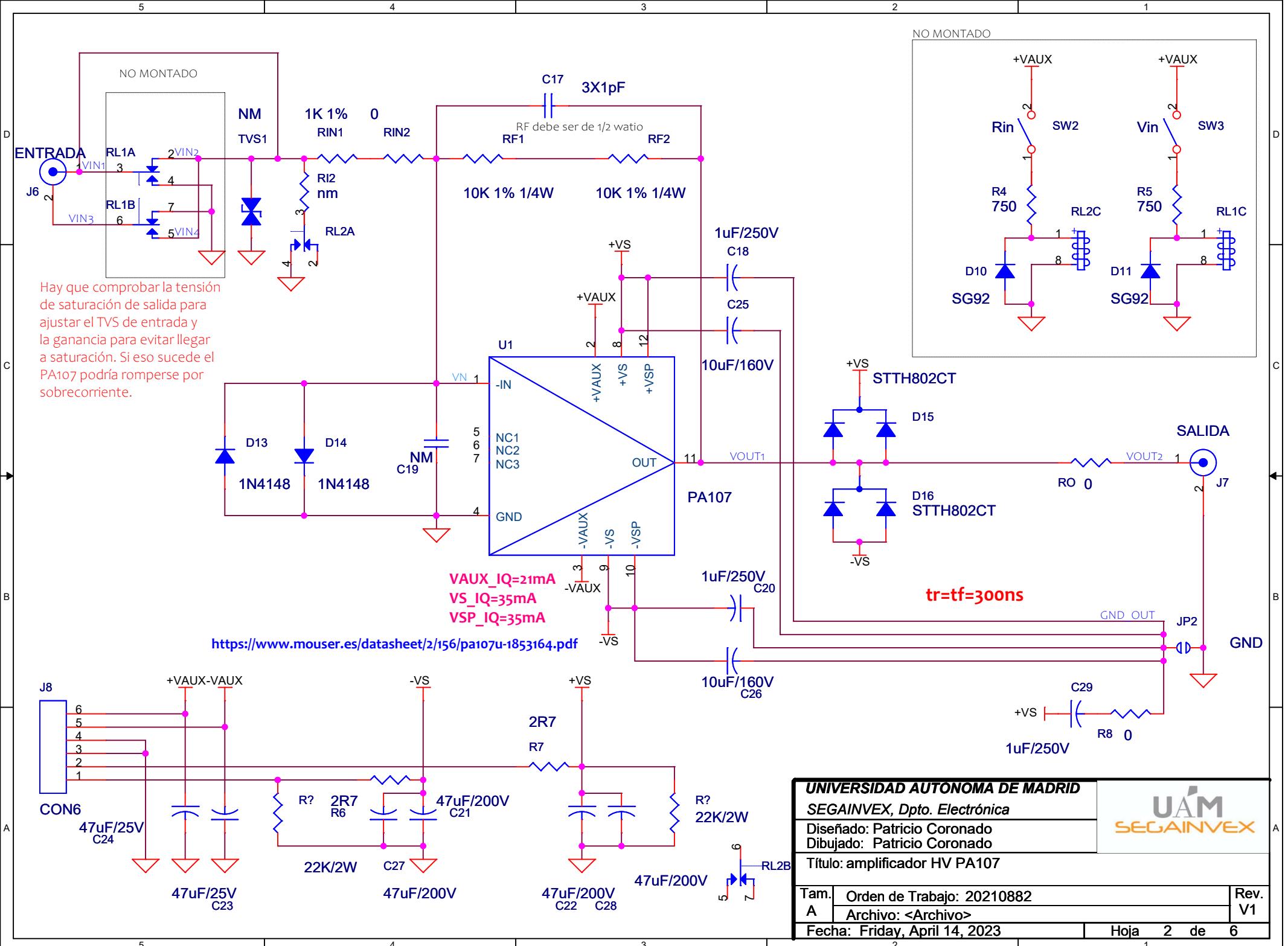


IMPEDANCIA DE ENTRADA = 1Koh
IMPEDANCIA DE SALIDA = 0 oh
GANANCIA = -20 V/V

<https://www.mouser.es/datasheet/2/156/pa107u-1853164.pdf>



UNIVERSIDAD AUTÓNOMA DE MADRID	
SEGAINVEX, Dpto. Electrónica	
Diseñado:	Patricio Coronado J.A.Higuera
Dibujado:	Patricio Coronado J.A.Higuera
Título:	amplificador de pulsos
Tam.	Orden de Trabajo: 20210882
A	Archivo: <Archivo>
Rev.	V1
Fecha: Friday, April 14, 2023	
Hoja	1 de 6



CABLE-PH04
N.º de producto de Digi-Key
1460-1295-ND

macho en PCB:
B3B-PH-K-S(LF)(SN)
RS:820-1431
contacto
BPH-002T-Po.5S
RS:820-1456
conector cable:
JST PHR-3
RS:820-1475

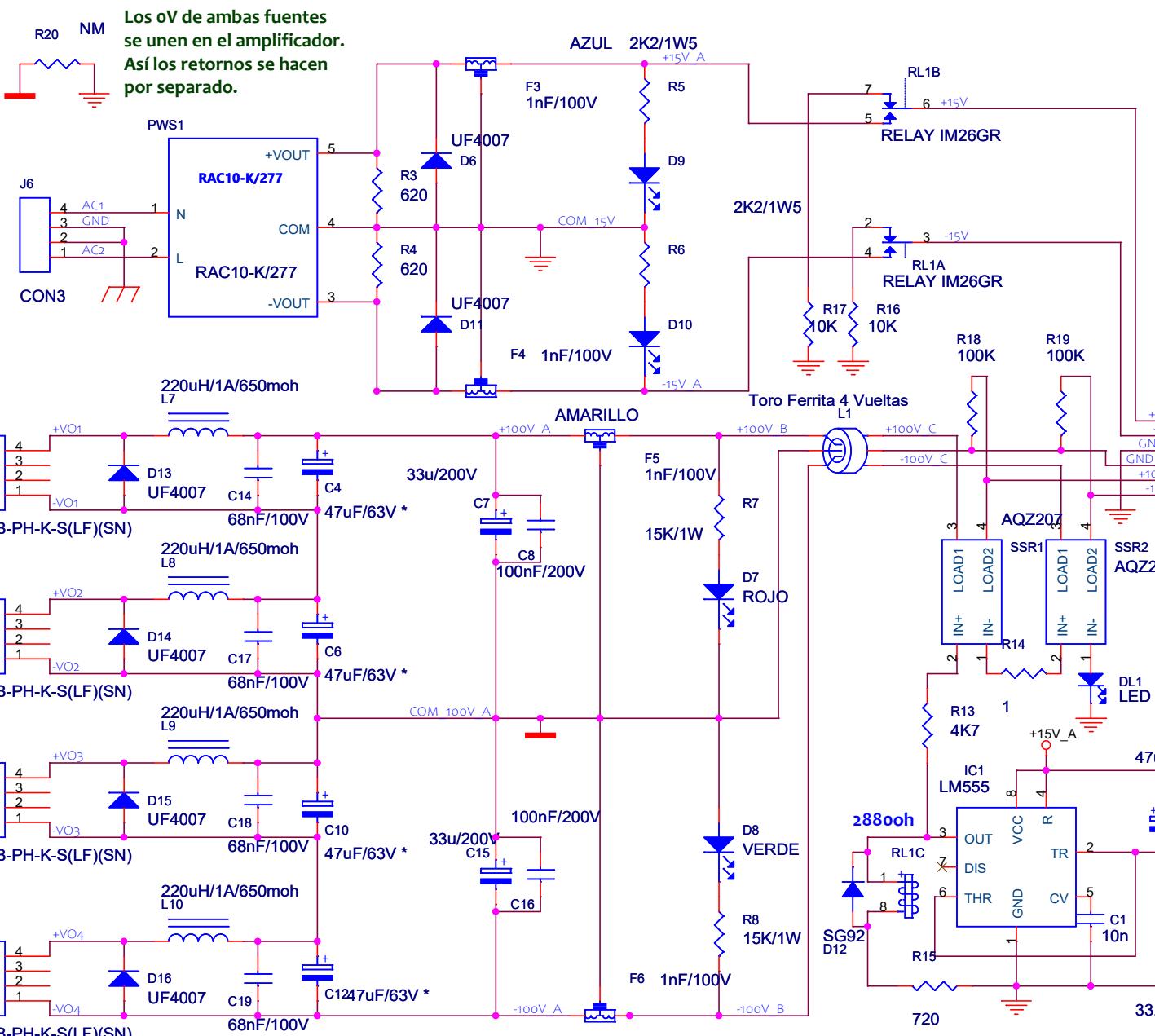
macho en PCB:B5B-PH-K-S(LF)(SN)
RS:820-1438
contacto:BPH-002T-Po.5S
RS:820-1456
conector cable:JST PHR-4
RS:820-1472

J9
5 N1
4
3
2
1 L1
B5B-PH-K-S(LF)(SN)

J10
5 N2
4
3
2
1 L2
B5B-PH-K-S(LF)(SN)

J11
5 N3
4
3
2
1 L3
B5B-PH-K-S(LF)(SN)

J12
5 N4
4
3
2
1 L4
B5B-PH-K-S(LF)(SN)



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SEGAINVEX, Dpto. Electrónica

Diseñado: Juan Antonio Higuera
Dibujado: Patricio Coronado

Título: FUENTE DE ALIMENTACIÓN

Tam.: Orden de Trabajo: 20210882

Custom:

Archivo: <Archivo>

Fecha: Friday, April 14, 2023

Rev. A

UAM
SEGAINVEX

6

3

de

1

Hoja



UNIVERSIDAD AUTONOMA DE MADRID

SEGAINVEX, Dpto. Electrónica

Diseñado:

Dibujado:

Título: oscilograma 1

UAM
SEGAINVEX

Tam. Orden de Trabajo: 20210882

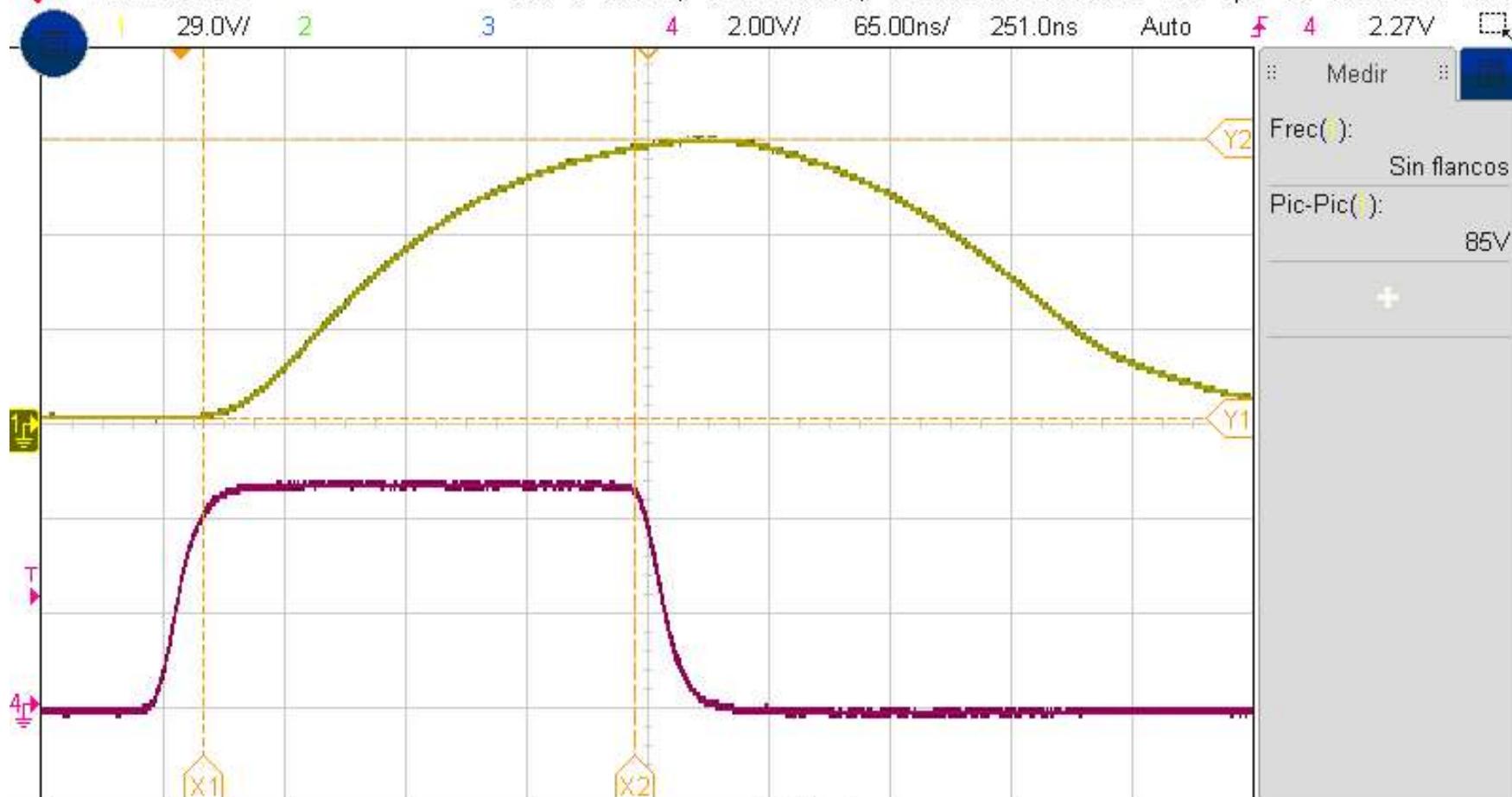
A Archivo: <Archivo>

Fecha: Friday, April 14, 2023

Rev.

A

Hoja 5 de 6



UNIVERSIDAD AUTONOMA DE MADRID

SEGAINVEX, Dpto. Electrónica

Diseñado:
Dibujado:

Título: oscilograma 2

UAM
SEGAINVEX

Tam. Orden de Trabajo: 20210882

A Archivo: <Archivo>

Fecha: Friday, April 14, 2023

Rev.

A

Hoja 6 de 6

Power Operational Amplifiers



RoHS
COMPLIANT

FEATURES

- Power Bandwidth 170 V_{P-P}, 2 MHz
- Output Voltage up to 180 V_{p-p}
- High Slew Rate 2500 V/ μ s Minimum with $A_{CL} = 20$
- High Gain Bandwidth Product 180 MHz
- High Output Current ± 1.5 A Steady State Within SOA
- High Peak Output Current ± 5 A



APPLICATIONS

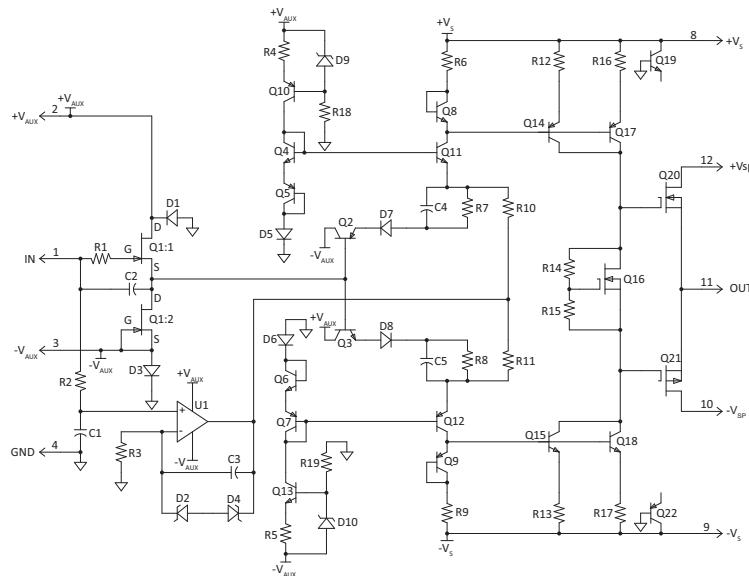
- Piezo Drive
- CRT Beam Intensity Control
- ATE Applications
- Line Driver

GENERAL DESCRIPTION

The PA107DP is a state of the art wideband high power operational amplifier designed to drive resistive, capacitive, or inductive loads. For optimum linearity the output stage is biased for class A/B operation. Feed forward technology is used to obtain wide bandwidth and excellent DC performance, but constricts use to inverting mode only. External compensation allows the user to obtain both high gain and wide bandwidth. Use of a heatsink is required to realize the SOA.

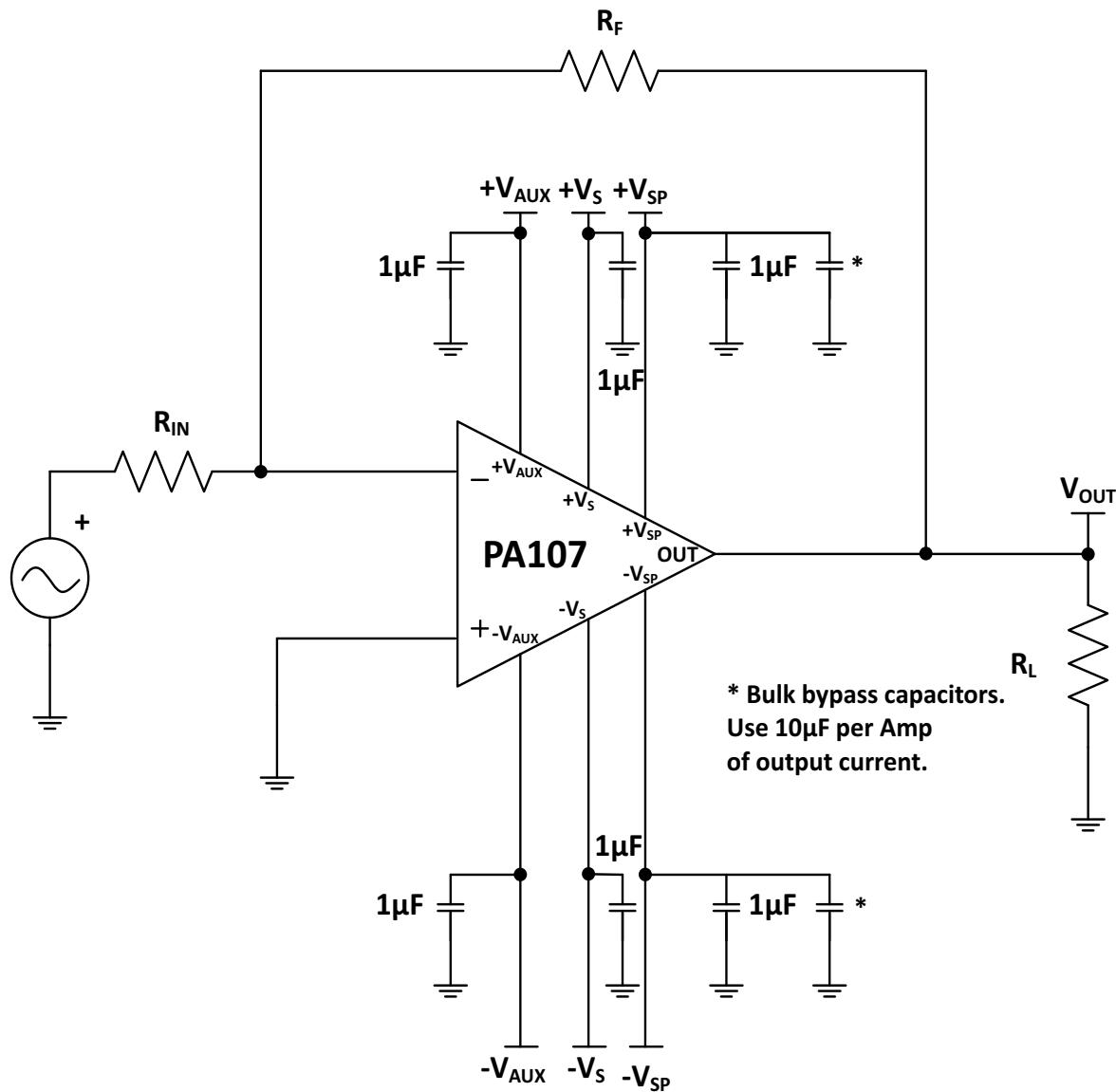
This hybrid integrated circuit uses thick film resistors, ceramic capacitors, and semiconductors to maximize reliability, minimize size, and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 12 pin SIP occupies only 2 square inches. The use of compressible insulation washers voids the warranty.

Figure 1: Equivalent Schematic



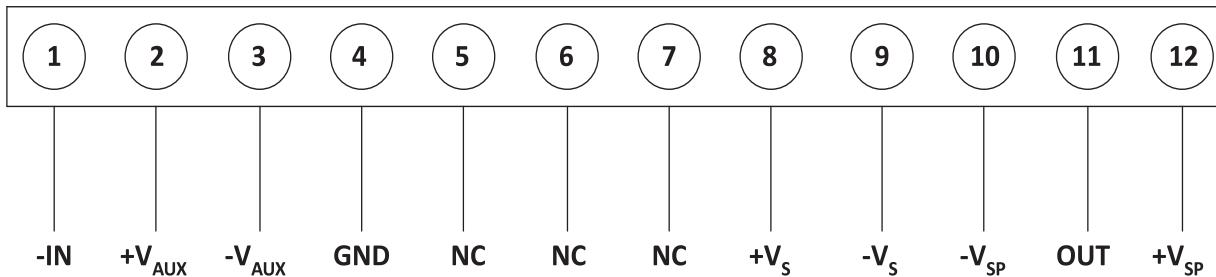
TYPICAL CONNECTION

Figure 2: Typical Connection



PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Pin Number	Name	Description
1	-IN	The summing junction input for inverting operational amplifier.
2	+V _{AUX}	+10 V to +18 V Supply for Input Stage.
3	-V _{AUX}	-10 V to -18 V Supply for Input Stage.
4	GND	Ground
5, 6, 7	NC	No connection.
8	+V _S	The positive supply rail.
9	-V _S	The negative supply rail.
10	-V _{SP}	-20V to -160V Supply for Output Source Follower. Short to pin 9.
11	OUT	The output. Connect this pin to load and to the feedback resistors.
12	+V _{SP}	+20V to +160V Supply for Output Source Follower. Short to pin 8.

The PA107 is constructed from MOSFET devices. ESD handling procedures must be observed. The substrate contains beryllia (BeO). Do not crush, machine or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

CAUTION

SPECIFICATIONS

All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and $T_C = 25^\circ\text{C}$. Unless otherwise noted test conditions are: $V_S = 100\text{V}$, $-V_S = -100\text{V}$, $V_{AUX} = 15\text{V}$, $-V_{AUX} = -15\text{V}$, $V_{SP} = V_S$, and $-V_{SP} = -V_S$.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, total $+V_S$ to $-V_{SP}$, $+V_{SP}$ to $-V_{SP}^2$	$+V_S$ to $-V_S$	40	200	V
Supply Voltage, $-V_S^2$	$-V_S$	-20	-160	V
Supply Voltage, $-V_{AUX}$ to $+V_{AUX}$	$-V_{AUX}$ to $+V_{AUX}$	20	36	V
Supply Voltage, $-V_{AUX}$	$-V_{AUX}$	-10	-18	V
Output Current, steady state (within SOA)	I_O		1.5	A
Output Current, peak (within SOA)	I_O		5	A
Power Dissipation, internal, DC	P_D		62.5	W
Input Voltage	V_{IN}	$-V_{AUX} + 2$	$+V_{AUX} - 2$	V
Temperature, pin solder, 10s			260	$^\circ\text{C}$
Temperature, junction ¹	T_J		150	$^\circ\text{C}$
Temperature Range, storage		-55	125	$^\circ\text{C}$
Operating Temperature, case	T_C	-40	85	$^\circ\text{C}$

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
2. Either rail may not exceed 160 V from ground reference.

INPUT

Parameter	Test Conditions	Min	Typ	Max	Units
Offset Voltage			5	10	mV
Offset Voltage vs. Temperature			10		$\mu\text{V}/^\circ\text{C}$
Bias Current, initial ¹			300		pA
Input Resistance, DC		13			$\text{G}\Omega$
Input Capacitance			2		pF
Input Voltage Range		$-V_{AUX} + 2$		$+V_{AUX} - 2$	V
Noise, RTI	1k Ω source, 500 kHz BW, $A_{CL} = 101$		13		nV/ $\sqrt{\text{Hz}}$

1. Doubles for every 10°C of case temperature increase.

GAIN

Parameter	Test Conditions	Min	Typ	Max	Units
Open Loop Gain @ DC			140		dB
Open Loop Gain @ 1MHz			40		dB
Power Bandwidth, 170Vp-p	Full temp range	2			MHz

OUTPUT

Parameter	Test Conditions	Min	Typ	Max	Units
Voltage Swing	Load = 10 MΩ 10 pF		187		V _{P-P}
Voltage Swing	I _O = 1.5A	±V _S -10			V
Current, peak				±5	A
Current, Steady State (within SOA)				±1.5	A
Slew Rate, 25% to 75%		2500	3000		V/μs
Settling Time to 0.1%			12		μs

POWER SUPPLY

Parameter	Test Conditions	Min	Typ	Max	Units
Voltage, +V _S , +V _{SP}		20		100	V
Voltage, -V _S , -V _{SP}		-100		-20	V
Voltage, +V _{AUX}		10	15	18	V
Voltage, -V _{AUX}		-18	-15	-10	V
Current, Quiescent, +V _S , +V _{SP}		20	30	35	mA
Current, Quiescent, -V _S , -V _{SP}		20	30	35	mA
Current, Quiescent, -V _{AUX}			19	21	mA
Current, Quiescent, +V _{AUX}			19	21	mA

THERMAL

Parameter	Test Conditions	Min	Typ	Max	Units
Resistance, AC, junction to case ¹				1.5	°C/W
Resistance, DC junction to case				2	°C/W
Resistance, junction to air				30	°C/W
Temperature Range, case		-25		85	°C

1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

Note: +V_S and -V_S denote the positive and negative supply voltages to the output stages. +V_{AUX} and -V_{AUX} denote the positive and negative supply voltages to the input stages.

TYPICAL PERFORMANCE GRAPHS

Figure 4: High Voltage Small Signal Response

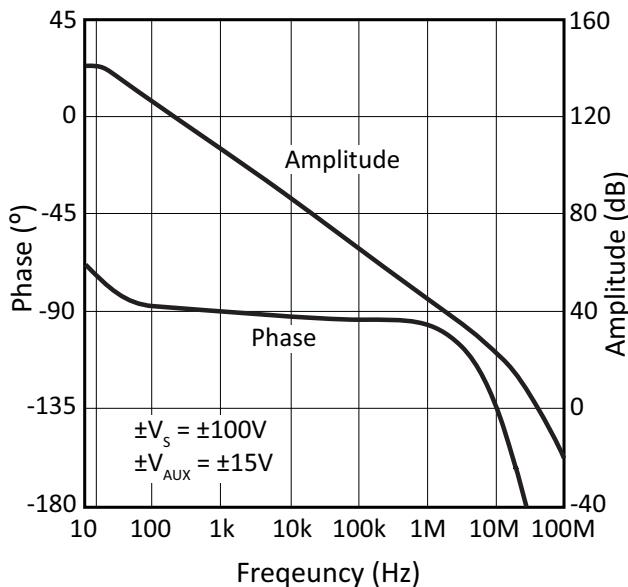


Figure 5: Low Voltage Small Signal Response

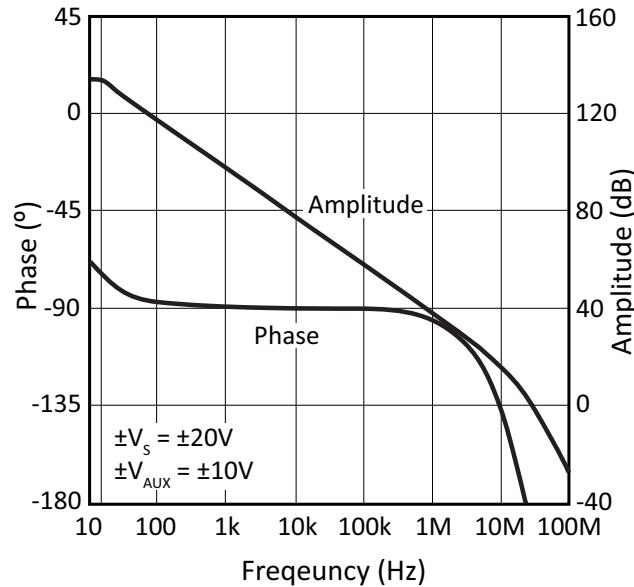


Figure 6: High Voltage Supply Current

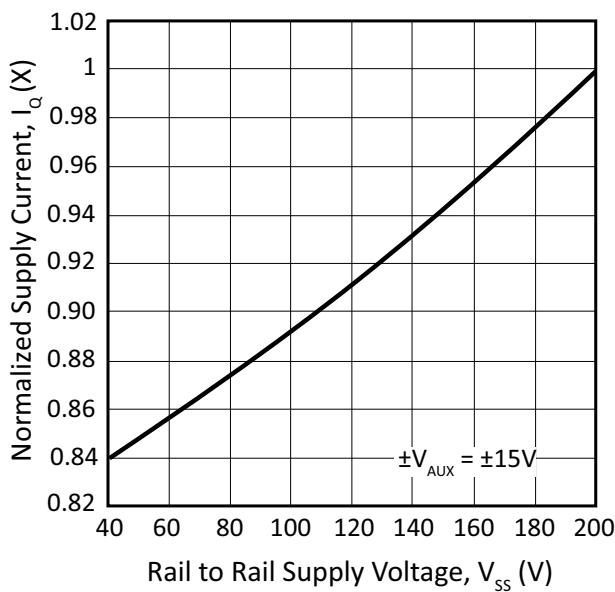


Figure 7: Response to 500 kHz Square Wave

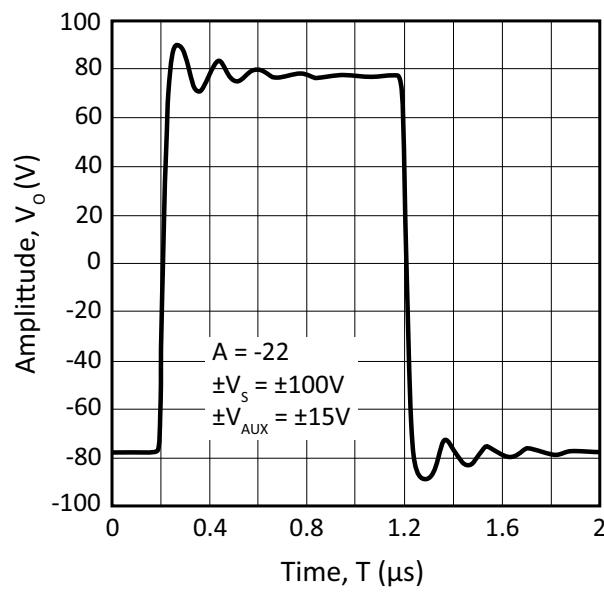


Figure 8: Positive Slew

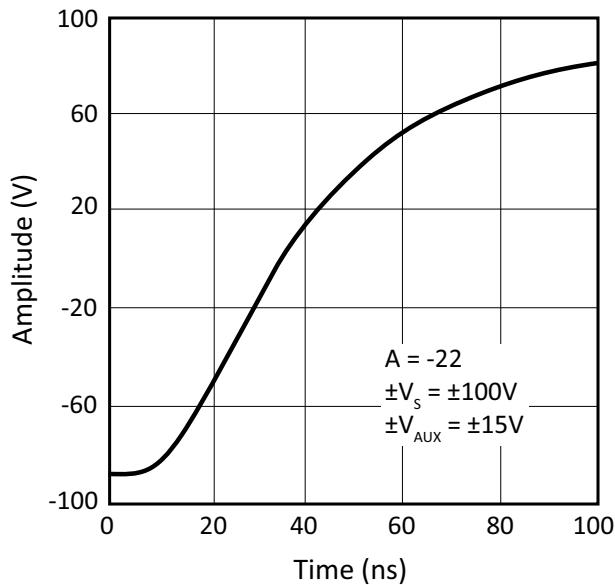


Figure 9: Negative Slew

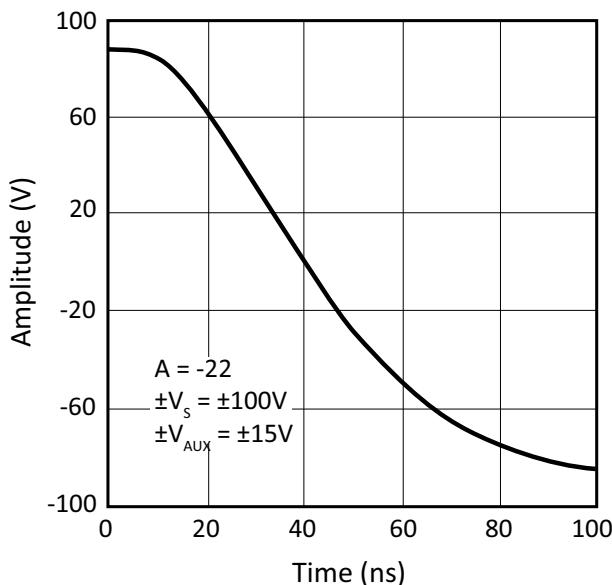


Figure 10: Power Derating

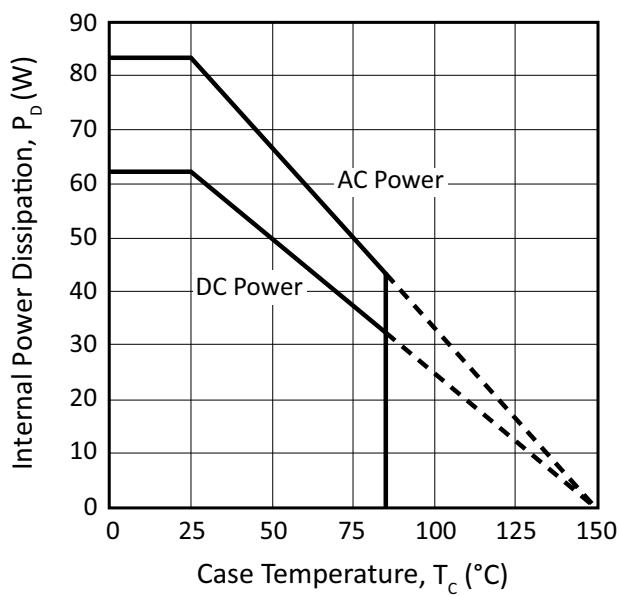


Figure 11: High Voltage Current vs. Temperature

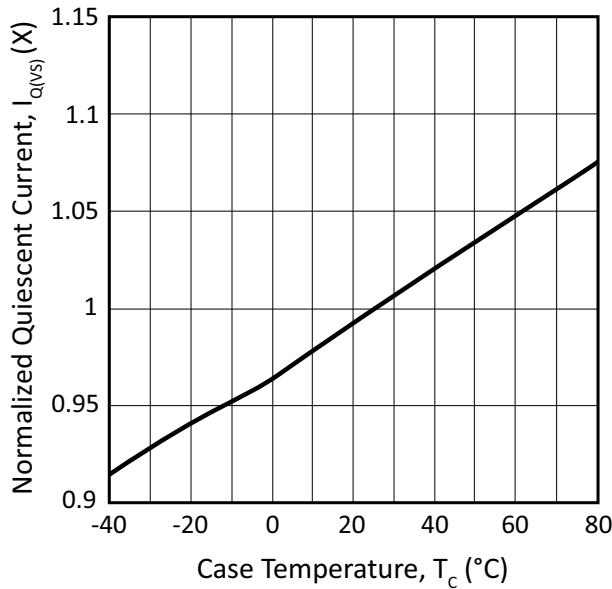


Figure 12: High Voltage Current vs. Frequency

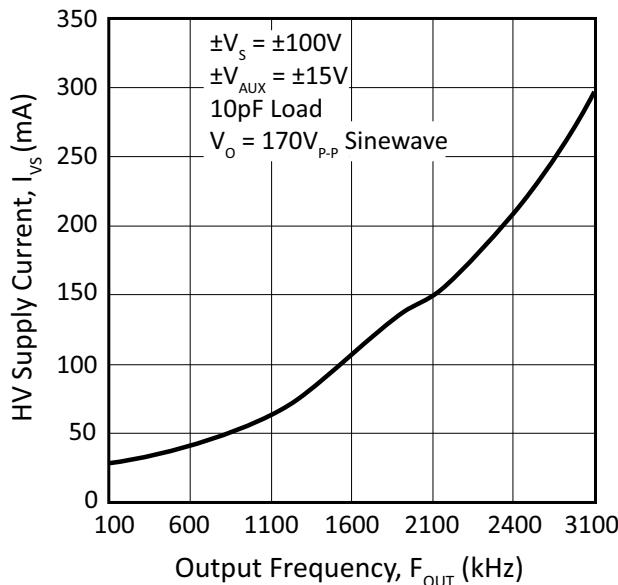


Figure 13: Power Supply Rejection ($\pm V_s$)

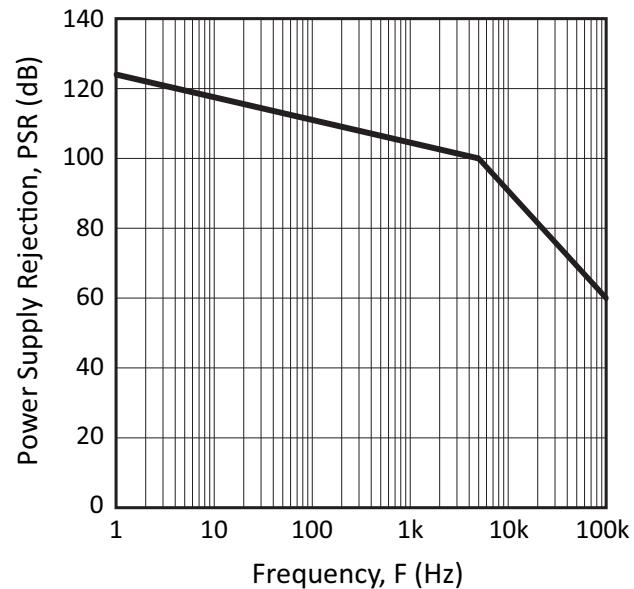


Figure 14: Power Supply Rejection ($\pm V_{AUX}$)

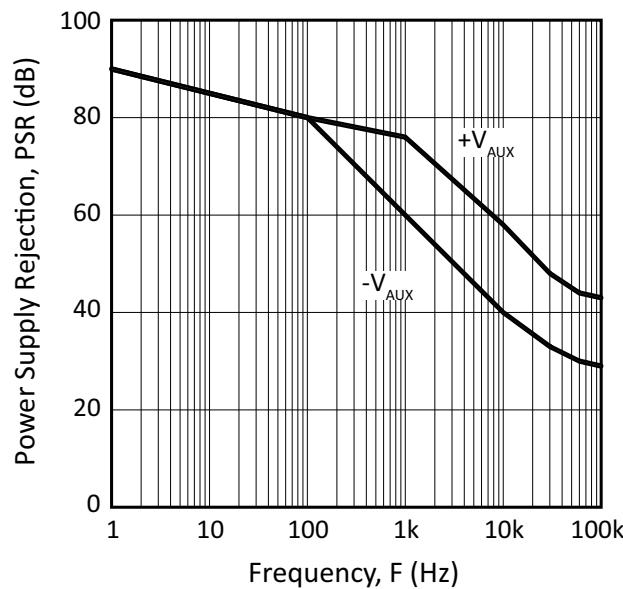
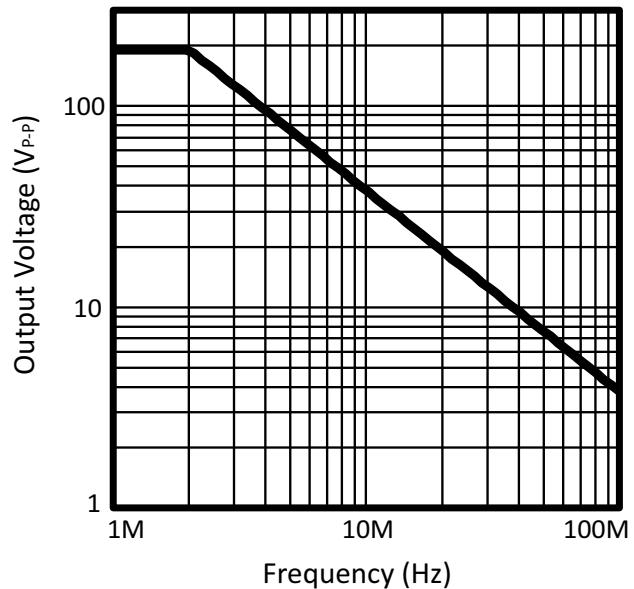


Figure 15: Power Response



SAFE OPERATING AREA (SOA)

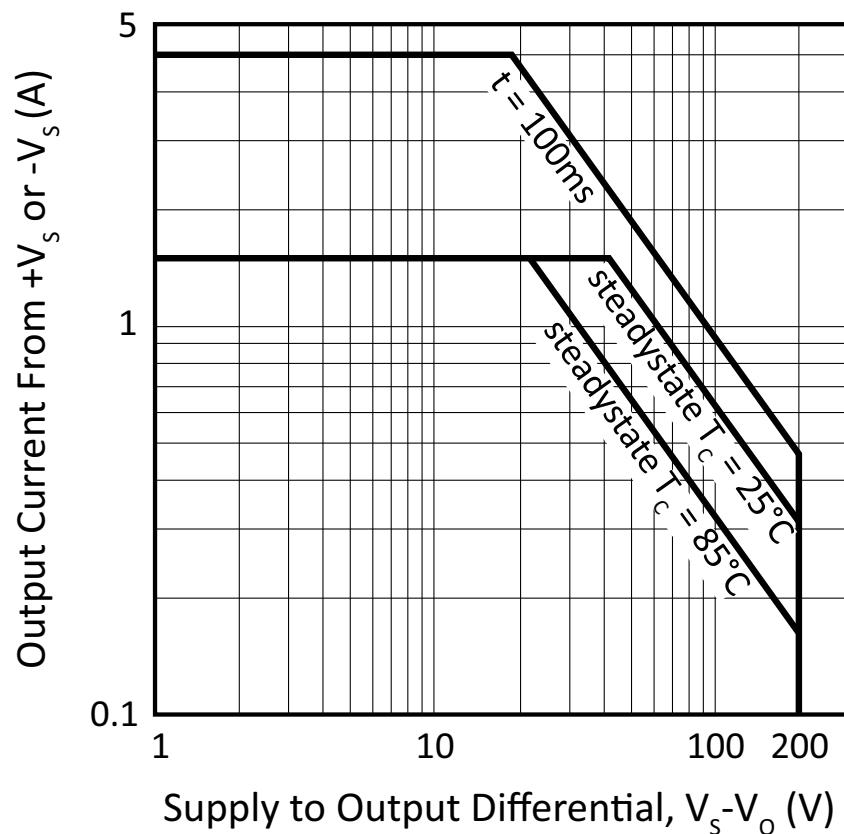
The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load. This is not the same as the absolute maximum internal power dissipation listed elsewhere in the specification since the quiescent power dissipation is significant compared to the total.

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

Note: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

Figure 16: SOA

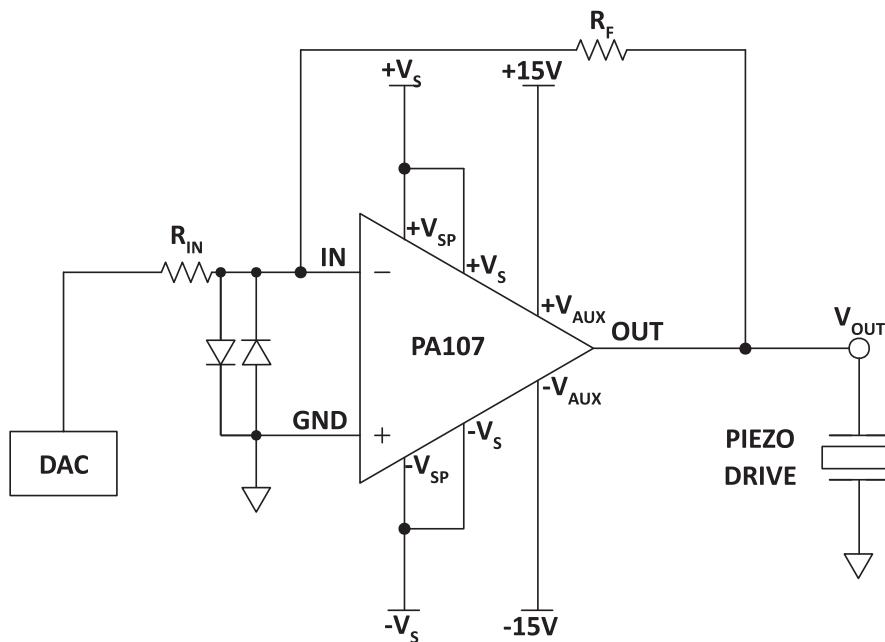


GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology's complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

TYPICAL APPLICATION

Figure 17: Typical Application



In order to achieve the highest speed with limited space short circuit protection and thermal protection were sacrificed. Do not short the output. Note that if current limiting at 1.5 A could be used, and the output was shorted, internal dissipation would be 150 W. This would still destroy the amplifier, albeit more slowly.

When the output stage is driven into saturation, the amplifier supply current may pull up to 1.5 A peaks, even unloaded. If there is any risk of non-linear operation, input protection diodes MUST be used as shown in the Typical Application diagram (figure 17). This will prevent high supply current peaks in most applications.

INTERNAL POWER DISSIPATION AND HEATSINK SELECTION

With the unique combination of high voltage and speed of the PA107, traditional formulas for heatsink selection will falsely lower the apparent power handling capability of this amplifier. To predict operating temperatures use the following procedure:

Find internal dissipation (PD) resulting from driving the load. Refer to Apex Applications Note 1, General Operating Considerations, paragraph 7. Find total quiescent power (PD_Q) by multiplying 0.035 A by V_{SS} (total

supply voltage), plus 0.021 times the total V_{AUX} ($+V_{AUX} + |-V_{AUX}|$). Find output stage quiescent power (PD_{QOUT}) by multiplying 0.001 by V_{SS} .

Calculate a heatsink rating which will maintain the case at 85°C or lower.

$$R_{\emptyset SA} = \frac{T_C - T_A}{PD + PD_Q} - 0.1 \frac{^{\circ}C}{W}$$

Where:

T_C = maximum case temperature allowed

T_A = maximum ambient temperature encountered

Calculate a heatsink rating which will maintain output transistor junctions at 150°C or lower.

$$R_{\emptyset SA} = \frac{T_J - T_A - (PD + PD_{QOUT}) \cdot R_{\emptyset JC}}{PD + PD_Q} - 0.1 \frac{^{\circ}C}{W}$$

Where:

T_J = maximum junction temperature allowed.

$R_{\emptyset JC}$ = AC or DC thermal resistance from the specification table.

Use the larger heatsink of these two calculations.

REACTIVE LOADS

The PA107DP is stable at a gain of 20 or above when driving either inductive or capacitive loads. However an inductor is essentially a short circuit at DC, therefore there must be enough resistance in series to keep low frequency power within ratings.

Driving a 1nF capacitor with a 2.3 MHz sine wave, the power bandwidth frequency, results in 2.6 A_{P-P}. The power dissipated in the amplifier while driving a purely capacitive load is given by the formula:

$$P = \frac{2V_{PK}V_S}{\pi X_C}$$

$$P = \frac{2I_{PK}V_S}{\pi}$$

Where:

V_{PK} = Peak Voltage

V_S = Supply Voltage

X_C = Capacitive Reactance

Notice that the power increases as V_{PK} increases, such that the maximum internal dissipation occurs when V_{PK} is maximum. The power dissipated in the amplifier while driving 1 nF at 2.3 MHz would be 82.76 W. This would not be a good thing to do! But driving 1 nF at 1 MHz at 180V_{P-P} would result in 36 W, which could be within the AC power rating.

This formula is optimistic; it is derived for an ideal class B amplifier output stage.

FEEDBACK CONSIDERATIONS

The output voltage of an unloaded PA107DP can easily go as high as 95 V. All of this voltage can be applied across the feedback resistor, so the minimum value of a $\frac{1}{2}$ W resistor in the feedback is 18050Ω . Practically, 20K is the minimum value for a un-derated $\frac{1}{2}$ W feedback resistor.

In order to provide the maximum slew rate, power bandwidth, and usable gain bandwidth, the PA107DP is not designed to be unity gain stable. It is necessary to add external compensation for gains less than 20. Often lower performance op-amps may be stabilized with a capacitor in parallel with the feedback resistor. This is because there is effectively one additional pole affecting the response. In the case of the PA107DP, however, there are multiple poles clustered near 30 MHz; therefore this approach does not work. A method of compensation that works is to choose a feedback capacitor such that the time constant of the feedback capacitor times the feedback resistor is greater than 33 nanoseconds. Also install a capacitor from pin 1 to ground, the summing junction, greater than 20 times as large as the feedback capacitor. The feedback capacitor or summing junction capacitor without the other will degrade stability and often cause oscillation. With the compensation described the closed loop bandwidth will be the reciprocal of $2\pi f_{FB}$.

Alternatively, at the expense of noise and offset, the amplifier can be stabilized by a resistor across the summing junction such that the parallel combination of the input resistor and summing junction resistor is less than a twentieth of the value of the feedback resistor. Note that this will increase noise and offset by up to 20 times the RTI values, but with 10 mV max offset and $13 \text{ nV}/(\text{Hz})^{1/2}$ noise, performance will be acceptable for many applications.

As seen by the very small values of capacitance used in compensation for low gain, stray feedback capacitance and/or summing junction capacitance can have a VERY large effect on performance. Therefore stray capacitance must be minimized in the layout. The summing junction lead must be as short as possible, and ground plane must be kept away from the summing junction lead.

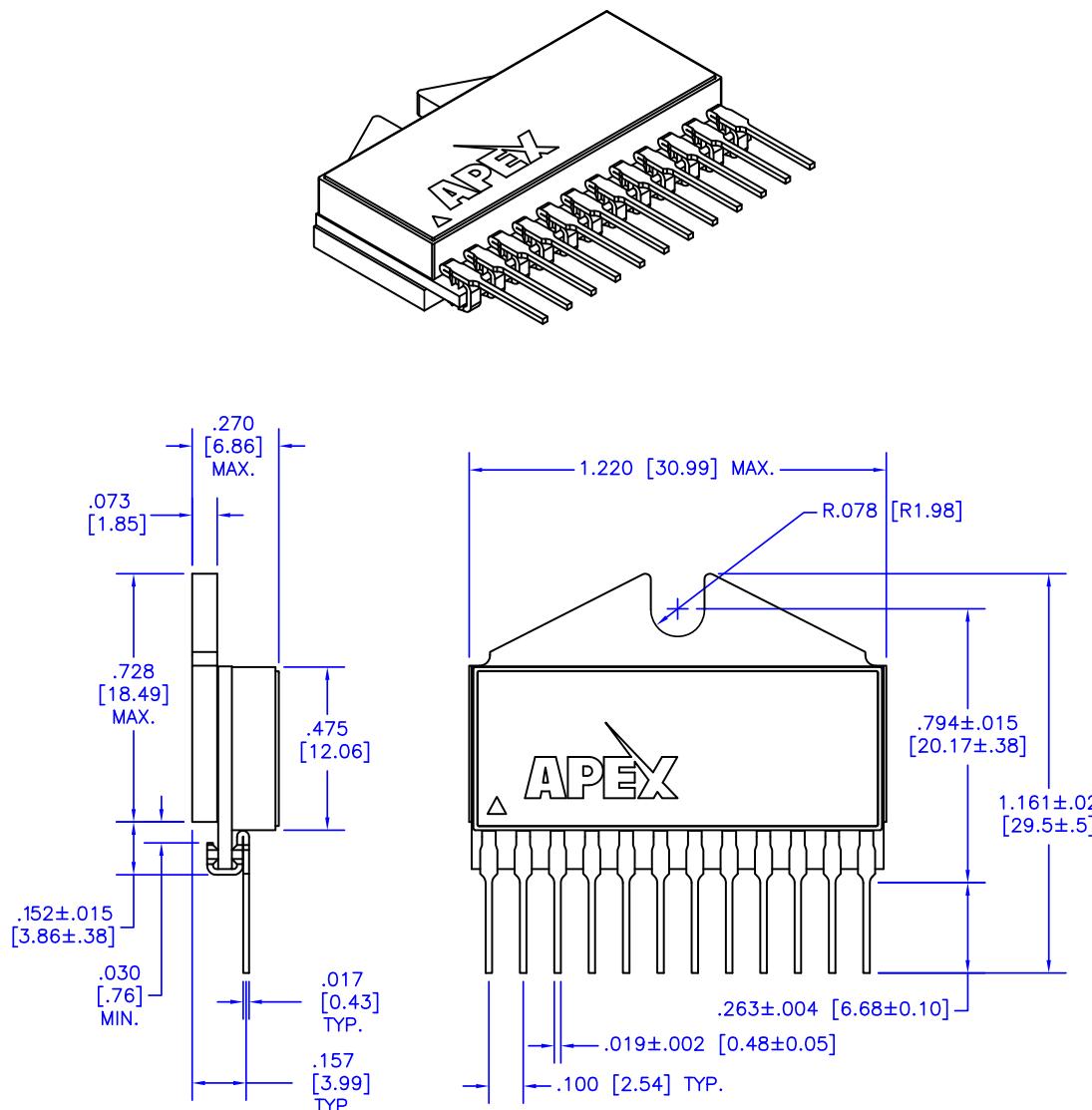
SLEW RATE AND FULL POWER BANDWIDTH

In the PA107DP the slew rate is measured from the 25% point to the 75% point of a $180\text{V}_{\text{P-P}}$ square wave. Slew rate is measured with no load and with auxiliary supplies at a nominal ± 15 V and V_S supplies at a maximum ± 100 V.

Power bandwidth is defined as the highest frequency at which an unloaded amplifier can have an undistorted sine wave at full power as its output. This frequency can be calculated as the slew rate divided by π times the peak to peak amplitude; which would be 4.7 MHz for the PA107DP. Unfortunately running full output at this frequency causes internal dissipation of up to 107 W, well over the power limits for the PA107DP. Cutting the frequency to 2 MHz reduces internal dissipation to 34 W, acceptable with a good heatsink.

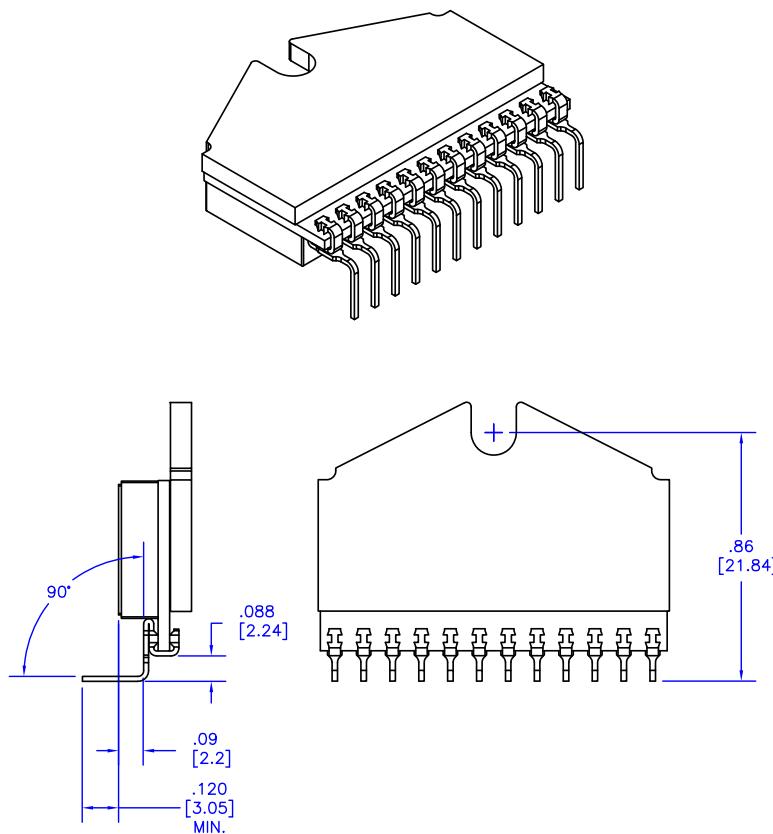
PACKAGE OPTIONS

PACKAGE STYLE DP



NOTES:

1. Dimensions are inches & [mm].
2. Triangle on lid denotes pin 1.
3. Pins: Alloy 510 phosphor bronze plated with matte tin (150 – 300 μ) over nickel (50 μ max.) underplate.
4. Package: Vectra liquid crystal polymer, black
5. Epoxy-sealed & ultrasonically welded non-hermetic package.
6. Package weight: .367 oz. [11.41 g]

PACKAGE STYLE EE**NOTES:**

1. Dimensions are inches & [mm].
2. For other dimensions and information on this package with unformed leads, see package DP.