

CPE CPU – A Soft-Core RISC-V Processor

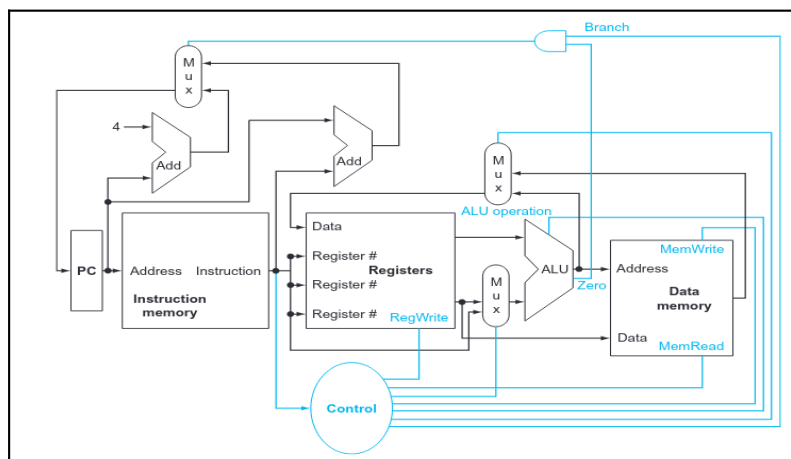
Introduction:

HAL-RV32 is a soft-core processor designed designed to implement the RV32I instruction set. The processor implements the relevant hardware pertaining to the programming model within the RV32I specification.

Requirements:

1. The HAL-RV32 shall be compatible with the RV32I specification with the exception of FENCE, ECALL, and EBREAK.
2. I/O Connections
 1. Inputs
 1. The HAL-RV32 shall have a single clock input.
 2. The HAL-RV32 shall have an active high asynchronous reset input that will place the module in a initialized state wherein execution will begin at instruction 0.
 3. The HAL-RV32 shall have a data input bus that is 32 bits wide.
 2. Outputs
 1. The HAL-RV32 shall have an address output bus that is 32 bits wide.
 2. The HAL-RV32 shall have a data output bus that is 32 bits wide.
 3. The HAL-RV32 shall have an active high data read enable output line.
 4. The HAL-RV32 shall have an active high data write enable output line.
 5. The HAL-RV32 shall have a instruction address output bus that is 32 bits wide.
3. Registers
 1. The HAL-RV32 shall have 32 general purpose registers that are 32 bits wide. These are set to 0 upon reset.
 2. The HAL-RV32 shall have a 32 bit program counter register that is set to 0 upon reset.

System Overview:



Overview of module is shown in figure above and modifications will be made to it. Figure taken from Computer Organization and Design (Patterson and Hennessy). Note that the instruction memory and data memory blocks are outside the scope of this module.

References:

Computer Organization and Design (RISC-V Edition), Patterson and Hennessy.

http://home.ustc.edu.cn/~louwenqi/reference_books_tools/Computer%20Organization%20and%20Design%20RISC-V%20edition.pdf

RISK-V ISA Specification Version 2.2, RISC-V Foundation.

<https://riscv.org/wp-content/uploads/2017/05/riscv-spec-v2.2.pdf>

CMOD-A7 35T Development Board, Digilent.

<https://digilent.com/shop/cmod-a7-breadboardable-artix-7-fpga-module/>