XInC2 miniDev

Development Board
User Guide

Version 1.0

Created by
Cory Duce
27 October 2008

Last Modified
29 October 2008

10150 - 100 Street, Suite 900
Edmonton, Alberta, Canada, T5J 0P6
Phone: (780) 425-6511
Fax: (780) 425-7006
Inquiries: duce@eleveneng.com
web: www.elevenengineering.com

0100 Overview

The XInC2 miniDev is a small development board in a module form factor intended for easy prototyping and development with the XInC2 microprocessor. The module form factor uses standard 0.1" headers to allow development on a bread board, as well as integration into a custom design.

This document is a guide to using the XInC2 miniDev board. A complete description of the XInC2 processor can be found in the *XInC2 User Guide*.

0101 XInC2 Processor

XInC2 (pronounced "zinc") is a cost-effective and flexible multithreaded processor. XInC2 has a low-power, RISC processor architecture supporting an extensive peripheral library. The multithreaded, pipelined design of the XInC2 processor core executes concurrent, real-time programs with guaranteed performance, giving it a marked advantage over conventional serial processor implementations. The multithreaded programming model simplifies software development and testing, significantly reducing time to market. Firmware is also more intuitive to understand, enabling easy maintenance. The XInC2 hardware approach to real-time event handling eliminates the need for a real-time operating system (RTOS) scheduling kernel.

XInC2 is a 16-bit pipelined RISC processor with 8 hardware threads. The 8 threads behave as 8 independent processors, each with access to main memory and the peripheral bus. With XInC2 the disadvantages of serial interrupt-based processors such as context swapping, task scheduling, unpredictable execution times, and RTOS overheads are avoided. The 8 thread processors share hardware resources with the exception of each thread's dedicated register set. Thus for the hardware cost of one processor, XInC2 provides 8. This approach results in outstanding MIPS/gate efficiency.

Each hardware thread is scheduled to execute at 1/8 of the system clock, thus removing the overhead of an RTOS. Firmware can be written as 8 independent programs. Each program runs on its own thread processor. Using simple interface conventions, programs on individual threads execute independently from each other. This allows for easy integration of firmware from different providers or team members.

Features The XInC2 processor include the following features:

- Independent execution of threads allows easy delineation and allocation of available processor cycles to unrelated applications.
- One or more threads can execute operations on a common data set
- Each thread has independent access to the peripheral bus.
- Firmware can be designed to assign one thread to service one or more Input/Output peripherals.
- Guaranteed response time to real-time events is realized via the elimination of interrupts and the division of task among the thread processors.
- A hardware peripheral library is provided that contains many common peripherals.
- Mathematical functions including multiplication, population count, bit reverse, and pack operations.
- Hardware semaphore mechanism for shared resource management.
- Inter-thread communication through a shared memory structure.

0200 Pinout Diagram

Figure 1 shows the dimensions and pinout of the XInC2 miniDev board. By populating only the headers on the two long sides, the miniDev can straddle two breadboards for development.

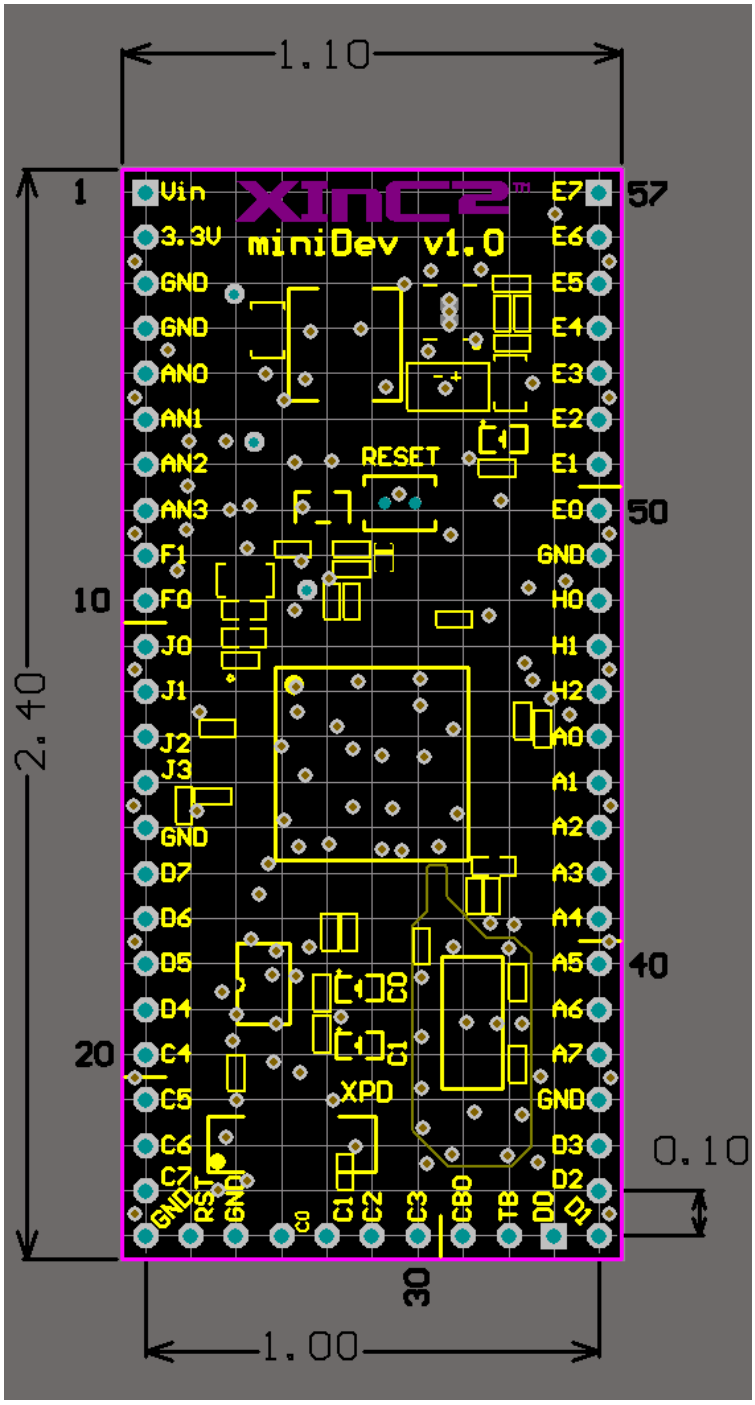


Figure 1 XInC2 miniDev board pinout. Dimensions in inches.

0300 Pin Descriptions

Table 1 shows the main and alternate functions for the pins on the miniDev board. Refer to the *XInC2 User Guide* for a complete description of IO and peripheral functions.

Table 1 XInC2 miniDev board pin descriptions

Pin	PCB Label	Main Function		Alternate Function	
		Name	Description	Name	Description
1	Vin	Unregulated Voltage Input	0.9 -3.3V input		
2	3.3V	Regulated 3.3V output	Output of onboard boost regulator	Regulated 3.3V input	Main supply input when onboard regulator is not used
3	GND				
4	GND				
5	AN0	AN0	ADC input 0		
6	AN1	AN1	ADC input 1		
7	AN2	AN2	ADC input 2		
8	AN3	AN3	ADC input 3		
9	F1	PF1	GPIO	SDIO2	DASI Data 2
10	F0	PF0	GPIO	SDIO1	DASI Data 1
11	J0	PJ0	GPIO	SDIO0	DASI Data 0
12	J1	PJ1	GPIO	LRCK	DASI Left Right Frame Clock
13	J2	PJ2	GPIO	SCLK	DASI Serial Clock
14	J3	PJ3	GPIO	MCLK	DASI Master Clock
15	GND				
16	D7	PD7	GPIO	TMRA3	Timer A 3 Input/Output
17	D6	PD6	GPIO	TMRA2	Timer A 2 Input/Output
18	D5	PD5	GPIO	TMRA1	Timer A 1 Input/Output
19	D4	PD4	GPIO	TMRA0	Timer A 0 Input/Output
20	C4	PC4	GPIO		
21	C5	PC5	GPIO		
22	C6	PC6	GPIO		
23	C7	PC7	GPIO		
24	GND				
25	RST	Reset	Active low reset		
26	GND				
27	C0	PC0	GPIO		
28	C1	PC1	GPIO		
29	C2	PC2	GPIO		
30	C3	PC3	GPIO		
31	CBO	CBO	Clock Buffer Output		
32	TB	TMRB	Timer B Input/Output		
33	D0	PD0	GPIO	MISO1	SPI 1 - Master In Slave Out
34	D1	PD1	GPIO	MOSI1	SPI 1 - Master Out Slave In
35	D2	PD2	GPIO	SCK1	SPI 1 - Serial Clock
36	D3	PD3	GPIO	SEN1	SPI 1 - Slave Enable
37	GND				
38	A7	PA7	GPIO		
39	A6	PA6	GPIO		
40	A5	PA5	GPIO		
41	A4	PA4	GPIO		
42	A3	PA3	GPIO		
43	A2	PA2	GPIO		
44	A1	PA1	GPIO		
45	A0	PA0	GPIO		
46	H2	PH2	GPIO	BB0I	Baseband Unit 0 Input
47	H1	PH1	GPIO	BB0O	Baseband Unit 0 Output
48	H0	PH0	GPIO	BB0CLK	Baseband Unit 0 Clock
49	GND				
50	E0	PE0	GPIO		
51	E1	PE1	GPIO		
52	E2	PE2	GPIO		
53	E3	PE3	GPIO		
54	E4	PE4	GPIO		
55	E5	PE5	GPIO		
56	E6	PE6	GPIO		
57	E7	PE7	GPIO		

0400 Electrical Characteristics

NOTE! **The IO cells are NOT tolerant to 5V input.**

0401 Absolute Maximum Ratings

Symbol	Parameter	Condition	min	max	Units
Vin	Voltage on Pin 1	No external supply on Pin 2	-0.3	7.0	V
3.3V	Voltage on Pin 2	No external supply on Pin 1	0	3.6	V
Avin	Analog Input voltage on Pins[5..8]		0	1.8	V
VIO	Voltage on GPIO pin		0	3.6	V
SysClk	System Clock		0	100	MHz

0402 Recommended operating conditions

Symbol	Parameter	Condition	min	Typ	max	Units
Vin	Voltage on Pin 1	No external supply on Pin 2	0.9		3.0	V
3.3V	Voltage on Pin 2	No external supply on Pin 1		3.3		V
VIO	Voltage on GPIO pin				3.3	V

0500 Power Supply Configurations

The XInC2 miniDev board has two power supply pins:

- Pin 1 – Vin Input to TPS61020 boost converter
- Pin 2 – 3.3V Output of TPS61020 boost converter

Figure 2 shows how these connections are arranged. Power should not be supplied to both power supply pins at the same time.

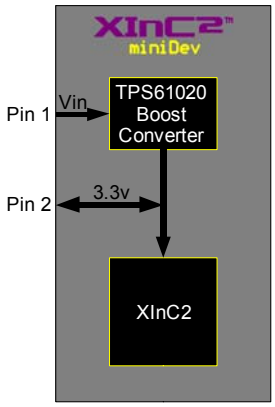
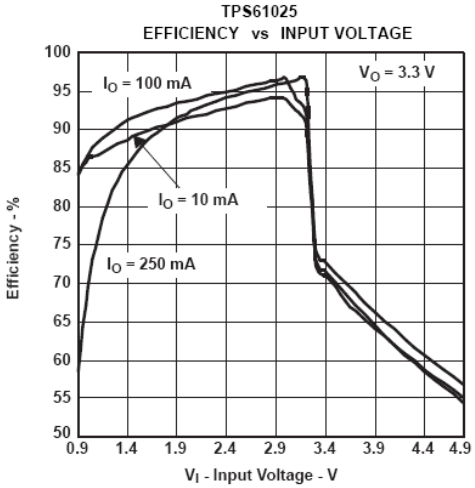


Figure 2 Onboard boost regulator

Using Internal TPS61020 Boost Converter

The XInC2 miniDev board includes an onboard high efficiency synchronous boost converter. The boost converter is included to allow for powering the miniDev from a one or two cell battery pack. The output of the boost converter is fixed at 3.3V. As well as powering the XInC2 processor, the output of the boost converter is available as an output on pin 2 for powering external devices that require 3.3V.

The TPS61020 operates most efficiently when 0.9V < Vin < 3.0V. When Vin exceeds 3.0V, the regulator switches to a linear regulator and operates at a lower efficiency. Operating the TPS61020 with Vin > 3.0V may cause the regulator to over heat. If the available supply voltage is greater than 3.0V, it is recommended to use an external regulator as described below. The following plot shows the relationship between the efficiency of the regulator and the input voltage, Vin.



Using External Regulator

An external regulator can be used to power the XInC2 miniDev board. To use and external regulator, pin 2 should be connected to a regulated 3.3V supply. Pin 1 should be left unconnected.

0600 Summary of Basic Peripherals

This section presents a very brief overview of some of the commonly used hardware interface peripherals on the XInC2 processor. A complete description of the operation of all XInC2 peripherals in contained in the XInC2 Users Guide.

0601 General Purpose IO

The XInC2 miniDev board has 41 general purpose input/output pins.

- Port A – 8 GPIO
- Port C – 8 GPIO
- Port D – 8 GPIO
- Port E – 8 GPIO
- Port F – 2 GPIO
- Port H – 3 GPIO
- Port J – 4 GPIO

The GPIO ports of XInC2 each have the capability to control input/output direction, output level, and to read the level applied at the pin associated with each I/O line. Some of the pins on GPIO ports are multiplexed with other peripheral modules to reduce the overall pin count. Table 1 shows the alternate function of multiplexed GPIO pins.

0602 Analog to Digital Converter

XInC2 has an on-chip 10-bit successive approximation analog-to-digital converter with all the biasing and sample-and-hold circuitry included. The full scale reference voltage is fixed at 1.8V on the module. The ADC can sample data from one of the four input channels. It has a built-in controller interface for continuous sampling of single or multiple channels. A power down mode is provided with less than 1µA of standby current.
The maximum input to the analog input pins is 1.8V.

- 10-bit resolution
- 4 Input Channels
- Low Power Dissipation (2mW)
- Power-Down Capability (1µA)
- Up to 44.64 kHz Conversion rate
- Continuous sampling capability

0603 Base Band Unit

The Baseband Unit (BBU) is designed to interface to many RF sections that use a digital bit stream for transmit and receive data. The BBU provides the following features:

- Configurable bit and word synchronization
- Automatic baud rate synchronization to the incoming bit stream
- Very fine baud rate generation
- RZ and NRZ encoding and decoding
- Asynchronous and synchronous clocking of data
- Optional 0V DC bias coding over 16 bits
- Optional 4 bit run length coding
- Automatic error correction of 3, 2, or 1 bit errors in every 16 bit code word, depending on data rate used.
- Firmware interface with the ability to gather statistics on the number of bit errors

XInC2 contains two Baseband Units. Only BBU0 is brought out to pins on the miniDev board header.

0604 Serial Peripheral Interface

The serial peripheral interface (SPI) is a high-speed synchronous serial port. It allows a serial bit stream of 8 bits to be shifted into and out of an attached device. Data is clocked in and out most significant bit first.

XInC2 contains two SPI peripherals. SPI0 and SPI1 function identically but they have different uses in a XInC2 system. SPI0 is an integral part of the XPD port. In the normal case a developer should use SPI1 to communicate to additional SPI devices. This allows the XPD port to be dedicated to debug and diagnostics.

0605 DASI

The Digital Audio Serial Interface (DASI) allows XInC2 to connect to digital audio devices conforming to the Inter-IC Sound (I2S) specification (and variations).

The DASI is equipped with three digital audio channels, each allowing the transfer of a stereo audio bit stream, for a total of 6 channels of audio (two per transceiver). Master and slave modes are available. This peripheral allows XInC2 to generate or receive arbitrary bit depth audio. The only constraint for bit depth lies in slave mode, where incomplete bytes are lost on receive (if 20-bit data is received, the frames must be at least 24 bits long or the last nibble of the data will be lost).

As master, the DASI outputs the digital audio master clock (MCLK), the bit clock (SCK) and the Left-Right channel clock (LRCK) or frame clock. As slave the SCK and LRCK pins become inputs, but the MCLK pin may still be configured to provide a clock to an external device. MCLK is not required for slave operation.

All transceivers share the bit clock (SCK) configuration, sample depth configuration, master/slave selection, and block/poll selection. Each transceiver is individually enabled and configured for transmit or receive and Left Justified or I2S format data.

0606 Timer A

TimerA is a general purpose 16 bit timer. The timer consists of multiple operating modes with selectable clock source, four configurable capture/compare registers, configurable input modules, and configurable output modules.
The timer can be used to generate output waveforms such as a PWM signals, capture input signals on compare, trigger an event on a input signal transition, or be used as a configurable source of time.

0607 Timer B

TimerB is very similar to TimerA except that it only has two capture/compare registers and only one input and one output module.

0608 UART

The XInC2 processor does not contain a hardware UART peripheral. Firmware UART routines are available to allow GPIO pins to be used for this function.

0609 I²C

The XInC2 processor does not contain a hardware I^2C peripheral. Firmware I^2C routines are available to allow GPIO pins to be used for this function.

0700 XPD Interface

The XPD port is the physical interface that Program code is loaded into XInC2 for execution and it also provides a path for debugging during code development and also as a diagnostic port in the field. The XPD port functions are accomplished by using a synchronous serial port(SPI0) and some general purpose I/O pins.

Connection to the XPD port is made through a 8 pin mini connector on the XInC2 miniDev board.

Programming XInC2 The XPD port provides an interface to the XInC2 platform and a PC running the XInC2 Development Environment (XDE). The XPD allows the programmer to download code into RAM.

Debugging XInC2 Once the firmware is executing, the XPD port can be used with XInC2 development Environment(XDE) or a serial terminal for firmware debugging.

Real Time Diagnostic The XPD port can also be used for diagnostics in the field. It provides a convenient interface to a PC or other display device.

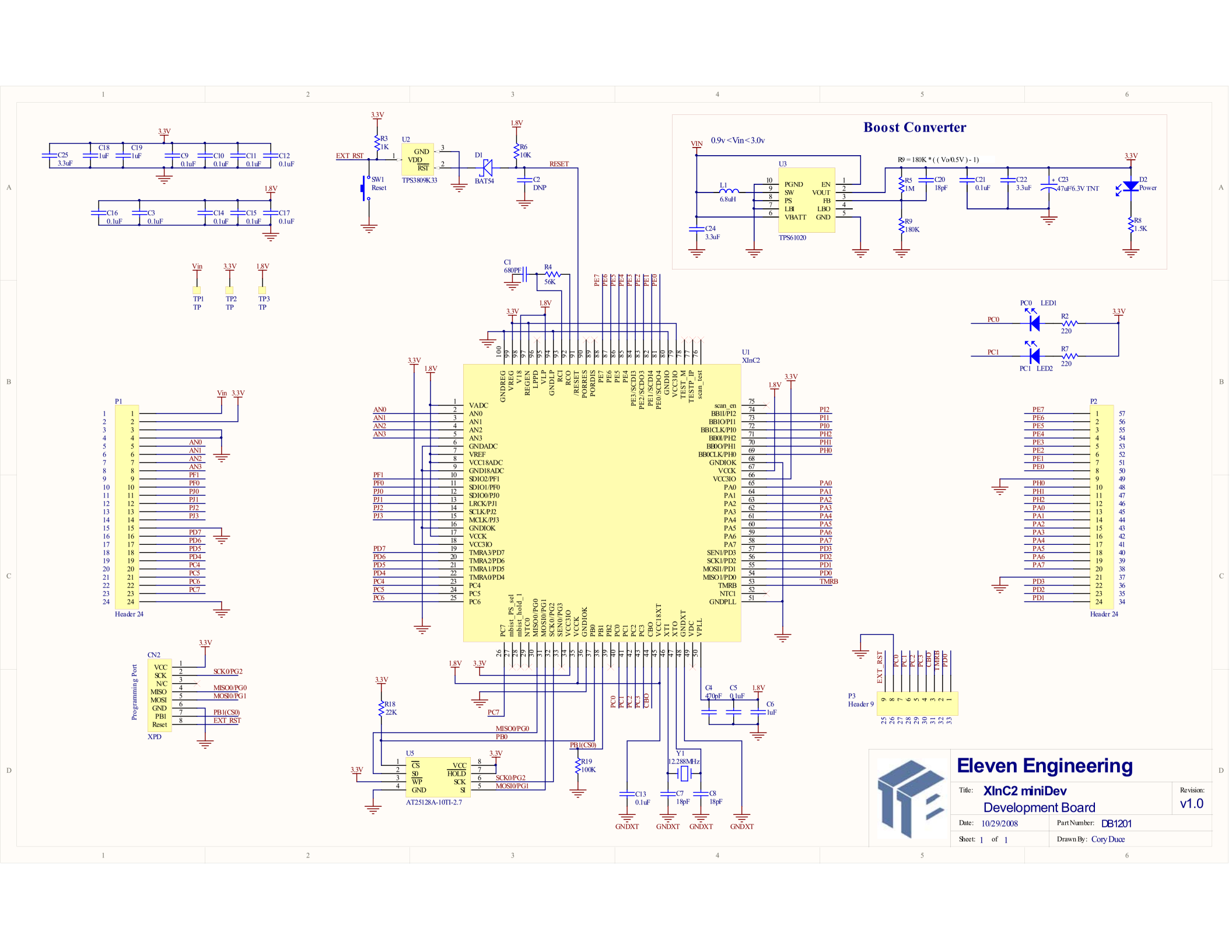
0800 Version History

10/29/2008 v1.0

- Initial release

0900 XInC2 miniDev Schematic

Eleven Engineering Incorporated
10150-100 street, suite 900
Edmonton, Alberta, Canada T5J 0P6
T: (780)425.6511 F: (780)425.7006
www.ElevenEngineering.com


Boost Converter
VIN
0.9v < Vin < 3.0v
R9 = 180K * ((Vo/0.5V) - 1)
U3
TPS61020
L1
6.8uH
C24
3.3uF
R5
1M
R9
180K
C20
18pF
C21
0.1uF
C22
3.3uF
C23
47uF/6.3V TNT
D2
Power
R8
1.5K
U1
XInC2
Eleven Engineering
Title: XInC2 miniDev
Development Board
Revision: v1.0
Date: 10/29/2008
Part Number: DB1201
Sheet: 1 of 1
Drawn By: Cory Duce