### 10.2.5 Signal multiplexing constraints

1. A given peripheral function must be assigned to a maximum of one package pin. Do not program the same function to more than one pin.
2. To ensure the best signal timing for a given peripheral's interface, choose the pins in closest proximity to each other.

## 10.3 Pinout

### 10.3.1 K64 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 144 LQFP | 144 MAP BGA | 121 XFBGA | 100 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| — | L5 | L7 | — | RTC_ WAKEUP_B | RTC_ WAKEUP_B | RTC_ WAKEUP_B | | | | | | | | |
| — | — | B11 | — | PTB12 | DISABLED | | PTB12 | UART3_ RTS_b | FTM1_CH0 | FTM0_CH4 | | FTM1_QD_ PHA | | |
| — | — | C11 | — | PTB13 | DISABLED | | PTB13 | UART3_ CTS_b | FTM1_CH1 | FTM0_CH5 | | FTM1_QD_ PHB | | |
| — | — | A11 | — | NC | NC | NC | | | | | | | | |
| — | M5 | — | — | NC | NC | NC | | | | | | | | |
| — | A10 | — | — | NC | NC | NC | | | | | | | | |
| — | B10 | K3 | — | NC | NC | NC | | | | | | | | |
| — | C10 | H4 | — | NC | NC | NC | | | | | | | | |
| 1 | D3 | E4 | 1 | PTE0 | ADC1_SE4a | ADC1_SE4a | PTE0 | SPI1_PCS1 | UART1_TX | SDHC0_D1 | TRACE_ CLKOUT | I2C1_SDA | RTC_ CLKOUT | |
| 2 | D2 | E3 | 2 | PTE1/ LLWU_P0 | ADC1_SE5a | ADC1_SE5a | PTE1/ LLWU_P0 | SPI1_SOUT | UART1_RX | SDHC0_D0 | TRACE_D3 | I2C1_SCL | SPI1_SIN | |
| 3 | D1 | E2 | 3 | PTE2/ LLWU_P1 | ADC0_DP2/ ADC1_SE6a | ADC0_DP2/ ADC1_SE6a | PTE2/ LLWU_P1 | SPI1_SCK | UART1_ CTS_b | SDHC0_ DCLK | TRACE_D2 | | | |
| 4 | E4 | F4 | 4 | PTE3 | ADC0_DM2/ ADC1_SE7a | ADC0_DM2/ ADC1_SE7a | PTE3 | SPI1_SIN | UART1_ RTS_b | SDHC0_ CMD | TRACE_D1 | | SPI1_SOUT | |
| 5 | E5 | E7 | — | VDD | VDD | VDD | | | | | | | | |
| 6 | F6 | F7 | — | VSS | VSS | VSS | | | | | | | | |
| 7 | E3 | H7 | 5 | PTE4/ LLWU_P2 | DISABLED | | PTE4/ LLWU_P2 | SPI1_PCS0 | UART3_TX | SDHC0_D3 | TRACE_D0 | | | |
| 8 | E2 | G4 | 6 | PTE5 | DISABLED | | PTE5 | SPI1_PCS2 | UART3_RX | SDHC0_D2 | | FTM3_CH0 | | |
| 9 | E1 | F3 | 7 | PTE6 | DISABLED | | PTE6 | SPI1_PCS3 | UART3_ CTS_b | I2S0_MCLK | | FTM3_CH1 | USB_SOF_ OUT | |

| 144 LQFP | 144 MAP BGA | 121 XFBGA | 100 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | F4 | — | — | PTE7 | DISABLED | | PTE7 | | UART3_ RTS_b | I2S0_RXD0 | | FTM3_CH2 | | |
| 11 | F3 | — | — | PTE8 | DISABLED | | PTE8 | I2S0_RXD1 | UART5_TX | I2S0_RX_FS | | FTM3_CH3 | | |
| 12 | F2 | — | — | PTE9 | DISABLED | | PTE9 | I2S0_TXD1 | UART5_RX | I2S0_RX_ BCLK | | FTM3_CH4 | | |
| 13 | F1 | — | — | PTE10 | DISABLED | | PTE10 | | UART5_ CTS_b | I2S0_TXD0 | | FTM3_CH5 | | |
| 14 | G4 | — | — | PTE11 | DISABLED | | PTE11 | | UART5_ RTS_b | I2S0_TX_FS | | FTM3_CH6 | | |
| 15 | G3 | — | — | PTE12 | DISABLED | | PTE12 | | | I2S0_TX_ BCLK | | FTM3_CH7 | | |
| 16 | E6 | E6 | 8 | VDD | VDD | VDD | | | | | | | | |
| 17 | F7 | G7 | 9 | VSS | VSS | VSS | | | | | | | | |
| 18 | H3 | L6 | — | VSS | VSS | VSS | | | | | | | | |
| 19 | H1 | F1 | 10 | USB0_DP | USB0_DP | USB0_DP | | | | | | | | |
| 20 | H2 | F2 | 11 | USB0_DM | USB0_DM | USB0_DM | | | | | | | | |
| 21 | G1 | G1 | 12 | VOUT33 | VOUT33 | VOUT33 | | | | | | | | |
| 22 | G2 | G2 | 13 | VREGIN | VREGIN | VREGIN | | | | | | | | |
| 23 | J1 | H1 | 14 | ADC0_DP1 | ADC0_DP1 | ADC0_DP1 | | | | | | | | |
| 24 | J2 | H2 | 15 | ADC0_DM1 | ADC0_DM1 | ADC0_DM1 | | | | | | | | |
| 25 | K1 | J1 | 16 | ADC1_DP1 | ADC1_DP1 | ADC1_DP1 | | | | | | | | |
| 26 | K2 | J2 | 17 | ADC1_DM1 | ADC1_DM1 | ADC1_DM1 | | | | | | | | |
| 27 | L1 | K1 | 18 | ADC0_DP0/ ADC1_DP3 | ADC0_DP0/ ADC1_DP3 | ADC0_DP0/ ADC1_DP3 | | | | | | | | |
| 28 | L2 | K2 | 19 | ADC0_DM0/ ADC1_DM3 | ADC0_DM0/ ADC1_DM3 | ADC0_DM0/ ADC1_DM3 | | | | | | | | |
| 29 | M1 | L1 | 20 | ADC1_DP0/ ADC0_DP3 | ADC1_DP0/ ADC0_DP3 | ADC1_DP0/ ADC0_DP3 | | | | | | | | |
| 30 | M2 | L2 | 21 | ADC1_DM0/ ADC0_DM3 | ADC1_DM0/ ADC0_DM3 | ADC1_DM0/ ADC0_DM3 | | | | | | | | |
| 31 | H5 | F5 | 22 | VDDA | VDDA | VDDA | | | | | | | | |
| 32 | G5 | G5 | 23 | VREFH | VREFH | VREFH | | | | | | | | |
| 33 | G6 | G6 | 24 | VREFL | VREFL | VREFL | | | | | | | | |
| 34 | H6 | F6 | 25 | VSSA | VSSA | VSSA | | | | | | | | |
| 35 | K3 | J3 | — | ADC1_SE16/ CMP2_IN2/ ADC0_SE22 | ADC1_SE16/ CMP2_IN2/ ADC0_SE22 | ADC1_SE16/ CMP2_IN2/ ADC0_SE22 | | | | | | | | |
| 36 | J3 | H3 | — | ADC0_SE16/ CMP1_IN2/ ADC0_SE21 | ADC0_SE16/ CMP1_IN2/ ADC0_SE21 | ADC0_SE16/ CMP1_IN2/ ADC0_SE21 | | | | | | | | |
| 37 | M3 | L3 | 26 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | | | | | | | | |

| 144 LQFP | 144 MAP BGA | 121 XFBGA | 100 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 38 | L3 | K5 | 27 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | | | | | | | | |
| 39 | L4 | K4 | — | DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23 | DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23 | DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23 | | | | | | | | |
| 40 | M7 | L4 | 28 | XTAL32 | XTAL32 | XTAL32 | | | | | | | | |
| 41 | M6 | L5 | 29 | EXTAL32 | EXTAL32 | EXTAL32 | | | | | | | | |
| 42 | L6 | K6 | 30 | VBAT | VBAT | VBAT | | | | | | | | |
| 43 | — | — | — | VDD | VDD | VDD | | | | | | | | |
| 44 | — | — | — | VSS | VSS | VSS | | | | | | | | |
| 45 | M4 | H5 | 31 | PTE24 | ADC0_SE17 | ADC0_SE17 | PTE24 | | UART4_TX | | I2C0_SCL | EWM_OUT_b | | |
| 46 | K5 | J5 | 32 | PTE25 | ADC0_SE18 | ADC0_SE18 | PTE25 | | UART4_RX | | I2C0_SDA | EWM_IN | | |
| 47 | K4 | H6 | 33 | PTE26 | DISABLED | | PTE26 | ENET_1588_ CLKIN | UART4_ CTS_b | | | RTC_ CLKOUT | USB_CLKIN | |
| 48 | J4 | — | — | PTE27 | DISABLED | | PTE27 | | UART4_ RTS_b | | | | | |
| 49 | H4 | — | — | PTE28 | DISABLED | | PTE28 | | | | | | | |
| 50 | J5 | J6 | 34 | PTA0 | JTAG_TCLK/ SWD_CLK/ EZP_CLK | | PTA0 | UART0_ CTS_b/ UART0_ COL_b | FTM0_CH5 | | | | JTAG_TCLK/ SWD_CLK | EZP_CLK |
| 51 | J6 | H8 | 35 | PTA1 | JTAG_TDI/ EZP_DI | | PTA1 | UART0_RX | FTM0_CH6 | | | | JTAG_TDI | EZP_DI |
| 52 | K6 | J7 | 36 | PTA2 | JTAG_TDO/ TRACE_ SWO/ EZP_DO | | PTA2 | UART0_TX | FTM0_CH7 | | | | JTAG_TDO/ TRACE_ SWO | EZP_DO |
| 53 | K7 | H9 | 37 | PTA3 | JTAG_TMS/ SWD_DIO | | PTA3 | UART0_ RTS_b | FTM0_CH0 | | | | JTAG_TMS/ SWD_DIO | |
| 54 | L7 | J8 | 38 | PTA4/ LLWU_P3 | NMI_b/ EZP_CS_b | | PTA4/ LLWU_P3 | | FTM0_CH1 | | | | NMI_b | EZP_CS_b |
| 55 | M8 | K7 | 39 | PTA5 | DISABLED | | PTA5 | USB_CLKIN | FTM0_CH2 | RMII0_ RXER/ MII0_RXER | CMP2_OUT | I2S0_TX_ BCLK | JTAG_ TRST_b | |
| 56 | E7 | E5 | 40 | VDD | VDD | VDD | | | | | | | | |
| 57 | G7 | G3 | 41 | VSS | VSS | VSS | | | | | | | | |
| 58 | J7 | — | — | PTA6 | DISABLED | | PTA6 | | FTM0_CH3 | | CLKOUT | | TRACE_ CLKOUT | |
| 59 | J8 | — | — | PTA7 | ADC0_SE10 | ADC0_SE10 | PTA7 | | FTM0_CH4 | | | | TRACE_D3 | |
| 60 | K8 | — | — | PTA8 | ADC0_SE11 | ADC0_SE11 | PTA8 | | FTM1_CH0 | | | FTM1_QD_ PHA | TRACE_D2 | |
| 61 | L8 | — | — | PTA9 | DISABLED | | PTA9 | | FTM1_CH1 | MII0_RXD3 | | FTM1_QD_ PHB | TRACE_D1 | |

| 144 LQFP | 144 MAP BGA | 121 XFBGA | 100 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 62 | M9 | J9 | — | PTA10 | DISABLED | | PTA10 | | FTM2_CH0 | MII0_RXD2 | | FTM2_QD_PHA | TRACE_D0 | |
| 63 | L9 | J4 | — | PTA11 | DISABLED | | PTA11 | | FTM2_CH1 | MII0_RXCLK | I2C2_SDA | FTM2_QD_PHB | | |
| 64 | K9 | K8 | 42 | PTA12 | CMP2_IN0 | CMP2_IN0 | PTA12 | CAN0_TX | FTM1_CH0 | RMII0_RXD1/ MII0_RXD1 | I2C2_SCL | I2S0_TXD0 | FTM1_QD_PHA | |
| 65 | J9 | L8 | 43 | PTA13/ LLWU_P4 | CMP2_IN1 | CMP2_IN1 | PTA13/ LLWU_P4 | CAN0_RX | FTM1_CH1 | RMII0_RXD0/ MII0_RXD0 | I2C2_SDA | I2S0_TX_FS | FTM1_QD_PHB | |
| 66 | L10 | K9 | 44 | PTA14 | DISABLED | | PTA14 | SPI0_PCS0 | UART0_TX | RMII0_CRS_DV/ MII0_RXDV | I2C2_SCL | I2S0_RX_BCLK | I2S0_TXD1 | |
| 67 | L11 | L9 | 45 | PTA15 | DISABLED | | PTA15 | SPI0_SCK | UART0_RX | RMII0_TXEN/ MII0_TXEN | | I2S0_RXD0 | | |
| 68 | K10 | J10 | 46 | PTA16 | DISABLED | | PTA16 | SPI0_SOUT | UART0_CTS_b/ UART0_COL_b | RMII0_TXD0/ MII0_TXD0 | | I2S0_RX_FS | I2S0_RXD1 | |
| 69 | K11 | H10 | 47 | PTA17 | ADC1_SE17 | ADC1_SE17 | PTA17 | SPI0_SIN | UART0_RTS_b | RMII0_TXD1/ MII0_TXD1 | | I2S0_MCLK | | |
| 70 | E8 | L10 | 48 | VDD | VDD | VDD | | | | | | | | |
| 71 | G8 | K10 | 49 | VSS | VSS | VSS | | | | | | | | |
| 72 | M12 | L11 | 50 | PTA18 | EXTAL0 | EXTAL0 | PTA18 | | FTM0_FLT2 | FTM_CLKIN0 | | | | |
| 73 | M11 | K11 | 51 | PTA19 | XTAL0 | XTAL0 | PTA19 | | FTM1_FLT0 | FTM_CLKIN1 | | LPTMR0_ALT1 | | |
| 74 | L12 | J11 | 52 | RESET_b | RESET_b | RESET_b | | | | | | | | |
| 75 | K12 | — | — | PTA24 | DISABLED | | PTA24 | | | MII0_TXD2 | | FB_A29 | | |
| 76 | J12 | — | — | PTA25 | DISABLED | | PTA25 | | | MII0_TXCLK | | FB_A28 | | |
| 77 | J11 | — | — | PTA26 | DISABLED | | PTA26 | | | MII0_TXD3 | | FB_A27 | | |
| 78 | J10 | — | — | PTA27 | DISABLED | | PTA27 | | | MII0_CRS | | FB_A26 | | |
| 79 | H12 | — | — | PTA28 | DISABLED | | PTA28 | | | MII0_TXER | | FB_A25 | | |
| 80 | H11 | H11 | — | PTA29 | DISABLED | | PTA29 | | | MII0_COL | | FB_A24 | | |
| 81 | H10 | G11 | 53 | PTB0/ LLWU_P5 | ADC0_SE8/ ADC1_SE8 | ADC0_SE8/ ADC1_SE8 | PTB0/ LLWU_P5 | I2C0_SCL | FTM1_CH0 | RMII0_MDIO/ MII0_MDIO | | FTM1_QD_PHA | | |
| 82 | H9 | G10 | 54 | PTB1 | ADC0_SE9/ ADC1_SE9 | ADC0_SE9/ ADC1_SE9 | PTB1 | I2C0_SDA | FTM1_CH1 | RMII0_MDC/ MII0_MDC | | FTM1_QD_PHB | | |
| 83 | G12 | G9 | 55 | PTB2 | ADC0_SE12 | ADC0_SE12 | PTB2 | I2C0_SCL | UART0_RTS_b | ENET0_1588_TMR0 | | FTM0_FLT3 | | |
| 84 | G11 | G8 | 56 | PTB3 | ADC0_SE13 | ADC0_SE13 | PTB3 | I2C0_SDA | UART0_CTS_b/ UART0_COL_b | ENET0_1588_TMR1 | | FTM0_FLT0 | | |

| 144 LQFP | 144 MAP BGA | 121 XFBGA | 100 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 85 | G10 | — | — | PTB4 | ADC1_SE10 | ADC1_SE10 | PTB4 | | | ENET0_ 1588_TMR2 | | FTM1_FLT0 | | |
| 86 | G9 | — | — | PTB5 | ADC1_SE11 | ADC1_SE11 | PTB5 | | | ENET0_ 1588_TMR3 | | FTM2_FLT0 | | |
| 87 | F12 | F11 | — | PTB6 | ADC1_SE12 | ADC1_SE12 | PTB6 | | | | FB_AD23 | | | |
| 88 | F11 | E11 | — | PTB7 | ADC1_SE13 | ADC1_SE13 | PTB7 | | | | FB_AD22 | | | |
| 89 | F10 | D11 | — | PTB8 | DISABLED | | PTB8 | | UART3_ RTS_b | | FB_AD21 | | | |
| 90 | F9 | E10 | 57 | PTB9 | DISABLED | | PTB9 | SPI1_PCS1 | UART3_ CTS_b | | FB_AD20 | | | |
| 91 | E12 | D10 | 58 | PTB10 | ADC1_SE14 | ADC1_SE14 | PTB10 | SPI1_PCS0 | UART3_RX | | FB_AD19 | FTM0_FLT1 | | |
| 92 | E11 | C10 | 59 | PTB11 | ADC1_SE15 | ADC1_SE15 | PTB11 | SPI1_SCK | UART3_TX | | FB_AD18 | FTM0_FLT2 | | |
| 93 | H7 | — | 60 | VSS | VSS | VSS | | | | | | | | |
| 94 | F5 | — | 61 | VDD | VDD | VDD | | | | | | | | |
| 95 | E10 | B10 | 62 | PTB16 | DISABLED | | PTB16 | SPI1_SOUT | UART0_RX | FTM_ CLKIN0 | FB_AD17 | EWM_IN | | |
| 96 | E9 | E9 | 63 | PTB17 | DISABLED | | PTB17 | SPI1_SIN | UART0_TX | FTM_ CLKIN1 | FB_AD16 | EWM_OUT_ b | | |
| 97 | D12 | D9 | 64 | PTB18 | DISABLED | | PTB18 | CAN0_TX | FTM2_CH0 | I2S0_TX_ BCLK | FB_AD15 | FTM2_QD_ PHA | | |
| 98 | D11 | C9 | 65 | PTB19 | DISABLED | | PTB19 | CAN0_RX | FTM2_CH1 | I2S0_TX_FS | FB_OE_b | FTM2_QD_ PHB | | |
| 99 | D10 | F10 | 66 | PTB20 | DISABLED | | PTB20 | SPI2_PCS0 | | | FB_AD31 | CMP0_OUT | | |
| 100 | D9 | F9 | 67 | PTB21 | DISABLED | | PTB21 | SPI2_SCK | | | FB_AD30 | CMP1_OUT | | |
| 101 | C12 | F8 | 68 | PTB22 | DISABLED | | PTB22 | SPI2_SOUT | | | FB_AD29 | CMP2_OUT | | |
| 102 | C11 | E8 | 69 | PTB23 | DISABLED | | PTB23 | SPI2_SIN | SPI0_PCS5 | | FB_AD28 | | | |
| 103 | B12 | B9 | 70 | PTC0 | ADC0_SE14 | ADC0_SE14 | PTC0 | SPI0_PCS4 | PDB0_ EXTRG | USB_SOF_ OUT | FB_AD14 | I2S0_TXD1 | | |
| 104 | B11 | D8 | 71 | PTC1/ LLWU_P6 | ADC0_SE15 | ADC0_SE15 | PTC1/ LLWU_P6 | SPI0_PCS3 | UART1_ RTS_b | FTM0_CH0 | FB_AD13 | I2S0_TXD0 | | |
| 105 | A12 | C8 | 72 | PTC2 | ADC0_SE4b/ CMP1_IN0 | ADC0_SE4b/ CMP1_IN0 | PTC2 | SPI0_PCS2 | UART1_ CTS_b | FTM0_CH1 | FB_AD12 | I2S0_TX_FS | | |
| 106 | A11 | B8 | 73 | PTC3/ LLWU_P7 | CMP1_IN1 | CMP1_IN1 | PTC3/ LLWU_P7 | SPI0_PCS1 | UART1_RX | FTM0_CH2 | CLKOUT | I2S0_TX_ BCLK | | |
| 107 | H8 | — | 74 | VSS | VSS | VSS | | | | | | | | |
| 108 | — | — | 75 | VDD | VDD | VDD | | | | | | | | |
| 109 | A9 | A8 | 76 | PTC4/ LLWU_P8 | DISABLED | | PTC4/ LLWU_P8 | SPI0_PCS0 | UART1_TX | FTM0_CH3 | FB_AD11 | CMP1_OUT | | |
| 110 | D8 | D7 | 77 | PTC5/ LLWU_P9 | DISABLED | | PTC5/ LLWU_P9 | SPI0_SCK | LPTMR0_ ALT2 | I2S0_RXD0 | FB_AD10 | CMP0_OUT | FTM0_CH2 | |
| 111 | C8 | C7 | 78 | PTC6/ LLWU_P10 | CMP0_IN0 | CMP0_IN0 | PTC6/ LLWU_P10 | SPI0_SOUT | PDB0_ EXTRG | I2S0_RX_ BCLK | FB_AD9 | I2S0_MCLK | | |
| 112 | B8 | B7 | 79 | PTC7 | CMP0_IN1 | CMP0_IN1 | PTC7 | SPI0_SIN | USB_SOF_ OUT | I2S0_RX_FS | FB_AD8 | | | |

| 144 LQFP | 144 MAP BGA | 121 XFBGA | 100 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 113 | A8 | A7 | 80 | PTC8 | ADC1_SE4b/ CMP0_IN2 | ADC1_SE4b/ CMP0_IN2 | PTC8 | | FTM3_CH4 | I2S0_MCLK | FB_AD7 | | | |
| 114 | D7 | D6 | 81 | PTC9 | ADC1_SE5b/ CMP0_IN3 | ADC1_SE5b/ CMP0_IN3 | PTC9 | | FTM3_CH5 | I2S0_RX_ BCLK | FB_AD6 | FTM2_FLT0 | | |
| 115 | C7 | C6 | 82 | PTC10 | ADC1_SE6b | ADC1_SE6b | PTC10 | I2C1_SCL | FTM3_CH6 | I2S0_RX_FS | FB_AD5 | | | |
| 116 | B7 | C5 | 83 | PTC11/ LLWU_P11 | ADC1_SE7b | ADC1_SE7b | PTC11/ LLWU_P11 | I2C1_SDA | FTM3_CH7 | I2S0_RXD1 | FB_RW_b | | | |
| 117 | A7 | B6 | 84 | PTC12 | DISABLED | | PTC12 | | UART4_ RTS_b | | FB_AD27 | FTM3_FLT0 | | |
| 118 | D6 | A6 | 85 | PTC13 | DISABLED | | PTC13 | | UART4_ CTS_b | | FB_AD26 | | | |
| 119 | C6 | A5 | 86 | PTC14 | DISABLED | | PTC14 | | UART4_RX | | FB_AD25 | | | |
| 120 | B6 | B5 | 87 | PTC15 | DISABLED | | PTC15 | | UART4_TX | | FB_AD24 | | | |
| 121 | — | — | 88 | VSS | VSS | VSS | | | | | | | | |
| 122 | — | — | 89 | VDD | VDD | VDD | | | | | | | | |
| 123 | A6 | D5 | 90 | PTC16 | DISABLED | | PTC16 | | UART3_RX | ENET0_ 1588_TMR0 | FB_CS5_b/ FB_TSIZ1/ FB_BE23_ 16_BLS15_ 8_b | | | |
| 124 | D5 | C4 | 91 | PTC17 | DISABLED | | PTC17 | | UART3_TX | ENET0_ 1588_TMR1 | FB_CS4_b/ FB_TSIZ0/ FB_BE31_ 24_BLS7_0_ b | | | |
| 125 | C5 | B4 | 92 | PTC18 | DISABLED | | PTC18 | | UART3_ RTS_b | ENET0_ 1588_TMR2 | FB_TBST_b/ FB_CS2_b/ FB_BE15_8_ BLS23_16_b | | | |
| 126 | B5 | A4 | — | PTC19 | DISABLED | | PTC19 | | UART3_ CTS_b | ENET0_ 1588_TMR3 | FB_CS3_b/ FB_BE7_0_ BLS31_24_b | FB_TA_b | | |
| 127 | A5 | D4 | 93 | PTD0/ LLWU_P12 | DISABLED | | PTD0/ LLWU_P12 | SPI0_PCS0 | UART2_ RTS_b | FTM3_CH0 | FB_ALE/ FB_CS1_b/ FB_TS_b | | | |
| 128 | D4 | D3 | 94 | PTD1 | ADC0_SE5b | ADC0_SE5b | PTD1 | SPI0_SCK | UART2_ CTS_b | FTM3_CH1 | FB_CS0_b | | | |
| 129 | C4 | C3 | 95 | PTD2/ LLWU_P13 | DISABLED | | PTD2/ LLWU_P13 | SPI0_SOUT | UART2_RX | FTM3_CH2 | FB_AD4 | | I2C0_SCL | |
| 130 | B4 | B3 | 96 | PTD3 | DISABLED | | PTD3 | SPI0_SIN | UART2_TX | FTM3_CH3 | FB_AD3 | | I2C0_SDA | |
| 131 | A4 | A3 | 97 | PTD4/ LLWU_P14 | DISABLED | | PTD4/ LLWU_P14 | SPI0_PCS1 | UART0_ RTS_b | FTM0_CH4 | FB_AD2 | EWM_IN | SPI1_PCS0 | |
| 132 | A3 | A2 | 98 | PTD5 | ADC0_SE6b | ADC0_SE6b | PTD5 | SPI0_PCS2 | UART0_ CTS_b/ UART0_ COL_b | FTM0_CH5 | FB_AD1 | EWM_OUT_ b | SPI1_SCK | |
| 133 | A2 | B2 | 99 | PTD6/ LLWU_P15 | ADC0_SE7b | ADC0_SE7b | PTD6/ LLWU_P15 | SPI0_PCS3 | UART0_RX | FTM0_CH6 | FB_AD0 | FTM0_FLT0 | SPI1_SOUT | |

| 144 LQFP | 144 MAP BGA | 121 XFBGA | 100 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 134 | M10 | — | — | VSS | VSS | VSS | | | | | | | | |
| 135 | F8 | — | — | VDD | VDD | VDD | | | | | | | | |
| 136 | A1 | A1 | 100 | PTD7 | DISABLED | | PTD7 | CMT_IRO | UART0_TX | FTM0_CH7 | | FTM0_FLT1 | SPI1_SIN | |
| 137 | C9 | A10 | — | PTD8 | DISABLED | | PTD8 | I2C0_SCL | UART5_RX | | | FB_A16 | | |
| 138 | B9 | A9 | — | PTD9 | DISABLED | | PTD9 | I2C0_SDA | UART5_TX | | | FB_A17 | | |
| 139 | B3 | B1 | — | PTD10 | DISABLED | | PTD10 | | UART5_ RTS_b | | | FB_A18 | | |
| 140 | B2 | C2 | — | PTD11 | DISABLED | | PTD11 | SPI2_PCS0 | UART5_ CTS_b | SDHC0_ CLKIN | | FB_A19 | | |
| 141 | B1 | C1 | — | PTD12 | DISABLED | | PTD12 | SPI2_SCK | FTM3_FLT0 | SDHC0_D4 | | FB_A20 | | |
| 142 | C3 | D2 | — | PTD13 | DISABLED | | PTD13 | SPI2_SOUT | | SDHC0_D5 | | FB_A21 | | |
| 143 | C2 | D1 | — | PTD14 | DISABLED | | PTD14 | SPI2_SIN | | SDHC0_D6 | | FB_A22 | | |
| 144 | C1 | E1 | — | PTD15 | DISABLED | | PTD15 | SPI2_PCS1 | | SDHC0_D7 | | FB_A23 | | |

## 10.3.2 K64 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.