11.2.5 Signal multiplexing constraints

1. A given peripheral function must be assigned to a maximum of one package pin. Do not program the same function to more than one pin.
2. To ensure the best signal timing for a given peripheral's interface, choose the pins in closest proximity to each other.

11.3 Pinout

11.3.1 K66 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
—	L5	RTC_ WAKEUP_B	RTC_ WAKEUP_B	RTC_ WAKEUP_B								
—	M5	NC	NC	NC								
—	A10	NC	NC	NC								
—	B10	NC	NC	NC								
—	C10	NC	NC	NC								
1	D3	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1	TRACE_ CLKOUT	I2C1_SDA	RTC_ CLKOUT	
2	D2	PTE1/ LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX	SDHC0_D0	TRACE_D3	I2C1_SCL	SPI1_SIN	
3	D1	PTE2/ LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_ CTS_b	SDHC0_ DCLK	TRACE_D2			
4	E4	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_ RTS_b	SDHC0_CMD	TRACE_D1		SPI1_SOUT	
5	E5	VDD	VDD	VDD								
6	H3	VSS	VSS	VSS								
7	E3	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX	SDHC0_D3	TRACE_D0			
8	E2	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2		FTM3_CH0		
9	E1	PTE6/ LLWU_P16	DISABLED		PTE6/ LLWU_P16	SPI1_PCS3	UART3_ CTS_b	I2S0_MCLK		FTM3_CH1	USB0_SOF_ OUT	
10	F4	PTE7	DISABLED		PTE7		UART3_ RTS_b	I2S0_RXD0		FTM3_CH2		
11	F3	PTE8	DISABLED		PTE8	I2S0_RXD1		I2S0_RX_FS	LPUART0_ TX	FTM3_CH3		
12	F2	PTE9/ LLWU_P17	DISABLED		PTE9/ LLWU_P17	I2S0_TXD1		I2S0_RX_ BCLK	LPUART0_ RX	FTM3_CH4		

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
13	F1	PTE10/ LLWU_P18	DISABLED		PTE10/ LLWU_P18	I2C3_SDA		I2S0_TXD0	LPUART0_ CTS_b	FTM3_CH5	USB1_ID	
14	G4	PTE11	DISABLED		PTE11	I2C3_SCL		I2S0_TX_FS	LPUART0_ RTS_b	FTM3_CH6		
15	G3	PTE12	DISABLED		PTE12			I2S0_TX_ BCLK		FTM3_CH7		
16	E6	VDD	VDD	VDD								
17	F7	VSS	VSS	VSS								
18	F6	VSS	VSS	VSS								
19	H1	USB0_DP	USB0_DP	USB0_DP								
20	H2	USB0_DM	USB0_DM	USB0_DM								
21	G1	VREG_OUT	VREG_OUT	VREG_OUT								
22	G2	VREG_IN0	VREG_IN0	VREG_IN0								
23	J2	VREG_IN1	DISABLED	VREG_IN1								
24	K2	USB1_VSS	DISABLED	USB1_VSS								
25	J1	USB1_DP	DISABLED	USB1_DP								
26	K1	USB1_DM	DISABLED	USB1_DM								
27	L1	USB1_VBUS	DISABLED	USB1_VBUS								
28	L2	ADC0_DM0/ ADC1_DM3	ADC0_DM0/ ADC1_DM3	ADC0_DM0/ ADC1_DM3								
29	M1	ADC1_DP0/ ADC0_DP3	ADC1_DP0/ ADC0_DP3	ADC1_DP0/ ADC0_DP3								
30	M2	ADC1_DM0/ ADC0_DM3	ADC1_DM0/ ADC0_DM3	ADC1_DM0/ ADC0_DM3								
31	H5	VDDA	VDDA	VDDA								
32	G5	VREFH	VREFH	VREFH								
33	G6	VREFL	VREFL	VREFL								
34	H6	VSSA	VSSA	VSSA								
35	K3	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	ADC1_SE16/ CMP2_IN2/ ADC0_SE22								
36	J3	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21								
37	M3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
38	L3	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
39	L4	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23								
40	M7	XTAL32	XTAL32	XTAL32								

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
41	M6	EXTAL32	EXTAL32	EXTAL32								
42	L6	VBAT	VBAT	VBAT								
43	—	VDD	VDD	VDD								
44	—	VSS	VSS	VSS								
45	M4	PTE24	ADC0_SE17	ADC0_SE17	PTE24	CAN1_TX	UART4_TX		I2C0_SCL	EWM_OUT_b		
46	K5	PTE25/ LLWU_P21	ADC0_SE18	ADC0_SE18	PTE25/ LLWU_P21	CAN1_RX	UART4_RX		I2C0_SDA	EWM_IN		
47	K4	PTE26	DISABLED		PTE26	ENET_1588_ CLKIN	UART4_ CTS_b			RTC_ CLKOUT	USB0_CLKIN	
48	J4	PTE27	DISABLED		PTE27		UART4_ RTS_b					
49	H4	PTE28	DISABLED		PTE28							
50	J5	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_ CTS_b/ UART0_ COL_b	FTM0_CH5		LPUART0_ CTS_b		JTAG_TCLK/ SWD_CLK	EZP_CLK
51	J6	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6	I2C3_SDA	LPUART0_ RX		JTAG_TDI	EZP_DI
52	K6	PTA2	JTAG_TDO/ TRACE_ SWO/ EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7	I2C3_SCL	LPUART0_ TX		JTAG_TDO/ TRACE_ SWO	EZP_DO
53	K7	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UART0_ RTS_b	FTM0_CH0		LPUART0_ RTS_b		JTAG_TMS/ SWD_DIO	
54	L7	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
55	M8	PTA5	DISABLED		PTA5	USB0_CLKIN	FTM0_CH2	RMII0_RXER/ MII0_RXER	CMP2_OUT	I2S0_TX_ BCLK	JTAG_TRST_ b	
56	E7	VDD	VDD	VDD								
57	G7	VSS	VSS	VSS								
58	J7	PTA6	DISABLED		PTA6		FTM0_CH3		CLKOUT		TRACE_ CLKOUT	
59	J8	PTA7	ADC0_SE10	ADC0_SE10	PTA7		FTM0_CH4		RMII0_MDIO/ MII0_MDIO		TRACE_D3	
60	K8	PTA8	ADC0_SE11	ADC0_SE11	PTA8		FTM1_CH0		RMII0_MDC/ MII0_MDC	FTM1_QD_ PHA/ TPM1_CH0	TRACE_D2	
61	L8	PTA9	DISABLED		PTA9		FTM1_CH1	MII0_RXD3		FTM1_QD_ PHB/ TPM1_CH1	TRACE_D1	
62	M9	PTA10/ LLWU_P22	DISABLED		PTA10/ LLWU_P22		FTM2_CH0	MII0_RXD2		FTM2_QD_ PHA/ TPM2_CH0	TRACE_D0	
63	L9	PTA11/ LLWU_P23	DISABLED		PTA11/ LLWU_P23		FTM2_CH1	MII0_RXCLK	I2C2_SDA	FTM2_QD_ PHB/ TPM2_CH1		

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
64	K9	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0	RMII0_RXD1/ MII0_RXD1	I2C2_SCL	I2S0_TXD0	FTM1_QD_ PHA/ TPM1_CH0	
65	J9	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1	RMII0_RXD0/ MII0_RXD0	I2C2_SDA	I2S0_TX_FS	FTM1_QD_ PHB/ TPM1_CH1	
66	L10	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX	RMII0_CRS_ DV/ MII0_RXDV	I2C2_SCL	I2S0_RX_ BCLK	I2S0_TXD1	
67	L11	PTA15	CMP3_IN1	CMP3_IN1	PTA15	SPI0_SCK	UART0_RX	RMII0_TXEN/ MII0_TXEN		I2S0_RXD0		
68	K10	PTA16	CMP3_IN2	CMP3_IN2	PTA16	SPI0_SOUT	UART0_ CTS_b/ UART0_ COL_b	RMII0_TXD0/ MII0_TXD0		I2S0_RX_FS	I2S0_RXD1	
69	K11	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_ RTS_b	RMII0_TXD1/ MII0_TXD1		I2S0_MCLK		
70	E8	VDD	VDD	VDD								
71	G8	VSS	VSS	VSS								
72	M12	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0			TPM_CLKIN0	
73	M11	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ ALT1	TPM_CLKIN1	
74	L12	RESET_b	RESET_b	RESET_b								
75	K12	PTA24	CMP3_IN4	CMP3_IN4	PTA24			MII0_TXD2		FB_A29		
76	J12	PTA25	CMP3_IN5	CMP3_IN5	PTA25			MII0_TXCLK		FB_A28		
77	J11	PTA26	DISABLED		PTA26			MII0_TXD3		FB_A27		
78	J10	PTA27	DISABLED		PTA27			MII0_CRS		FB_A26		
79	H12	PTA28	DISABLED		PTA28			MII0_TXER		FB_A25		
80	H11	PTA29	DISABLED		PTA29			MII0_COL		FB_A24		
81	H10	PTB0/ LLWU_P5	ADC0_SE8/ ADC1_SE8/ TSI0_CH0	ADC0_SE8/ ADC1_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0	RMII0_MDIO/ MII0_MDIO	SDRAM_ CAS_b	FTM1_QD_ PHA/ TPM1_CH0		
82	H9	PTB1	ADC0_SE9/ ADC1_SE9/ TSI0_CH6	ADC0_SE9/ ADC1_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1	RMII0_MDC/ MII0_MDC	SDRAM_ RAS_b	FTM1_QD_ PHB/ TPM1_CH1		
83	G12	PTB2	ADC0_SE12/ TSI0_CH7	ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	UART0_ RTS_b	ENET0_ 1588_TMR0	SDRAM_WE	FTM0_FLT3		
84	G11	PTB3	ADC0_SE13/ TSI0_CH8	ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	UART0_ CTS_b/ UART0_ COL_b	ENET0_ 1588_TMR1	SDRAM_ CS0_b	FTM0_FLT0		
85	G10	PTB4	ADC1_SE10	ADC1_SE10	PTB4			ENET0_ 1588_TMR2	SDRAM_ CS1_b	FTM1_FLT0		
86	G9	PTB5	ADC1_SE11	ADC1_SE11	PTB5			ENET0_ 1588_TMR3		FTM2_FLT0		
87	F12	PTB6	ADC1_SE12	ADC1_SE12	PTB6				FB_AD23/ SDRAM_D23			

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
88	F11	PTB7	ADC1_SE13	ADC1_SE13	PTB7				FB_AD22/ SDRAM_D22			
89	F10	PTB8	DISABLED		PTB8		UART3_ RTS_b		FB_AD21/ SDRAM_D21			
90	F9	PTB9	DISABLED		PTB9	SPI1_PCS1	UART3_ CTS_b		FB_AD20/ SDRAM_D20			
91	E12	PTB10	ADC1_SE14	ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX		FB_AD19/ SDRAM_D19	FTM0_FLT1		
92	E11	PTB11	ADC1_SE15	ADC1_SE15	PTB11	SPI1_SCK	UART3_TX		FB_AD18/ SDRAM_D18	FTM0_FLT2		
93	H7	VSS	VSS	VSS								
94	F5	VDD	VDD	VDD								
95	E10	PTB16	TSI0_CH9	TSI0_CH9	PTB16	SPI1_SOUT	UART0_RX	FTM_CLKIN0	FB_AD17/ SDRAM_D17	EWM_IN	TPM_CLKIN0	
96	E9	PTB17	TSI0_CH10	TSI0_CH10	PTB17	SPI1_SIN	UART0_TX	FTM_CLKIN1	FB_AD16/ SDRAM_D16	EWM_OUT_b	TPM_CLKIN1	
97	D12	PTB18	TSI0_CH11	TSI0_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_ BCLK	FB_AD15/ SDRAM_A23	FTM2_QD_ PHA/ TPM2_CH0		
98	D11	PTB19	TSI0_CH12	TSI0_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_ PHB/ TPM2_CH1		
99	D10	PTB20	DISABLED		PTB20	SPI2_PCS0			FB_AD31/ SDRAM_D31	CMP0_OUT		
100	D9	PTB21	DISABLED		PTB21	SPI2_SCK			FB_AD30/ SDRAM_D30	CMP1_OUT		
101	C12	PTB22	DISABLED		PTB22	SPI2_SOUT			FB_AD29/ SDRAM_D29	CMP2_OUT		
102	C11	PTB23	DISABLED		PTB23	SPI2_SIN	SPI0_PCS5		FB_AD28/ SDRAM_D28	CMP3_OUT		
103	B12	PTC0	ADC0_SE14/ TSI0_CH13	ADC0_SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_ EXTRG	USB0_SOF_ OUT	FB_AD14/ SDRAM_A22	I2S0_TXD1		
104	B11	PTC1/ LLWU_P6	ADC0_SE15/ TSI0_CH14	ADC0_SE15/ TSI0_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_ RTS_b	FTM0_CH0	FB_AD13/ SDRAM_A21	I2S0_TXD0		
105	A12	PTC2	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	PTC2	SPI0_PCS2	UART1_ CTS_b	FTM0_CH1	FB_AD12/ SDRAM_A20	I2S0_TX_FS		
106	A11	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_ BCLK		
107	H8	VSS	VSS	VSS								
108	—	VDD	VDD	VDD								
109	A9	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11/ SDRAM_A19	CMP1_OUT		
110	D8	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	I2S0_RXD0	FB_AD10/ SDRAM_A18	CMP0_OUT	FTM0_CH2	
111	C8	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_ EXTRG	I2S0_RX_ BCLK	FB_AD9/ SDRAM_A17	I2S0_MCLK		

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
112	B8	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB0_SOF_OUT	I2S0_RX_FS	FB_AD8/ SDRAM_A16			
113	A8	PTC8	ADC1_SE4b/ CMP0_IN2	ADC1_SE4b/ CMP0_IN2	PTC8		FTM3_CH4	I2S0_MCLK	FB_AD7/ SDRAM_A15			
114	D7	PTC9	ADC1_SE5b/ CMP0_IN3	ADC1_SE5b/ CMP0_IN3	PTC9		FTM3_CH5	I2S0_RX_BCLK	FB_AD6/ SDRAM_A14	FTM2_FLT0		
115	C7	PTC10	ADC1_SE6b	ADC1_SE6b	PTC10	I2C1_SCL	FTM3_CH6	I2S0_RX_FS	FB_AD5/ SDRAM_A13			
116	B7	PTC11/ LLWU_P11	ADC1_SE7b	ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA	FTM3_CH7	I2S0_RXD1	FB_RW_b			
117	A7	PTC12	DISABLED		PTC12		UART4_RTS_b	FTM_CLKIN0	FB_AD27/ SDRAM_D27	FTM3_FLT0	TPM_CLKIN0	
118	D6	PTC13	DISABLED		PTC13		UART4_CTS_b	FTM_CLKIN1	FB_AD26/ SDRAM_D26		TPM_CLKIN1	
119	C6	PTC14	DISABLED		PTC14		UART4_RX		FB_AD25/ SDRAM_D25			
120	B6	PTC15	DISABLED		PTC15		UART4_TX		FB_AD24/ SDRAM_D24			
121	—	VSS	VSS	VSS								
122	—	VDD	VDD	VDD								
123	A6	PTC16	DISABLED		PTC16	CAN1_RX	UART3_RX	ENET0_1588_TMR0	FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_BLS15_8_b/ SDRAM_DQM2			
124	D5	PTC17	DISABLED		PTC17	CAN1_TX	UART3_TX	ENET0_1588_TMR1	FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_BLS7_0_b/ SDRAM_DQM3			
125	C5	PTC18	DISABLED		PTC18		UART3_RTS_b	ENET0_1588_TMR2	FB_TBST_b/ FB_CS2_b/ FB_BE15_8_BLS23_16_b/ SDRAM_DQM1			
126	B5	PTC19	DISABLED		PTC19		UART3_CTS_b	ENET0_1588_TMR3	FB_CS3_b/ FB_BE7_0_BLS31_24_b/ SDRAM_DQM0	FB_TA_b		
127	A5	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_b	FTM3_CH0	FB_ALE/ FB_CS1_b/ FB_TS_b			
128	D4	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b	FTM3_CH1	FB_CS0_b			

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
129	C4	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX	FTM3_CH2	FB_AD4/ SDRAM_A12		I2C0_SCL	
130	B4	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX	FTM3_CH3	FB_AD3/ SDRAM_A11		I2C0_SDA	
131	A4	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_ RTS_b	FTM0_CH4	FB_AD2/ SDRAM_A10	EWM_IN	SPI1_PCS0	
132	A3	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_ CTS_b/ UART0_ COL_b	FTM0_CH5	FB_AD1/ SDRAM_A9	EWM_OUT_b	SPI1_SCK	
133	A2	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0	SPI1_SOUT	
134	M10	VSS	VSS	VSS								
135	F8	VDD	VDD	VDD								
136	A1	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7	SDRAM_CKE	FTM0_FLT1	SPI1_SIN	
137	C9	PTD8/ LLWU_P24	DISABLED		PTD8/ LLWU_P24	I2C0_SCL			LPUART0_ RX	FB_A16		
138	B9	PTD9	DISABLED		PTD9	I2C0_SDA			LPUART0_ TX	FB_A17		
139	B3	PTD10	DISABLED		PTD10				LPUART0_ RTS_b	FB_A18		
140	B2	PTD11/ LLWU_P25	DISABLED		PTD11/ LLWU_P25	SPI2_PCS0		SDHC0_ CLKIN	LPUART0_ CTS_b	FB_A19		
141	B1	PTD12	DISABLED		PTD12	SPI2_SCK	FTM3_FLT0	SDHC0_D4		FB_A20		
142	C3	PTD13	DISABLED		PTD13	SPI2_SOUT		SDHC0_D5		FB_A21		
143	C2	PTD14	DISABLED		PTD14	SPI2_SIN		SDHC0_D6		FB_A22		
144	C1	PTD15	DISABLED		PTD15	SPI2_PCS1		SDHC0_D7		FB_A23		

11.3.2 K66 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.