100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	1	PTE0/ CLKOUT32K	ADC1_SE4a	ADC1_SE4a	PTE0/ CLKOUT32K	SPI1_PCS1	UART1_TX			I2C1_SDA		
2	2	PTE1/ LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX			I2C1_SCL	SPI1_SIN	
3	—	PTE2/ LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_ b					
4	—	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_ b				SPI1_SOUT	
5	—	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	LPUART0_TX					
6	—	PTE5	DISABLED		PTE5	SPI1_PCS2	LPUART0_RX					
7	—	PTE6	DISABLED		PTE6	SPI1_PCS3	LPUART0_ CTS_b					
8	3	VDD	VDD	VDD								
9	4	VSS	VSS	VSS								
10	5	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
11	6	PTE17	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPTMR0_ ALT3		
12	7	PTE18	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_ b	I2C0_SDA				
13	8	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_ b	I2C0_SCL				
14	—	ADC0_DP1	ADC0_DP1	ADC0_DP1								
15	—	ADC0_DM1	ADC0_DM1	ADC0_DM1								
16	—	ADC1_DP1/ ADC0_DP2	ADC1_DP1/ ADC0_DP2	ADC1_DP1/ ADC0_DP2								
17	—	ADC1_DM1/ ADC0_DM2	ADC1_DM1/ ADC0_DM2	ADC1_DM1/ ADC0_DM2								
18	9	ADC0_DP0/ ADC1_DP3	ADC0_DP0/ ADC1_DP3	ADC0_DP0/ ADC1_DP3								
19	10	ADC0_DM0/ ADC1_DM3	ADC0_DM0/ ADC1_DM3	ADC0_DM0/ ADC1_DM3								
20	11	ADC1_DP0/ ADC0_DP3	ADC1_DP0/ ADC0_DP3	ADC1_DP0/ ADC0_DP3								
21	12	ADC1_DM0/ ADC0_DM3	ADC1_DM0/ ADC0_DM3	ADC1_DM0/ ADC0_DM3								
22	13	VDDA	VDDA	VDDA								
23	14	VREFH	VREFH	VREFH								
24	15	VREFL	VREFL	VREFL								
25	16	VSSA	VSSA	VSSA								
26	17	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
27	18	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
28	19	CMP0_IN4/ ADC1_SE23	CMP0_IN4/ ADC1_SE23	CMP0_IN4/ ADC1_SE23								
29	—	VSS	VSS	VSS								
30	—	VDD	VDD	VDD								
31	20	PTE24	ADC0_SE17	ADC0_SE17	PTE24		FTM0_CH0		I2C0_SCL	EWM_OUT_b		
32	21	PTE25	ADC0_SE18	ADC0_SE18	PTE25		FTM0_CH1		I2C0_SDA	EWM_IN		
33	—	PTE26/ CLKOUT32K	DISABLED		PTE26/ CLKOUT32K							
34	22	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK		PTA0	UART0_CTS_ b	FTM0_CH5		EWM_IN		JTAG_TCLK/ SWD_CLK	EZP_CLK
35	23	PTA1	JTAG_TDI/ EZP_DI		PTA1	UART0_RX	FTM0_CH6	CMP0_OUT	FTM2_QD_ PHA	FTM1_CH1	JTAG_TDI	EZP_DI
36	24	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO		PTA2	UART0_TX	FTM0_CH7	CMP1_OUT	FTM2_QD_ PHB	FTM1_CH0	JTAG_TDO/ TRACE_SWO	EZP_DO
37	25	PTA3	JTAG_TMS/ SWD_DIO		PTA3	UART0_RTS_ b	FTM0_CH0	FTM2_FLT0	EWM_OUT_b		JTAG_TMS/ SWD_DIO	
38	26	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b		PTA4/ LLWU_P3		FTM0_CH1		FTM0_FLT3		NMI_b	EZP_CS_b
39	27	PTA5	DISABLED		PTA5		FTM0_CH2				JTAG_TRST_ b	
40	—	VDD	VDD	VDD								
41	—	VSS	VSS	VSS								
42	28	PTA12	DISABLED		PTA12		FTM1_CH0				FTM1_QD_ PHA	
43	29	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4		FTM1_CH1				FTM1_QD_ PHB	
44	—	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX					
45	—	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX					
46	—	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_ b					
47	—	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_ b					
48	30	VDD	VDD	VDD								
49	31	VSS	VSS	VSS								
50	32	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
51	33	PTA19	XTAL0	XTAL0	PTA19	FTM0_FLT0	FTM1_FLT0	FTM_CLKIN1		LPTMR0_ ALT1		
52	34	RESET_b	RESET_b	RESET_b								
53	35	PTB0/ LLWU_P5	ADC0_SE8/ ADC1_SE8	ADC0_SE8/ ADC1_SE8	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA	UART0_RX	
54	36	PTB1	ADC0_SE9/ ADC1_SE9	ADC0_SE9/ ADC1_SE9	PTB1	I2C0_SDA	FTM1_CH1	FTM0_FLT2	EWM_IN	FTM1_QD_ PHB	UART0_TX	
55	37	PTB2	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	UART0_RTS_ b	FTM0_FLT1		FTM0_FLT3		

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
56	38	PTB3	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	UART0_CTS_b			FTM0_FLT0		
57	—	PTB9	DISABLED		PTB9	SPI1_PCS1	LPUART0_CTS_b					
58	—	PTB10	ADC1_SE14	ADC1_SE14	PTB10	SPI1_PCS0	LPUART0_RX			FTM0_FLT1		
59	—	PTB11	ADC1_SE15	ADC1_SE15	PTB11	SPI1_SCK	LPUART0_TX			FTM0_FLT2		
60	—	VSS	VSS	VSS								
61	—	VDD	VDD	VDD								
62	39	PTB16	DISABLED		PTB16	SPI1_SOUT	UART0_RX	FTM_CLKIN0		EWM_IN		
63	40	PTB17	DISABLED		PTB17	SPI1_SIN	UART0_TX	FTM_CLKIN1		EWM_OUT_b		
64	41	PTB18	DISABLED		PTB18		FTM2_CH0			FTM2_QD_PHA		
65	42	PTB19	DISABLED		PTB19		FTM2_CH1			FTM2_QD_PHB		
66	—	PTB20	DISABLED		PTB20					CMP0_OUT		
67	—	PTB21	DISABLED		PTB21					CMP1_OUT		
68	—	PTB22	DISABLED		PTB22							
69	—	PTB23	DISABLED		PTB23		SPI0_PCS5					
70	43	PTC0	ADC0_SE14	ADC0_SE14	PTC0	SPI0_PCS4	PDB0_EXTRG			FTM0_FLT1	SPI0_PCS0	
71	44	PTC1/LLWU_P6	ADC0_SE15	ADC0_SE15	PTC1/LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0			LPUART0_RTS_b	
72	45	PTC2	ADC0_SE4b/CMP1_IN0	ADC0_SE4b/CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1			LPUART0_CTS_b	
73	46	PTC3/LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT		LPUART0_RX	
74	47	VSS	VSS	VSS								
75	48	VDD	VDD	VDD								
76	49	PTC4/LLWU_P8	DISABLED		PTC4/LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	LPUART0_TX	
77	50	PTC5/LLWU_P9	DISABLED		PTC5/LLWU_P9	SPI0_SCK	LPTMR0_ALT2			CMP0_OUT	FTM0_CH2	
78	51	PTC6/LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/LLWU_P10	SPI0_SOUT	PDB0_EXTRG				I2C0_SCL	
79	52	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN					I2C0_SDA	
80	53	PTC8	ADC1_SE4b/CMP0_IN2	ADC1_SE4b/CMP0_IN2	PTC8							
81	54	PTC9	ADC1_SE5b/CMP0_IN3	ADC1_SE5b/CMP0_IN3	PTC9					FTM2_FLT0		
82	55	PTC10	ADC1_SE6b	ADC1_SE6b	PTC10	I2C1_SCL						
83	56	PTC11/LLWU_P11	ADC1_SE7b	ADC1_SE7b	PTC11/LLWU_P11	I2C1_SDA						
84	—	PTC12	DISABLED		PTC12							
85	—	PTC13	DISABLED		PTC13							
86	—	PTC14	DISABLED		PTC14							
87	—	PTC15	DISABLED		PTC15							

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
88	—	VSS	VSS	VSS								
89	—	VDD	VDD	VDD								
90	—	PTC16	DISABLED		PTC16		LPUART0_RX					
91	—	PTC17	DISABLED		PTC17		LPUART0_TX					
92	—	PTC18	DISABLED		PTC18		LPUART0_ RTS_b					
93	57	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_ b	FTM0_CH0		LPUART0_ RTS_b		
94	58	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_ b	FTM0_CH1		LPUART0_ CTS_b		
95	59	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX	FTM0_CH2		LPUART0_RX	I2C0_SCL	
96	60	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX	FTM0_CH3		LPUART0_TX	I2C0_SDA	
97	61	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_ b	FTM0_CH4		EWM_IN	SPI1_PCS0	
98	62	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_ b	FTM0_CH5		EWM_OUT_b	SPI1_SCK	
99	63	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6		FTM0_FLT0	SPI1_SOUT	
100	64	PTD7	DISABLED		PTD7		UART0_TX	FTM0_CH7		FTM0_FLT1	SPI1_SIN	

10.3.2 KV31F Pinouts

The following figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.