UNIVERSITY OF DUBLIN

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TRINITY COLLEGE

FACULTY OF ENGINEERING, MATHEMATICS AND SCIENCE

SCHOOL OF COMPUTER SCIENCE AND STATISTICS

B.A. (Mod) Computer Science
Junior Freshman Examination

Trinity Term 2009

1BA4 Digital Logic Design

Saturday 23rd May, 2009 **Regent House** 14:00–17:00

Dr.B.A.Coghlan

Attempt FOUR questions

Materials:
Log tables are available from the invigilators, if required.

Non-programmable calculators are permitted for this examination—please indicate the make and model of your calculator on each answer book used.

1.

(a) Using only Huntington's Postulates and theorems, **algebraically** prove that:

$$AB + A'C + BC = AB + A'C$$ [9 marks]

(b) List all 16 possible Boolean functions of 2 variables, giving their conventional name in each case. [8 marks]

(c) Explain the differences between canonical, standard and non-standard forms of a Boolean equation. [8 marks]

2. Use Karnaugh Maps to minimize the logic for a 1bit combinatorial logic block that has a two outputs, Y and Z, three inputs D, D_L and D_R, and performs the Boolean functions shown in Table 1, depending upon mode inputs M_{2-0}.

D_R is intended to connect to the next **least** significant bit's Y output, so that it functions as the carry and borrow input for increment and decrement respectively, and as a shift-left input when shifting left. Similarly, D_L is intended to connect to the next most significant bit's Y output, so that it functions as a shift-right input when shifting right.

Draw a circuit diagram showing the interconnections between 3 such blocks. [25 marks]

3. Use **J-K flip-flops** to design the logic for a synchronous up/down counter that counts "up" through the sequence 1 2 6 3 5 7 if the input switch UP is 1, and "down" through the sequence 7 2 1 5 3 6 if UP is 0. Verify that the counter is self-starting. [25 marks]

4. A hotel suite light controller has three switches $S1$, $S2$ and $S3$ distributed around the suite. Whenever one of the switches is pressed the light switches ON if they are OFF, or vice versa. There is also a "freeze" switch F to prevent the lights from changing state, and a 1Hz clock input.

(a) Draw the state diagram

(b) Design a minimum-logic light controller using D flip-flops

[25 marks]

5. Assume N is a 2bit unsigned integer count input, and Y is a 3bit unsigned integer output. Assume that apart from basic logic you also have a supply of 2-bit full adder/subtractors and 2:1 multiplexers. Completely design an algorithmic state machine to perform the following algorithm:

```
        R0 := N;  R1 := 0              ; input N and initialise result
Loop:   R1 := R1 + R0;  R0 := R0 - 1   ; accumulate result and decrement count
        If (R0 <> 0) GoTo Loop         ; loop until R0=0
        Y := R1                        ; output the result
```

[25 marks]

6. Using implication tables and merger diagrams, minimize the flow table shown in Table 2. [25 marks]

M_2	M_1	M_0	$Youtput$	$Zoutput$	**function**
0	0	0	X	0	reset
0	0	1	X	1	set
0	1	0	D	D_R	shift left
0	1	1	D	D_L	shift right
1	0	0	carry	(D + 1)	increment
1	0	1	borrow	(D - 1)	decrement
1	1	0	X	D'	complement
1	1	1	X	D	load

Table 1: Truth table for Question 2

	00	**01**	**11**	**10**
a	a,0	d,X	a,0	c,X
b	a,X	b,0	b,1	d,X
c	d,X	c,1	b,X	c,0
d	d,1	d,1	e,X	d,1
e	f,X	e,0	e,1	c,X
f	f,1	b,X	a,X	f,0
g	f,X	g,0	g,1	i,X
h	d,X	h,1	b,X	i,X
i	d,X	i,1	b,X	i,0

Table 2: Primitive flow table for Question 6