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Computer Architecture

EE/CE 4304

Spring 2025 Project v1.0

VERSION Patrick Sigler

Instructions

This is your personalized project.

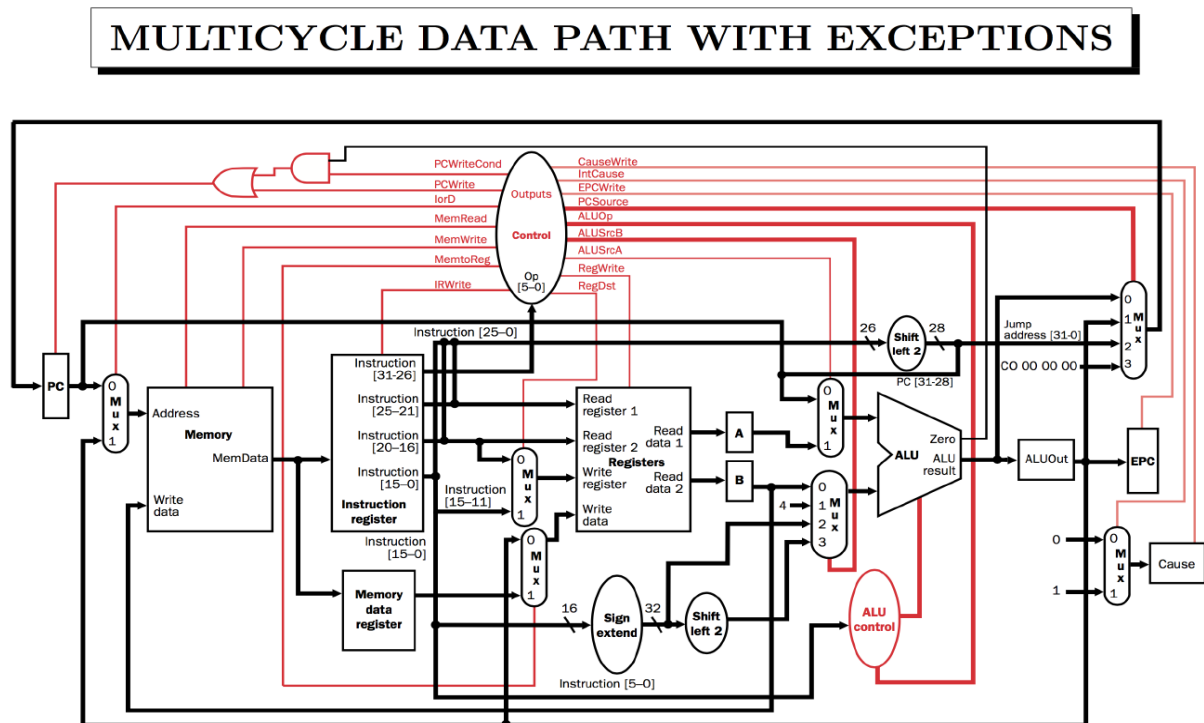
Consultation with any person (other than the TAs or Professor) at any location constitutes cheating. However, you are free to visit the Web and explore solutions to your design problem. In fact, ASIC World at <http://asicworld.com> and similar sites are encouraged.

If cheating is detected, the incident will be dealt with according to established UT-Dallas procedures. Possible disciplinary actions for academic dishonesty include a failing grade on this project.

Problem Statement—Version pts200000

In this project, you are to design your own Instruction Set Architecture (ISA) and a multi-cycle computer (or other advance topologies) which implements it. You will be given specifications for your computer which make it unique from other students in this class. You will need to implement an architecture. You may implement either multi-cycle, pipelined, or Out-of-Order architectures. An example of the multicycle architecture is shown in Figure 1 below. In order to make the project less daunting, the project will have two phases: 1) ISA design and specification and 2) implementation and simulation using Verilog.

Figure 1: Multi Cycle Computer Architecture



After David A. Patterson and John L. Hennessy, *Computer Organization and Design*, 2nd Edition

Specifications for pts200000

Your computer specification follows:

Marketing has determined that your computer is targeted as a Embedded Systems computer and so you memory address space should be implemented using a Harvard architecture.

Your address bus has a width of 13 bits which means that your computer must support 8192 addresses. This address space is shared between the instructions and your computer's program data space. The OS architect has already determined that the entry point of programs will be at the center of the address space or 0x1000. All programs will be loaded at that address and any branches should be relative to that starting address.

Your computer will have a data width of 24 bits. Your register files will be addressed using 4 bits resulting in a register file which is 16 by 24. This computer should use Little Endian to access memory and perform calculations.

You are to design your own instruction set architecture with an instruction that is 34 bits wide. Your instruction should accommodate an immediate field which has 16 bits. You should have 6 bits devoted to instruction types which means your computer can support 64 instructions.

Your computer will need to support two simple programs:

$$C \leftarrow A + B$$

and

```
int sum = 0 ;
for( i = 0 ; i <= 10 ; i++ ){
    sum += i ;
}
```

Phase 1 - Instruction Set Design

You will need to design and specify your instruction set, that is, you will need to determine your command set. How will you define the fields for each instruction? You need to determine whether you want to use two or three operand codes. How will your registers be named and defined? You are free to borrow ideas from MIPS, x86, RiscV, PowerPC, and any computer Assembly Language. You will need to provide Verilog on how to decode your instructions. For an example, here is a slice of the MIPS architecture:

```
module instruction_fields(
    input [31:0] instruction,
    output [4:0] Register_Rs,
    output [4:0] Register_Rt,
    output [4:0] Register_Rd,
    output [15:0] immediate ) ;

    assign Register_Rs = instruction[25:21];
    assign Register_Rt = instruction[20:16];
    assign Register_Rd = instruction[15:11];
    assign immediate = instruction[15:0];
endmodule
```

Phase 2 - Implementation in Verilog and Simulation

In the second phase of the project, you will implement the various Verilog modules which will implement your design. You may use Xilinx ISE, iVerilog, EDA Playground, Synopsys, or Cadence tools to simulate your design. Your implementation will be tested on the two programs above.

Notes

This document will be updated with more details and information as needed.

Specifications for pts200000

Target Market: Embedded Systems Computer

Memory Organization: Harvard architecture

Address Bus Width: 13 bits

Number of Addresses 8192

Program Load Address: 0x1000

Data Bus Width: 24 bits

Number of Register File Address Bits: 4

Number Register File Registers: 16

Width of Register File Register : 24

Instruction Width: 34 bits

Size of Immediate Field: 16 bits

Maximum number of Instructions: 64

Memory Addressing Endianess : Little