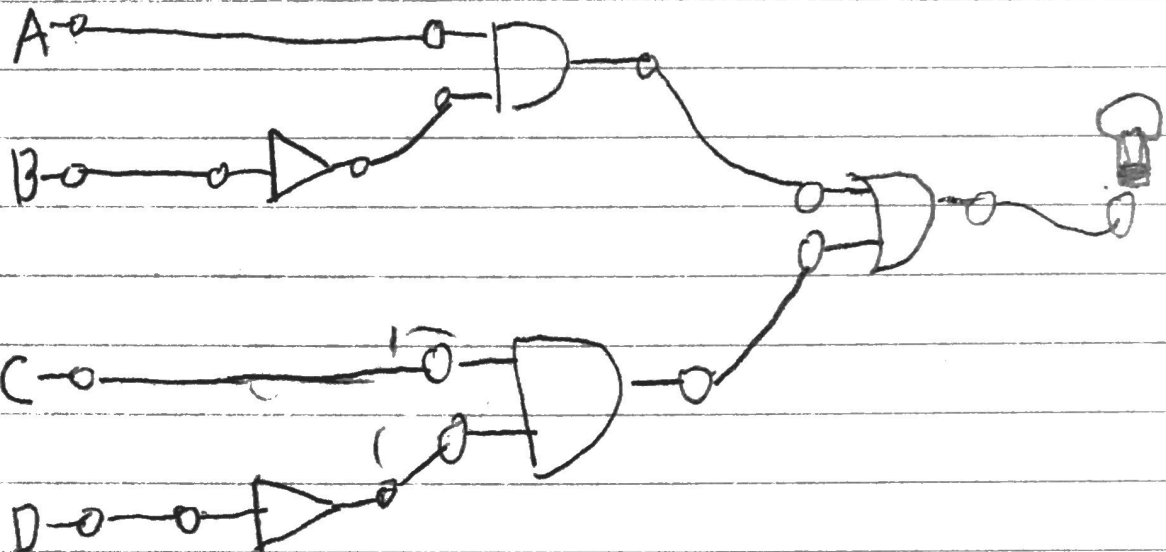


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3) Stage	CI \downarrow Adda RA, RB	IR \downarrow irmova RA, RB	MR \downarrow mrmova RA, RB
Fetch	$i\text{code}, i\text{fun} \leftarrow M_1[PC]$ $RA, RB \leftarrow M_1[PC+1]$ $V_{aP} \leftarrow PC+2$	$i\text{code}, i\text{fun} \leftarrow M_1[PC]$ $RA, RB \leftarrow M_1[PC+1]$ $V_{aIC} \leftarrow M_2[PC+2]$ $V_{aIP} \leftarrow PC+10$	$i\text{code}, i\text{fun} \leftarrow M_1[PC]$ $RA, RB \leftarrow M_1[PC+1]$ $V_{aIB} \leftarrow M_2[PC+2]$ $V_{aIP} \leftarrow PC+10$
Decode	$V_{aIA} \leftarrow R[RA]$ $V_{aIB} \leftarrow R[RB]$		$V_{aIB} \leftarrow R[RB]$
Execute	$V_{aIE} \leftarrow V_{aIB} + V_{aIA}$	$V_{aIE} \leftarrow 0 + V_{aIC}$	$V_{aIE} \leftarrow V_{aIB} + V_{aIC}$
Memory			$V_{aIM} \leftarrow M_2[V_{aIE}]$
Write back	$R[RB] \leftarrow V_{aIE}$	$R[RB] \leftarrow V_{aIE}$	$R[RA] \leftarrow V_{aIM}$
PC update	$PC \leftarrow V_{aIP}$	$PC \leftarrow V_{aIP}$	$PC \leftarrow V_{aIP}$