

MultiCore - SingleBus

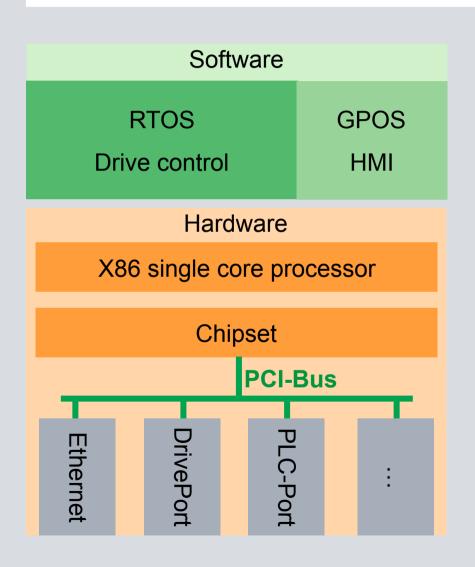
Mutual Influence between Processors and Peripherals

Overview

- System description
- Modeling of the system
- Analysis
- Results
- Summary and outlook



System description



Two main parts

- Real time drive application
- GPOS based HMI

Separated by hardware timer

- 70% RTOS
- 30% GPOS

Peripherals on PCI

- Ethernet ports
- Drive connections
- PLC connection
- ...

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Industry Sector



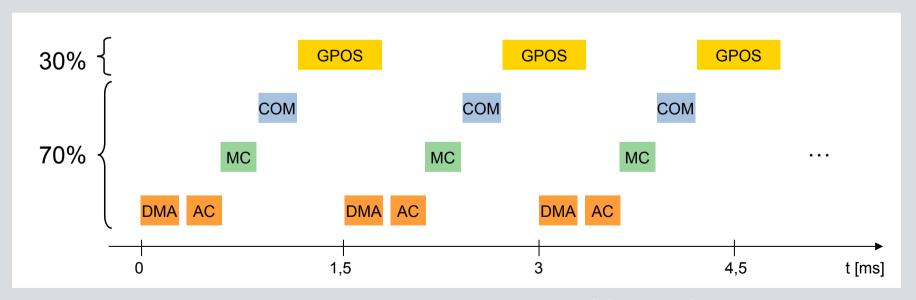
Software structure

RTOS tasks

- Axis controller (AC)
- Motion controller (MC)
- Communication (COM)

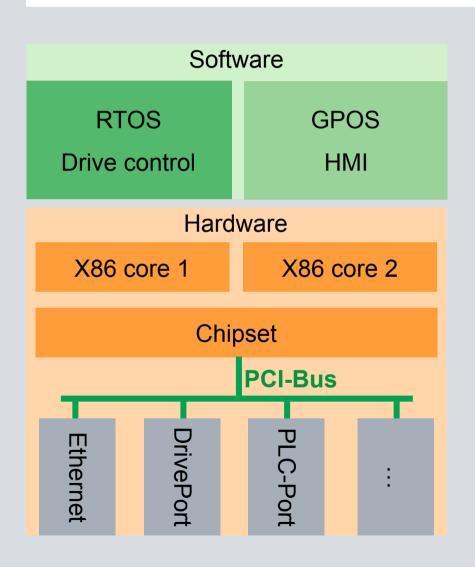
GPOS/HMI tasks

- Communication (HMI data)
- Visualization





New system design



Two main parts

- Real time drive application
- GPOS based HMI

Separated by core affinity

- 100% RTOS
- 100% GPOS

Peripherals on single PCI bus

- Ethernet ports
- Drive connections
- PLC connection
-



Expectations vs. reality

Expectations

- GPOS-HMI runs up to three times faster
 - More throughput on the network
 - Better reaction of the GUI
- Real time worst case runtime nearly unchanged

Reality

- GPOS HMI runs significantly faster
- BUT: Real time side runs up to three times slower than before!!!!
- → System analysis by replacing HMI by well-defined load tests



Reality figures

Scenario

- First analysis leads to collisions on PCI bus → further investigation
- RTOS software runs as it is, MC can run 1, 2 or 4 times slower than AC
- GPOS generates load on PCI bus by copying 4k blocks

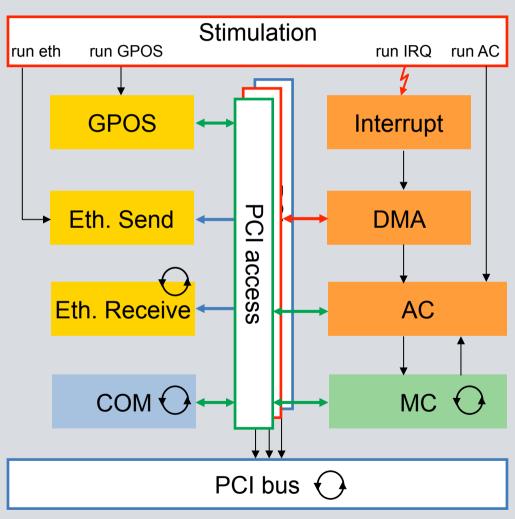
AC 1.5 ms		MC 1.5 ms		MC 3.0 ms		MC 6.0 ms	
		max.AC	max.MC	max.AC	max.MC	max.AC	max.MC
1 Core	Idle state	110 µs	365 µs	110 µs	365 µs	110 µs	365 µs
1 Core	PCI load	110 µs	365 µs	110 µs	365 µs	110 µs	365 µs
2 Core	Idle state	110 µs	365 µs	110 µs	365 µs	106 µs	365 µs
2 Core	PCI load	235 µs	925 µs	233 µs	930 µs	232 µs	920 µs

→ System modeling necessary to identify problems

Modeling of tasks

Modeling with ChronSim

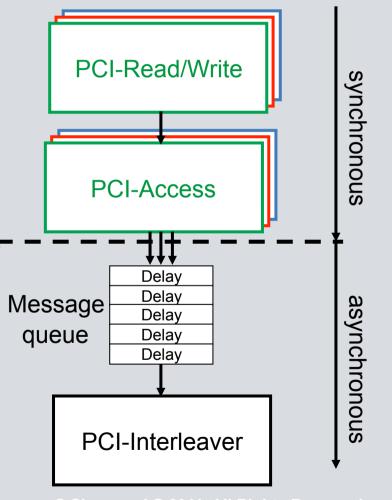
- Cyclic activation of tasks
- Synchronization with message queues
- Three channels for PCI to simulate arbitration logic
- Resources
 - CPU (GPOS, AC, MC, COM)
 - Ethernet (send / receive)
 - PCI bus
 - DMA (read)



Modeling of PCI bus

PCI bus is an independent resource

- Message queue to serialize accesses
- Queuing from three different channels
 - Mixing accesses from different sources
 - Leads to significant delays on collision
 - Various arbitration logic strategies possible
- Interleaver idles corresponding to data size
 - Normal read: 2.3 MB/s
 - Normal write: 16 MB/s
 - DMA (burst): 40 MB/s (max 128 byte)





Model vs. reality

Green numbers show deviation from reality figures

Model shows significant raise of runtime for real time tasks

Can be used for further investigation

- Different arbitration logic
- Software controlled access of non-real time tasks to PCI bus

AC 1.5 ms		MC 1.5 ms		MC 3.0 ms		MC 6.0 ms	
		max.AC	max.MC	max.AC	max.MC	max.AC	max.MC
1 Core	Idle state	108 µs	369 µs	109 µs	370 us	110 us	363 µs
	Deviation	-2 µs	+4 µs	-1 µs	+5 µs	0 µs	-2 µs
1 Core	PCI load	112 µs	384 µs	116 µs	380 µs	122 µs	378 µs
	Deviation	+2 µs	+19 µs	+6 µs	+15 µs	+12 µs	+13 µs
2 Core	Idle state	108 µs	367 µs	109 µs	366 µs	114 µs	367 µs
	Deviation	-2 µs	+2 µs	-1 µs	+1 µs	+8 µs	+2 µs
2 Core	PCI load	187 µs	904 µs	190 µs	885 µs	166 µs	860 µs
	Deviation	-48 µs	-21 µs	- 43 µs	-45 µs	- 66 µs	- 60 µs



Measures

- Reducing of PCI read
 - Reading take a lot more time than writing
 - Peripherals should write data into main memory, if possible
 - Usage of DMA
- Use of software locks
 - GPOS has to wait, until RTOS has finished PCI access
 - Drawback: Software needs a lot of changes
- Other aspects
 - Cache was also an issue
 - No modelling possible because of lack of knowledge on cache behavior



Conclusions

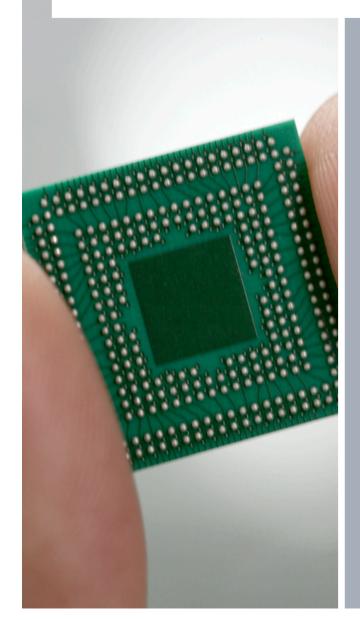
Pro

- Simulation can help to find bottlenecks
- Easy use of modeling and simulation tools
- Integrated diagrams and reporting
- Variation of system parameters to evaluate different solutions

Contra

- Model should be used early in the development
- Hardware model not available, but simulated by software
- Long calculation times

Thank you for your attention!



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