Infoblatt

Texas Instruments - Digital Signal Processor (DSP): TMS320C6711

Performance

Eight 32-Bit Instructions / Cycle
100-, 150-MHz Clock Rates / 10-, 6.7-ns Instruction Cycle Time
600, 900 MFLOPS (Million FLoating point Operations Per Second)

VelociTI - Advanced Very Long Instruction Word (VLIW) DSP Core

Eight Highly Independent Functional Units:

Four ALUs (Floating- and Fixed-Point)
Two ALUs (Fixed-Point)
Two Multipliers (Floating- and Fixed-Point)

Load-Store Architecture With 32 32-Bit General-Purpose Registers
Instruction Packing Reduces Code Size
All Instructions Conditional

Instruction Set Features

Hardware Support for IEEE Single-Precision and Double-Precision Instructions
Byte-Addressable (8-, 16-, 32-Bit Data)
8-Bit Overflow Protection
Saturation
Bit-Field Extract, Set, Clear
Bit-Counting
Normalization

L1/L2 Memory Architecture

32K-Bit (4K-Byte) L1P Program Cache (Direct Mapped)
32K-Bit (4K-Byte) L1D Data Cache (2-Way Set-Associative)
512K-Bit (64K-Byte) L2 Unified Mapped RAM/Cache (Flexible Data/Program Allocation)

32-Bit External Memory Interface (EMIF)

Glueless Interface to Asynchronous Memories: SRAM and EPROM
Glueless Interface to Synchronous Memories: SDRAM and SBSRAM
512M-Byte Total Addressable External Memory Space

Enhanced Direct-Memory-Access (EDMA) Controller (16 Independent Channels)

16-Bit Host-Port Interface (HPI)

Access to Entire Memory Map

Device Configuration

Boot Mode: HPI, 8-, 16-, 32-Bit ROM Boot
Endianness: Little Endian, Big Endian

Two 32-Bit General-Purpose Timers

Two Multichannel Buffered Serial Ports (McBSPs)

Full-duplex communication
Highly programmable clock and frame synchronization / generation
Independent framing and clocking for receive and transmit
A wide selection of data sizes, including 8, 12, 16, 20, 24, and 32 bits
Up to 256 channels each
µ-Law and A-Law companding

Direct interface to:
- industry-standard codecs
- analog interface chips (AICs)
- T1/E1 framers
- MVIP switching and ST-Bus compliant devices including:
  - MVIP framers
  - H.100 framers
  - SCSA framers
- IOM-2 compliant devices
- AC97 compliant devices
- IIS compliant devices
- Serial-Peripheral-Interface (SPI) compatible devices (Motorola)

Flexible Phase-Locked-Loop (PLL) Clock Generator

IEEE-1149.1 (JTAG) Boundary-Scan-Compatible

0.18-µm/5-Level Metal Process,CMOS Technology, 3.3-V I/Os, 1.8-V Internal

256-Pin Ball Grid Array (BGA) Package (GFN Suffix)
C6211, C6211B, C6711, and C6711B are Pin-Compatible