Improved Performance of FFT Based Cardiac Analyzer Using Advanced Booth Algorithm

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Abstract— **Cardiac vascular is a disease which plays a high risk factor in the world, where many people leads to death due to sudden cardiac arrest. Doctor uses several test to detect the factors that put people at high risk of Sudden Cardiac Attack like Echocardiography (ECG), Multi Gated Acquisition Scan (MUGA) Test or Cardiac Magnetic Resonance Imaging(MRI), Cardiac Catheterization, and Blood Test which all are in off line analysis of cardiac patient but recently proposed the method of real time Cardiac monitoring system which is used to analyze the abnormality of ECG signal using Fast Fourier Transform (FFT) and send comments to the receiver using short message service(SMS) through Global System Mobile(GSM), where the Fast Fourier Transform (FFT) used in this has more delay, which takes much time in computation due to the presence of multiplier in it. Thus to increase the speed of FFT the Advanced booth algorithm is proposed here, in which the number of slice, number of 4-input LUTs and number of bonded IOB gets reduced when compare to the other existing FFT speed increment algorithm, Hence it is proved that the proposed FFT analyzer improved the overall performance of existing system.**

Keywords- Advanced Booth Algorithm, Cardiac Arrest, ECG, FFT and Multiplier

I. INTRODUCTION

Cardiac arrest is a major problem in the human body which is stops the blood circulation suddenly due to failure of the heart. Heart rate can be measured by using the ECG, where the PQRST waveform occurred by rhythm which is used to analysis the normal and abnormality of the heart rate [1 - 3]. The change in pumping of heart causes changes in rhythm of PQRST wave is called arrhythmia. Cardiac arrest occurs in fraction of second which may not be identifying easily. Hence recently proposed the real time Cardiac patient monitoring using FFT algorithm which is predict the cardiac arrest before it occurs, here the ECG signal is acquired from the sensor module which is given to kalman filter to extract the future ECG signal, from the extracted signal the FFT processor is find whether the future ECG signal is normal or abnormal of Cardiac arrest [4].

The speed of FFT processor is depending on multiplier, where delay occurs in digital processing which will reduce the speed and increases the power consumption. To overcome this problem the high speed multipliers and adders are required to speed up the FFT. Hence we propose the advanced booth algorithm to perform the high speed FFT function.

Various types of algorithm are available to increase the multiplier speed which helps to increase the performance of FFT at high speed, such as Vedic mathematics it has 16 sutras and 13 sub sutras where each sutra has different operation. Among the 16 sutras nikilam and urthras are applicable for the multiplications purpose this Vedic method performing high speed multiplication with some partial product addition **[5 - 7].** Array multiplier is performed the function based on its regular structure here multiplication process followed addition with shifting function and final partial product addition is performed by carry propagation adder it introduce delay for carry propagation**.** Multiplication based on Booth algorithm increase the speed of the multiplication by reducing the intermediate steps of it. Thus it concluded radix 8 is higher speed than radix 2 and radix 4 [8 - 9]. In this all existing multiplication algorithm reflect performance degradation is more timing waste, high power consumption and it takes more number of slices and input LUTs.

To overcome these existing problems, we propose Advanced Booth algorithm to perform high speed FFT analysis, it eliminates carry propagation delay with less number of logical blocks. The propose method achieves less area, low power and high speed.

II. PROPOSED SYSTEM

Proposed system design the reliable multiplier based on Adaptive hold logic circuit implementation. The multiplier based on the Variable-latency pipelined multiplier architecture with an advanced booth radix-4 algorithm. The proposed algorithm performing multiplication function with three steps, such as partial product generation, performed the partial product addition continuously until the last two rows are remained and finally calculate the multiplication result by workout the last two rows addition.

Proposed algorithm decreases the 50% of partial product in the first step. Proposed system using Advanced Booth encoding (MBE) table to perform the multiplication which is called competent Booth encoding and decoding system, here multiplication performed U by V, U is multiplicand and V is multiplier, using proposed algorithm first grouping multiplier by 3 bits and encoding into one of {-2, -1, 0, 1, 2} which is shown in Table I. The Booth decoder performed the partial products using the encoded signals and finally performed the partial product addition using Wallace tree.

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To improve the performance of multiplier we need to include the parallel processing which is useful to reduce the number of subsequent stages. To perform the proposed algorithm using Radix – 2 method had two drawbacks. Which are: (i) the maximum number of arithmetic functions and shifting operations are inconsistent and problematic to designing parallel multipliers. (ii) The numbers are isolated 1's the algorithm becomes ineffective. To overcome this problem using modified Radix-4 method in proposed algorithm.

TABLE I
RADIX-4 ADVANCED BOOTH ENCODING TABLE

Block	Partial Product
000	0
001	1*Multiplicand
010	1*Multiplicand
011	2*Multiplicand
100	2*Multiplicand
101	-1*Multiplicand
110	-1*Multiplicand
111	0

This proposed advanced booth algorithm based multiplier performed high speed operations and reduces the overall number of slices and 4 input LUTs.

III. FAST FOURIER TRANSFORM

The proposed Advanced Booth algorithm based multiplier is implemented in this section to verify the performance of FFT analyzer. The FFT algorithm is used to perform high speed computational evaluation of DFT and IDFT of sequences with less no of multiplication and addition compare to direct method of DFT evaluation. the FFT decomposes the set of data to be transformed into a series of smaller data sets to be transformed. Then, it decomposes those smaller sets into even smaller sets. At each stage of processing, the results of the previous stage are combined in special way. Finally, it calculates the DFT of each small data set [10-11]. For example, an FFT of size 32 is broken into 2 FFTs of size 16, which are broken into 4 FFTs of size 8, which are broken into 8 FFTs of size 4, which are broken into 16 FFTs of size 2. Calculating a DFT of size 2 is simple one (radix-2) FFT begins by calculating N/2 2-point DFTs. This is applicable for less number of sequences less than 10. By using radix – 4 the "twiddle factors" are all 1, -1, j, or -j, which can be applied without any multiplications at all.

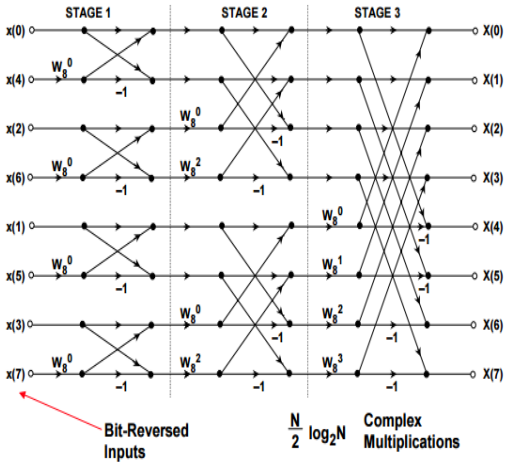


Fig 1 Eight-point decimation-in-time FFT algorithms

Fig 1 shows the butterfly structure representation of 8 point FFT. In order to simplify the diagram, note that the quantity W_N is defined as

$$W_N=e^{-j2\pi/N} \quad \dots (1)$$

This leads to the definition of the twiddle factors as:

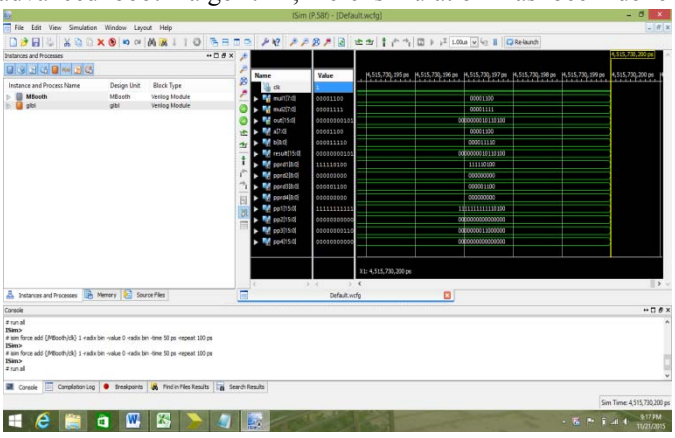
$$W_N^{nk}=e^{-j2\pi nk/N} \quad \dots (2)$$

The twiddle factors are based on sine and cosine functions.

IV. RESULT

A. *Simulation Result of Multiplier :*

Fig 2 shows the simulation result of multiplier based on advanced booth algorithm; here simulation has been done



using Xilinx. The results are evaluated and the performance of system architecture is analyzed using the input sequence mux1 = 1100 and mux2 = 1111. The multiplier output 0000000010110100 displayed in fig 2.

Fig 2 Simulation Output of Multiplier

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B. ***Comparison output of proposed multiplier :***

The comparison statement of existing and proposed system architecture is presented in table 2 and 3. Table 2 show the result of number of slices, Look up tables (LUT) and number of bonded IOB used in existing Multiplier and proposed Multiplier. Similarly table 3 displays the comparison results of existing and proposed FFT processor result. Fig 3 and 4 display the graphical representation of multiplier and FFT processor utilization chart.

TABLE II
COMPARISON RESULT OF MULTIPLIERS

Method	No of slices	No of 4-input LUTs	No of bonded IOB
Array	258	505	64
Urdhvathiryakbhayam	125	219	64
Nikhilam sutra	162	250	66
Advanced Booth	99	148	33

The simulation result of proposed multiplier shows that there is considerable reduction in number of slices, number of LUTs and No of bonded IOB.

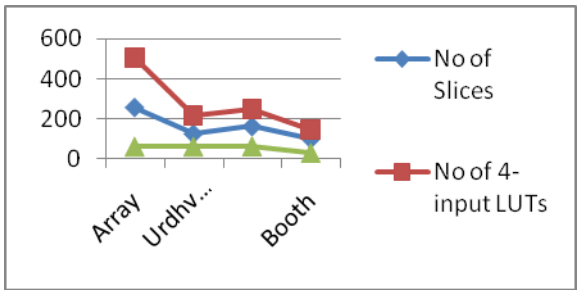

Fig 3 Graphical representation Multiplier utilization report

TABLE III
COMPARISON OF OUTPUT OF PROPOSED FFT PROCESSOR

Method	No of slices	No of 4-input LUTs
Urdhvathiryakbhyam	3610	6139
Nikhilam sutra	3317	5278
Advanced Booth	1615	2914

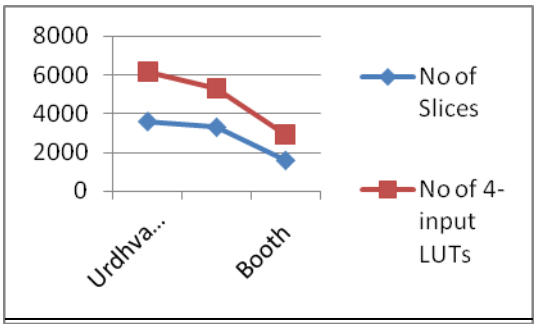

Fig 4 Graphical representation FFT processor utilization report

V. CONCLUSION

FFT is a simplest and powerful algorithm to produce n-point DFT. It has many applications such as signal processing, image processing, communication, and spectrum analysis. In this paper a novel FFT processor design is presented using advanced booth algorithm. Simulation results of the proposed FFT processor design utilizes 1615 slices to perform 8-point FFT compared to 3610 slices for Urdhvathiryakbhyam and 3317 slices for Nikhilam sutra, similarly 2914 4-input LUTs to perform 8-point FFT compared to 6139 LUTs for Urdhvathiryakbhyam and 5278 LUTs for Nikhilam sutra of the existing FFT processor. Hence the overall area of the proposed FFT processor is reduced considerably. This increases the computation speed of the processor. Hence it is evident that the proposed FFT processer incorporating compressor-based multiplier outperforms the existing FFT processors. This proposed FFT algorithm is implemented FFT based Cardiac analyzer and evaluate the performance of Cardiac system.

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