CSC258 Lab1 Pre-Lab Report

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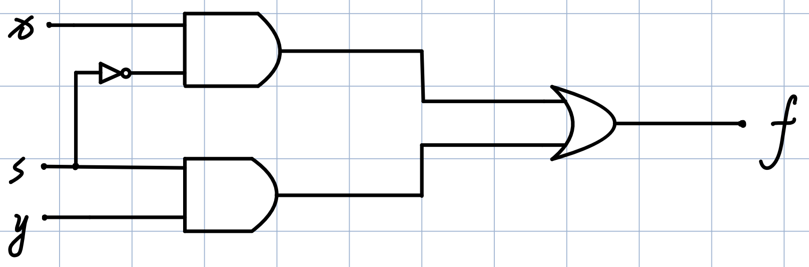
Part I

$$f = xs' + ys$$

We could express the above Boolean function using logic words :

$$f = (x \text{ AND } (\text{NOT } s)) \text{ OR } (y \text{ AND } s)$$

1. Draw the gate diagram that implements this 2-to-1 multiplexer design.



2. Write out the truth table for this design.

x	s	y	xs'	ys	f
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	1	1
1	0	0	1	0	1
1	0	1	1	0	1
1	1	0	0	0	0
1	1	1	0	1	1

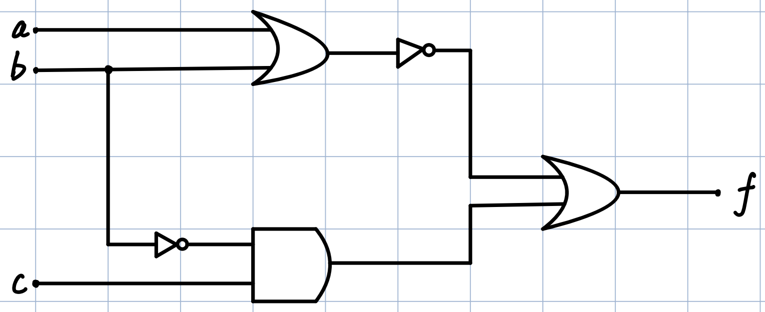
Part II

$$f = (a+b)' + cb'$$

We could express the above Boolean function using logic words :

f = (NOT (a OR b)) OR (c AND (NOT b))

1. Draw the gate diagram for the function shown above.



2. Write out the truth table for this expression.

a	b	c	$(a+b)'$	cb'	f
0	0	0	1	0	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	0	0	0
1	1	1	0	0	0

3. Yes, there is a cheaper implementation for the design that uses fewer gates.

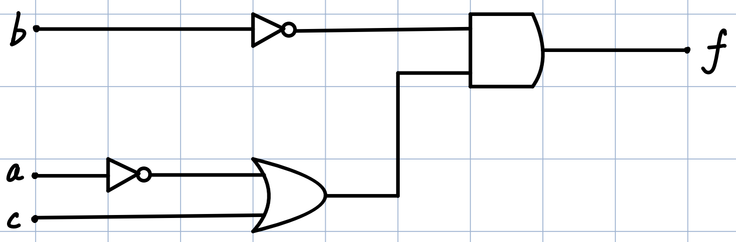
$$f = (a+b)' + cb'$$

$$= a'b' + cb' \quad \text{by De Morgan's Law}$$

$$= b'(a'+c)$$

which in logic words: $f =$ (NOT b) AND ((NOT a) OR c)

① Draw the gate diagram for the function shown above.

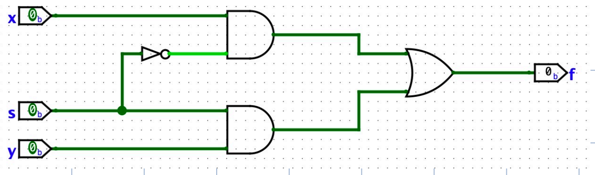


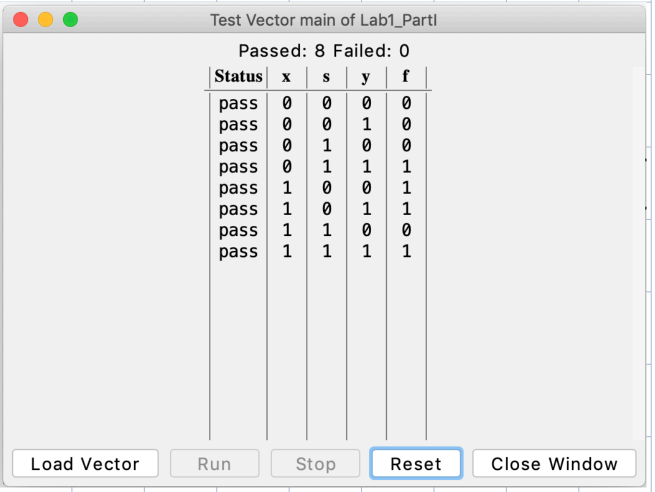
② Write out the truth table for this expression.

a	b	c	b'	a'+c	f
0	0	0	1	1	1
0	0	1	1	1	1
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	0	1	0

Part III

1. Implemented circuit from Part I and its test result screenshots.

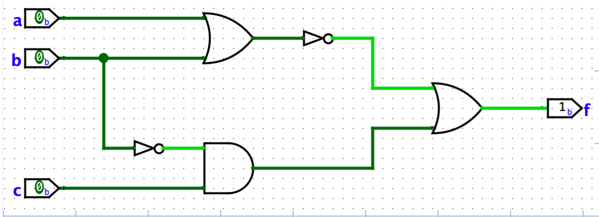


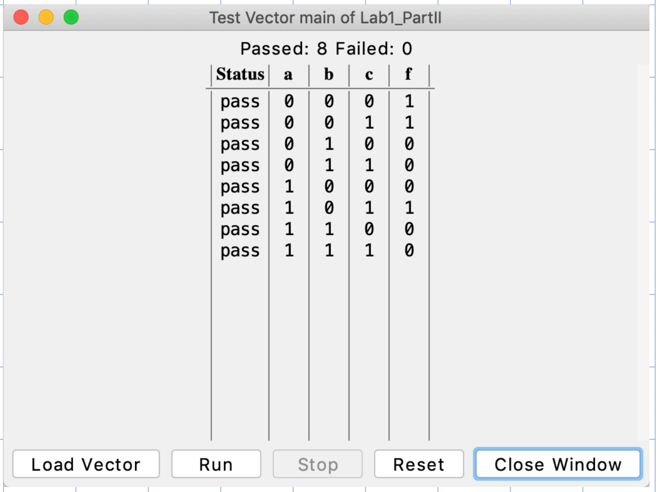


Passed: 8 Failed: 0

Status	x	s	y	f
pass	0	0	0	0
pass	0	0	1	0
pass	0	1	0	0
pass	0	1	1	1
pass	1	0	0	1
pass	1	0	1	1
pass	1	1	0	0
pass	1	1	1	1

2. Implemented circuit from Part II and its test result screenshots.





Passed: 8 Failed: 0

Status	a	b	c	f
pass	0	0	0	1
pass	0	0	1	1
pass	0	1	0	0
pass	0	1	1	0
pass	1	0	0	0
pass	1	0	1	1
pass	1	1	0	0
pass	1	1	1	0