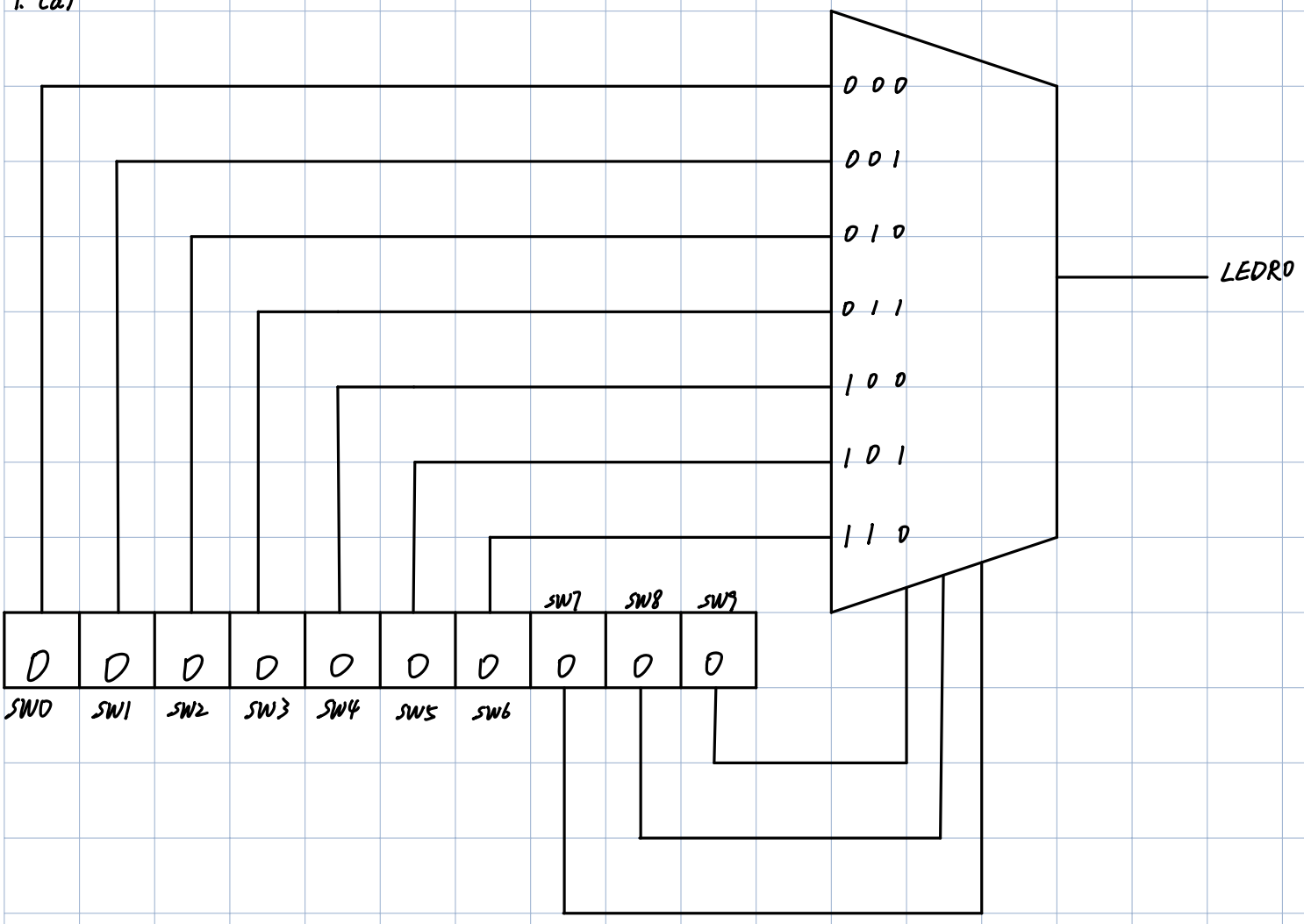
CSC258 Lab3 Pre-Lab Report

Name: Yulin Wang

Student #: 1003942326

Part I

1. (a)

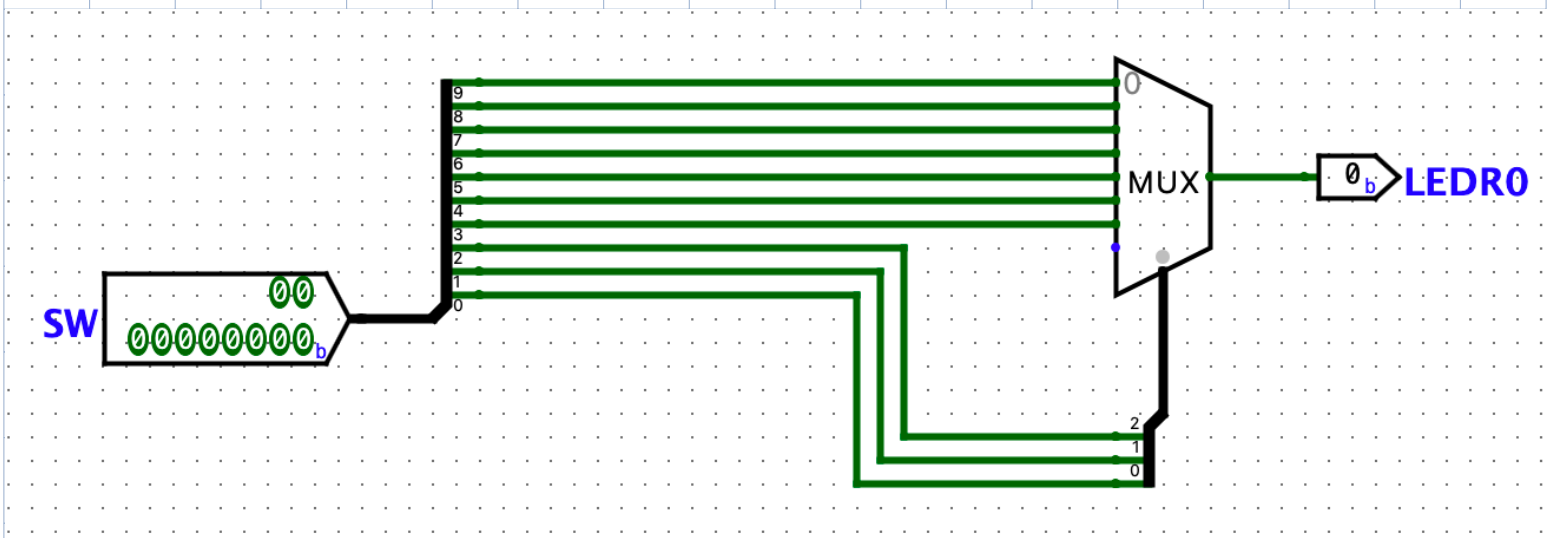


1. (b)

The multi-bit input needs to be 10 bits long.

Since we need 7 data bits for input and 3 bits for select bits.

2.



3.

Test Vector main of lab3_part1

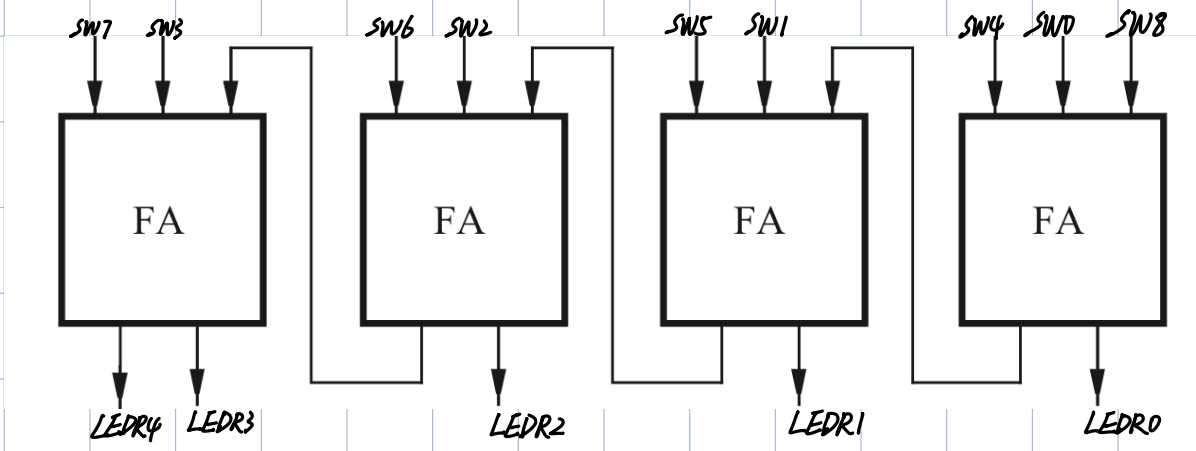
Passed: 14 Failed: 0

Status	SW	LEDR0
pass	01 1111 1000	0
pass	10 0000 0000	1
pass	10 1111 1001	0
pass	01 0000 0001	1
pass	11 0111 1010	0
pass	00 1000 0010	1
pass	11 1011 1011	0
pass	00 0100 0011	1
pass	11 1101 1100	0
pass	00 0010 0100	1
pass	11 1110 1101	0
pass	00 0001 0101	1
pass	11 1111 0110	0
pass	00 0000 1110	1

Load Vector | Run | Stop | Reset | Close Window

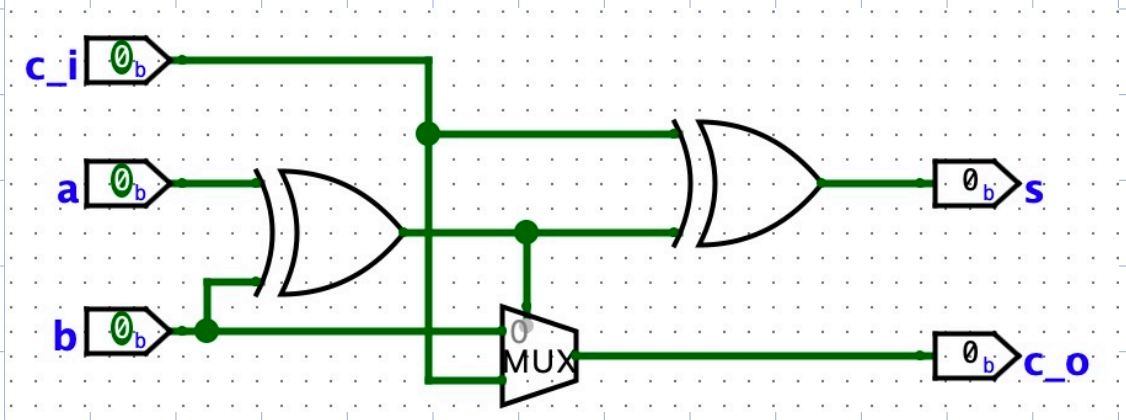
Part II

1.

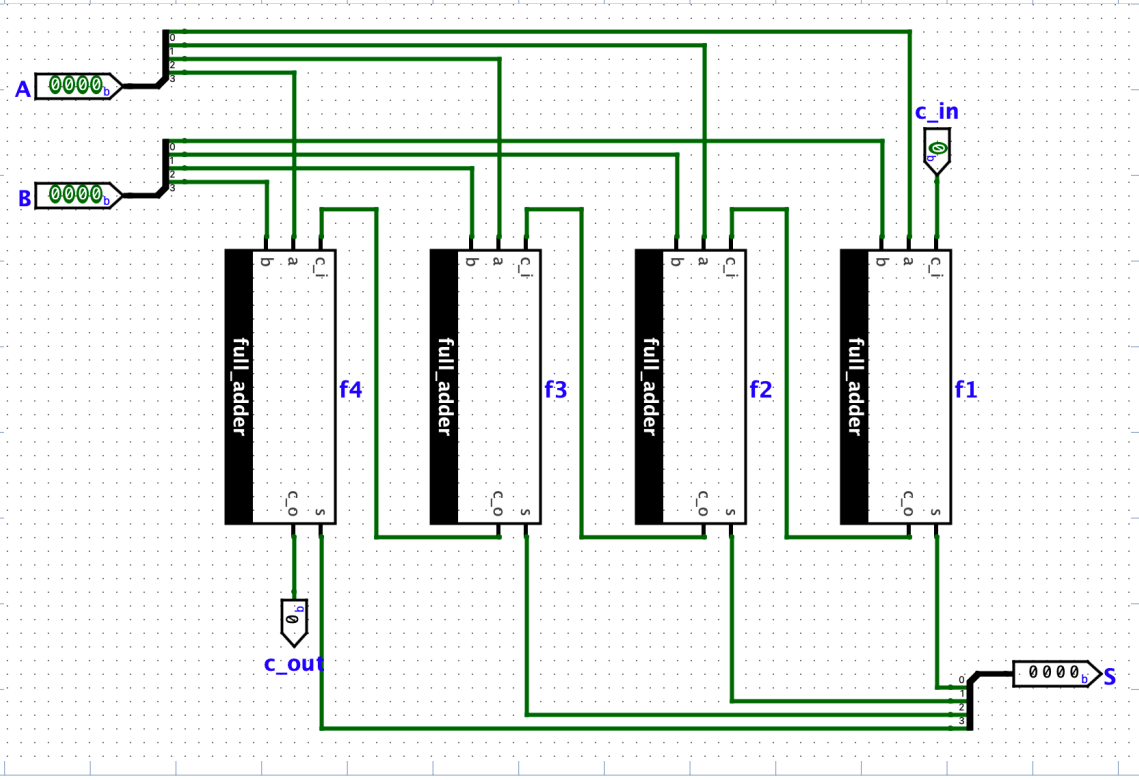


2.

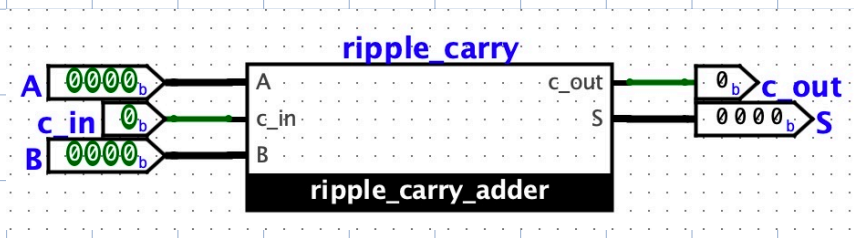
Full adder



Four-bit ripple-carry adder



3.



Test Vector main of lab3_part2

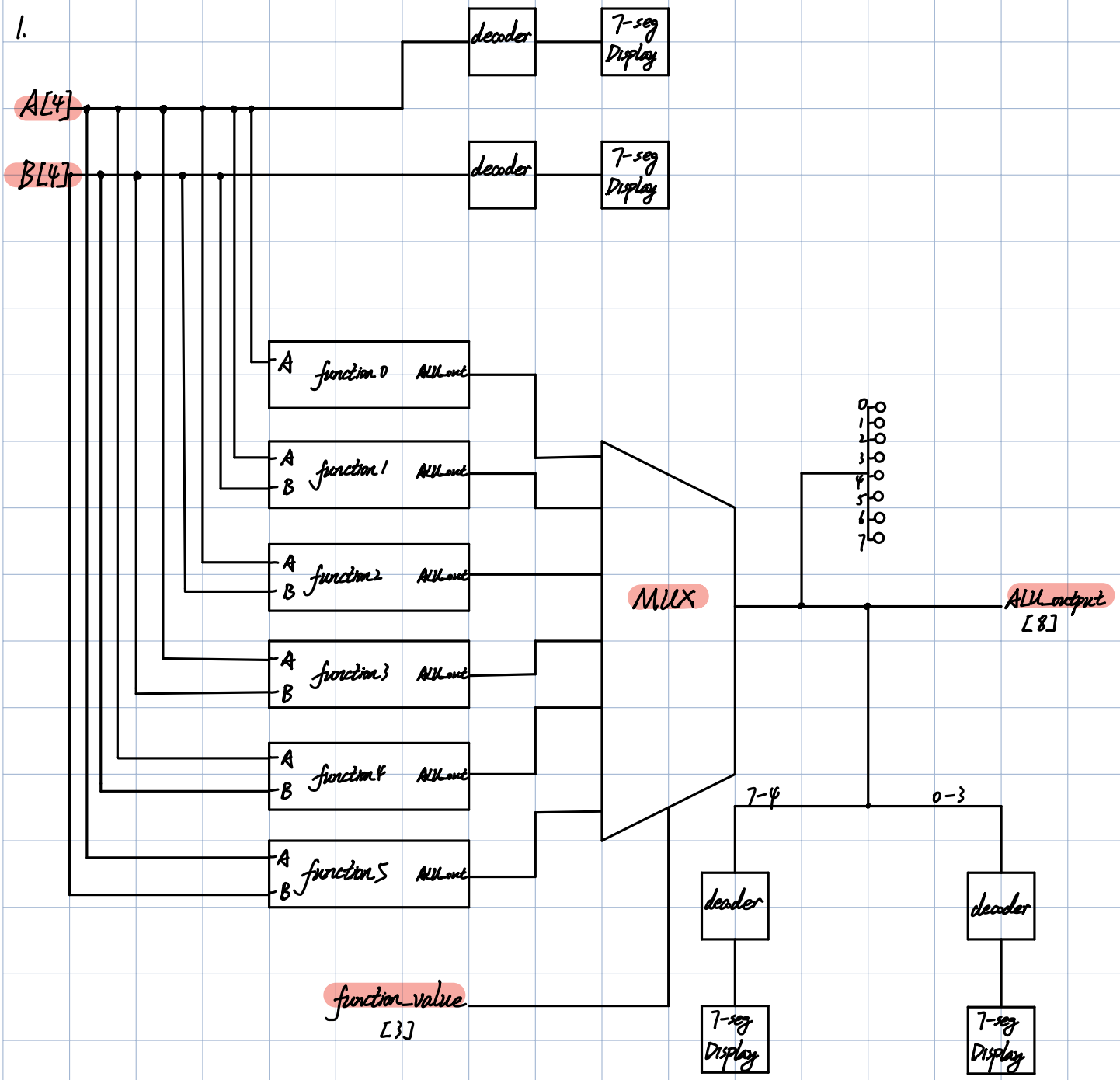
Passed: 10 Failed: 0

Status	A	B	c_in	S	c_out
pass	0000	0000	0	0000	0
pass	0001	0000	0	0001	0
pass	0010	0011	0	0101	0
pass	1111	0001	0	0000	1
pass	1111	1111	0	1110	1
pass	0000	0000	1	0001	0
pass	0001	0000	1	0010	0
pass	0010	0011	1	0110	0
pass	1111	0001	1	0001	1
pass	1111	1111	1	1111	1

Load Vector | Run | Stop | Reset | Close Window

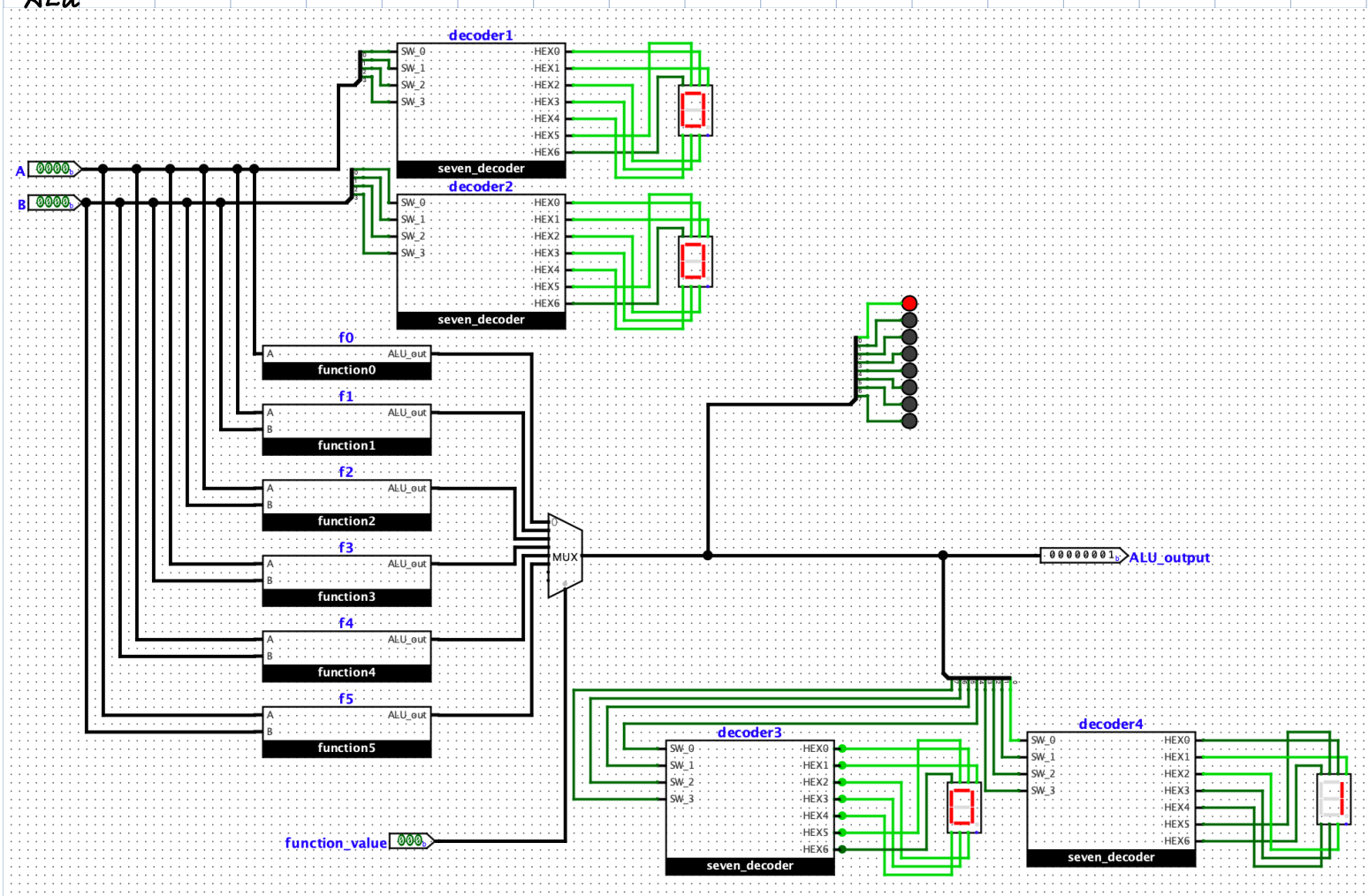
Part III

1.

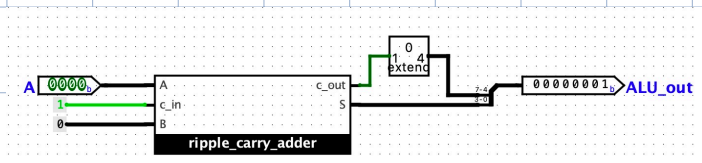

decoder
7-seg Display
A[4]
B[4]
decoder
7-seg Display
A
B
function 0
ALU_out
function 1
function 2
function 3
function 4
function 5
MUX
0
1
2
3
4
5
6
7
ALU_output [8]
7-4
0-3
decoder
decoder
7-seg Display
7-seg Display
function_value [3]

2.

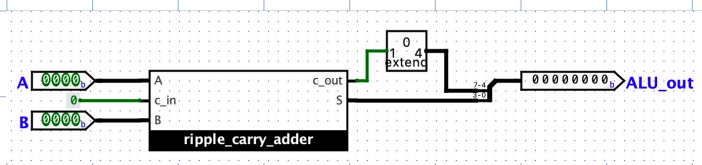
ALU



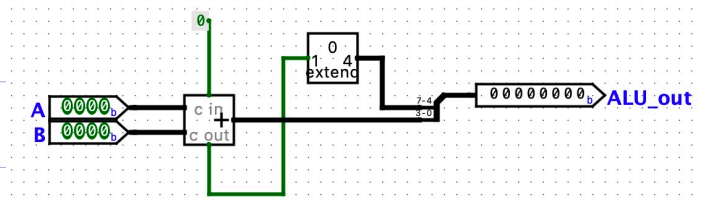
function 0



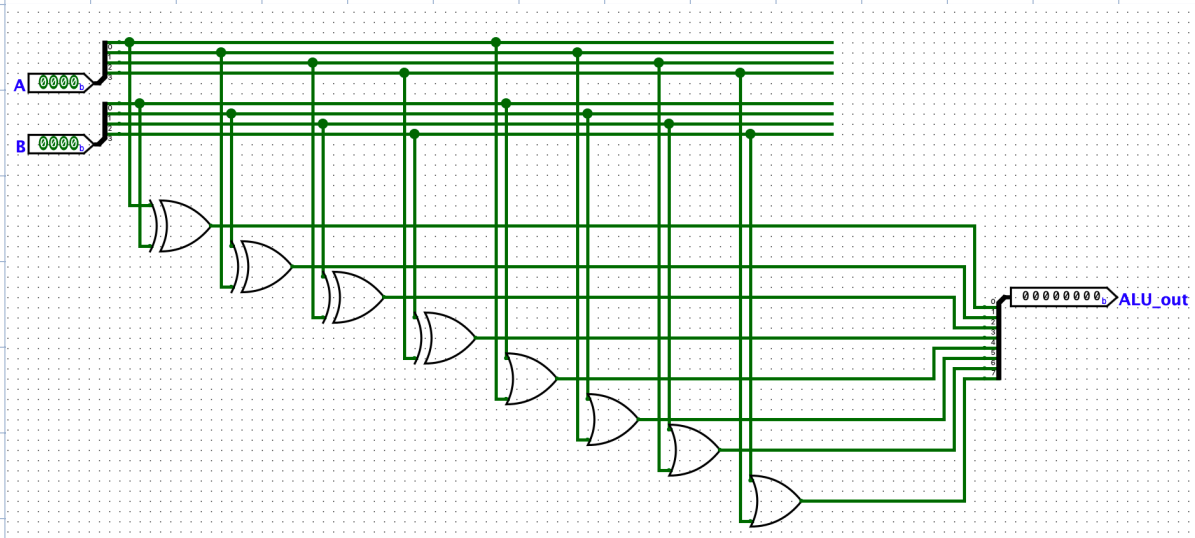
function 1



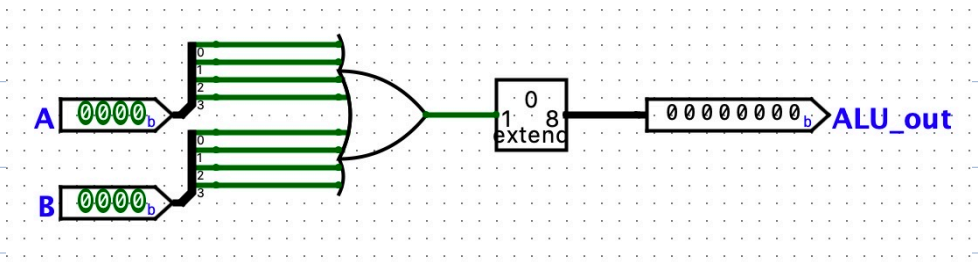
function 2



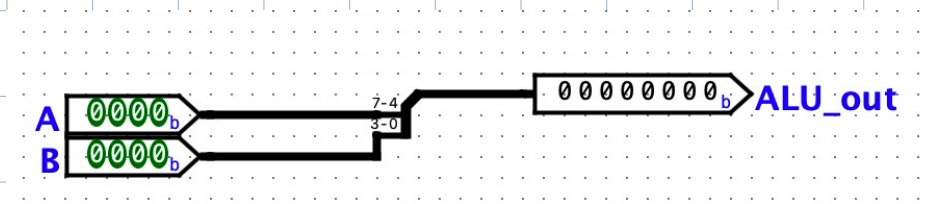
function 3



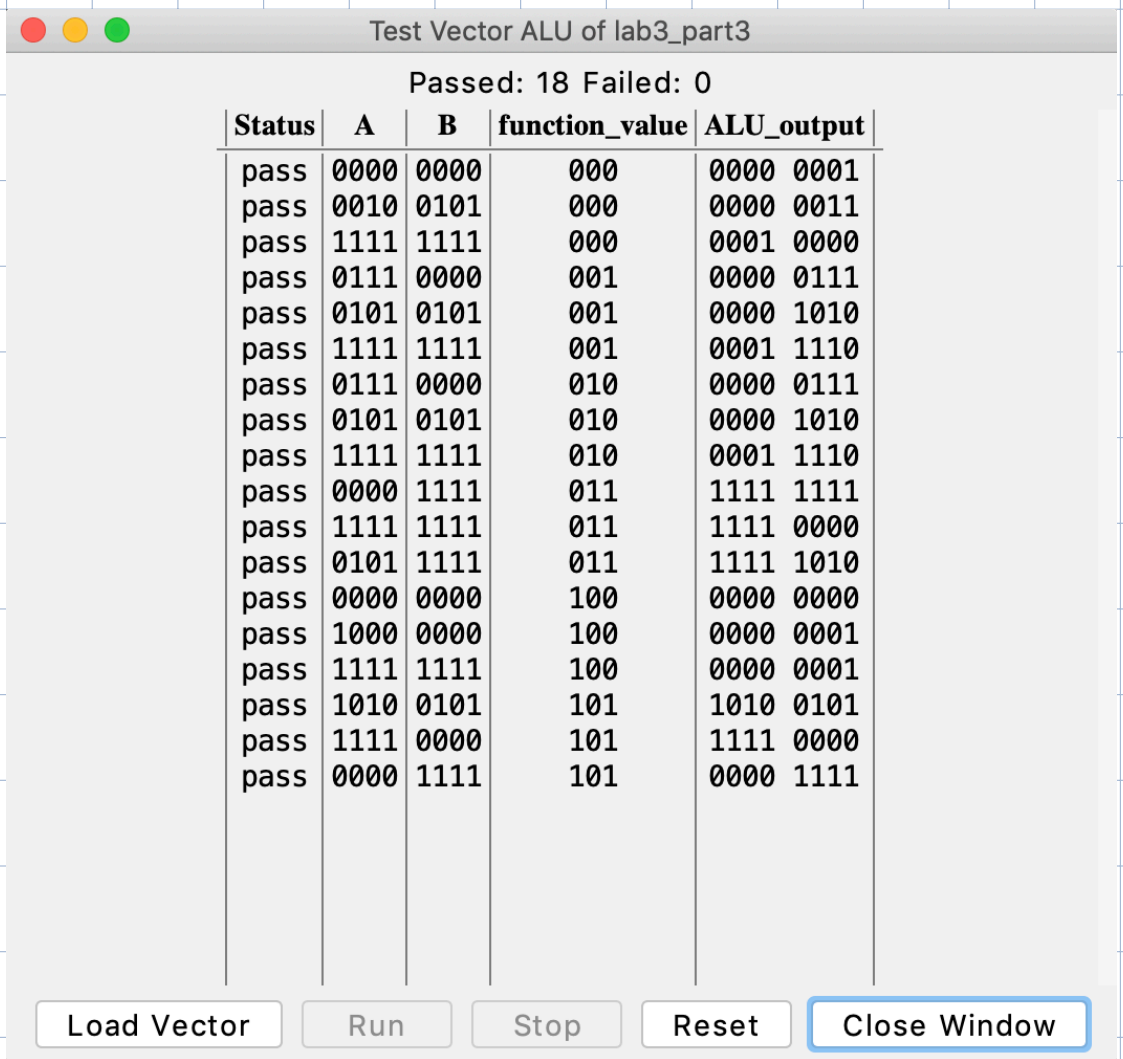
function 4



function 5



3.



Status	A	B	function_value	ALU_output
pass	0000	0000	000	0000 0001
pass	0010	0101	000	0000 0011
pass	1111	1111	000	0001 0000
pass	0111	0000	001	0000 0111
pass	0101	0101	001	0000 1010
pass	1111	1111	001	0001 1110
pass	0111	0000	010	0000 0111
pass	0101	0101	010	0000 1010
pass	1111	1111	010	0001 1110
pass	0000	1111	011	1111 1111
pass	1111	1111	011	1111 0000
pass	0101	1111	011	1111 1010
pass	0000	0000	100	0000 0000
pass	1000	0000	100	0000 0001
pass	1111	1111	100	0000 0001
pass	1010	0101	101	1010 0101
pass	1111	0000	101	1111 0000
pass	0000	1111	101	0000 1111