CSC258 Lab2 Pre-Lab Report

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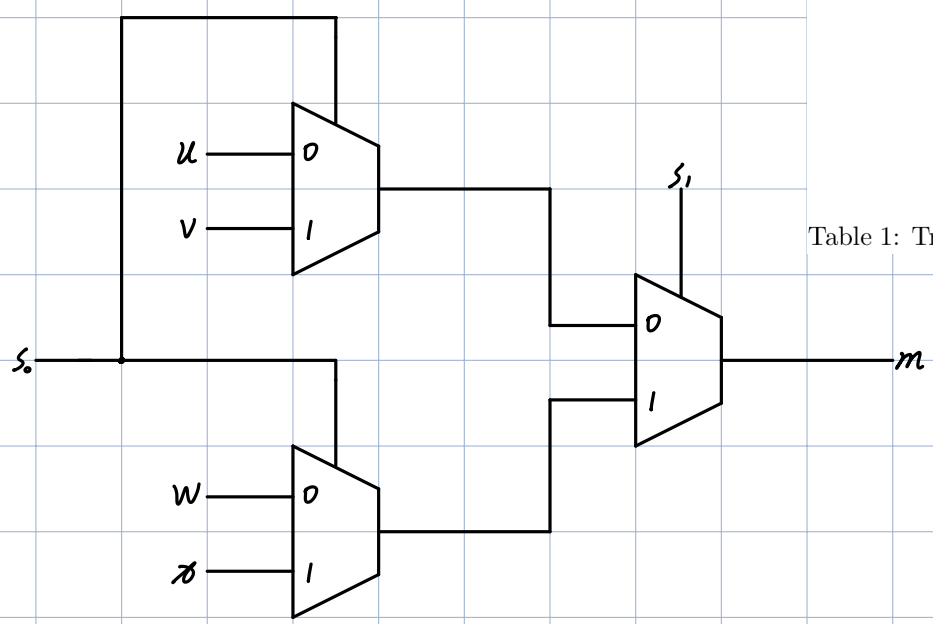
Part II

1. Since a 4-to-1 multiplexer has 6 inputs, u, v, w, x, s_0, s_1,
   so its truth table would have $2^6 = 64$ rows

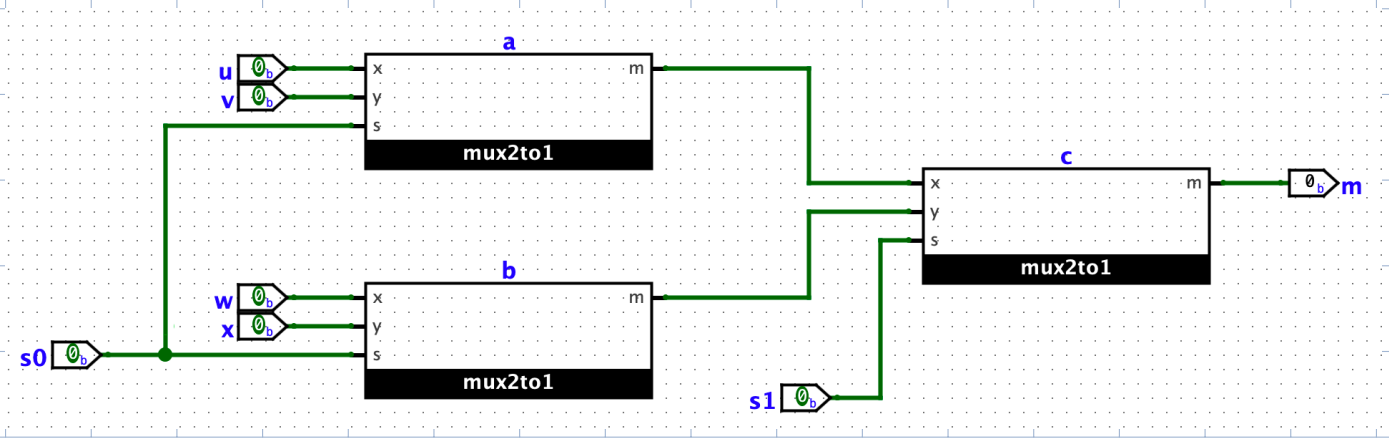
2.



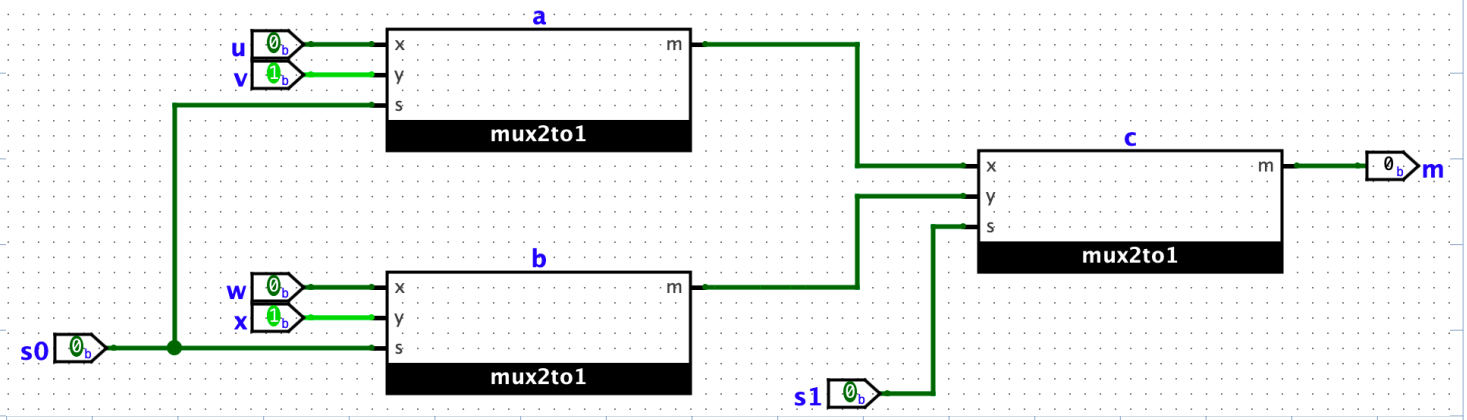
$s_1 s_0$	m
00	u
01	v
10	w
11	x

Table 1: Truth table for a 4-to-1 multiplexer

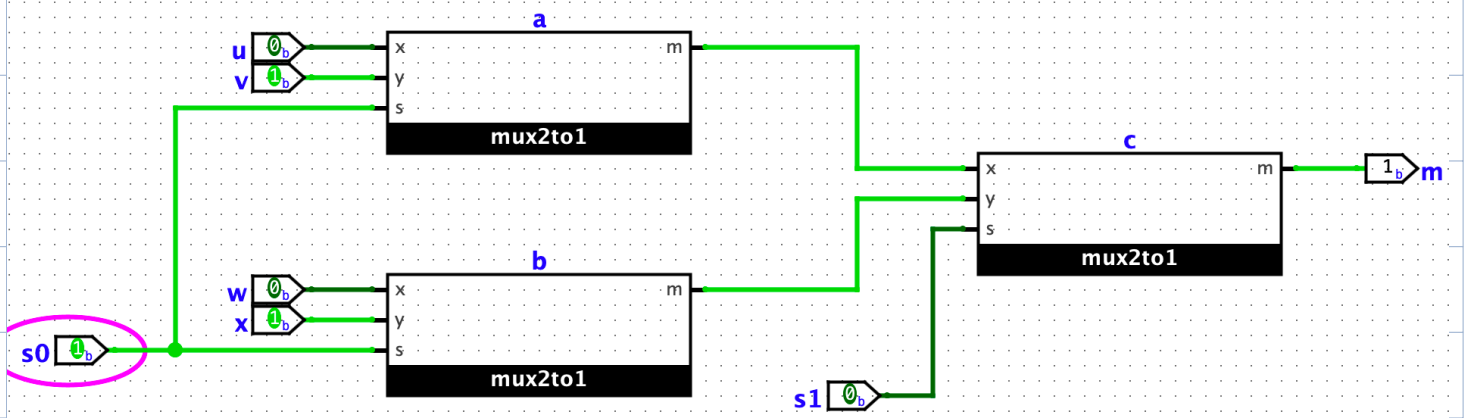
3.



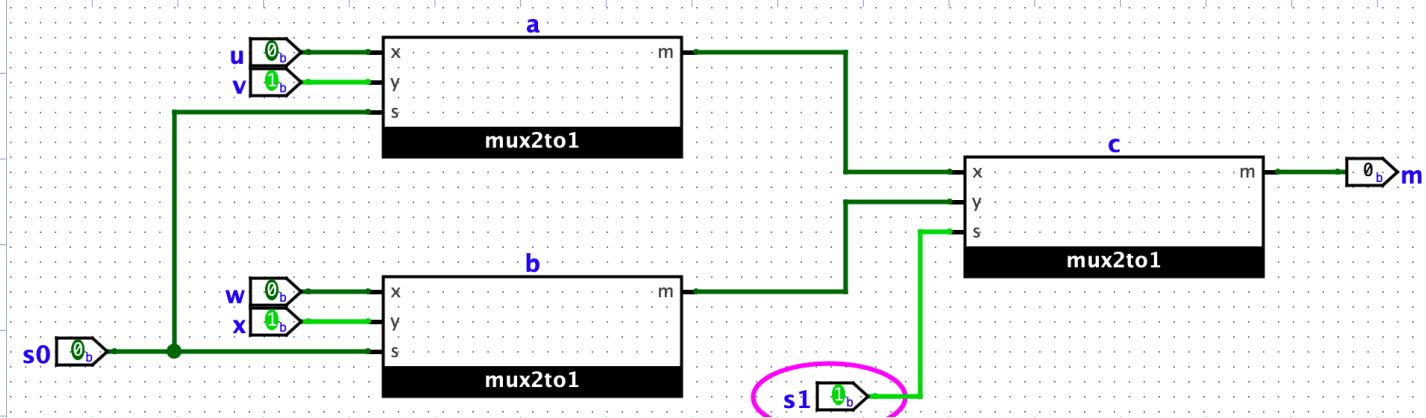
4. ① Test when $s_0 = 0$, $s_1 = 0 \Rightarrow m = u$



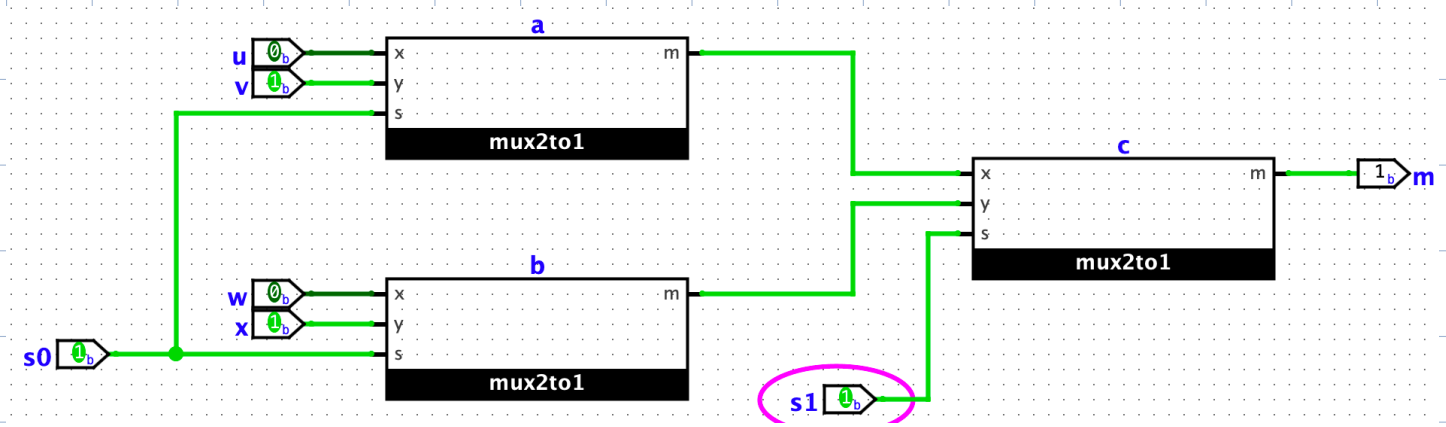
② Test when $s_0 = 1$, $s_1 = 0 \Rightarrow m = v$



③ Test when $s_0 = 0$ $s_1 = 1 \Rightarrow m = w$

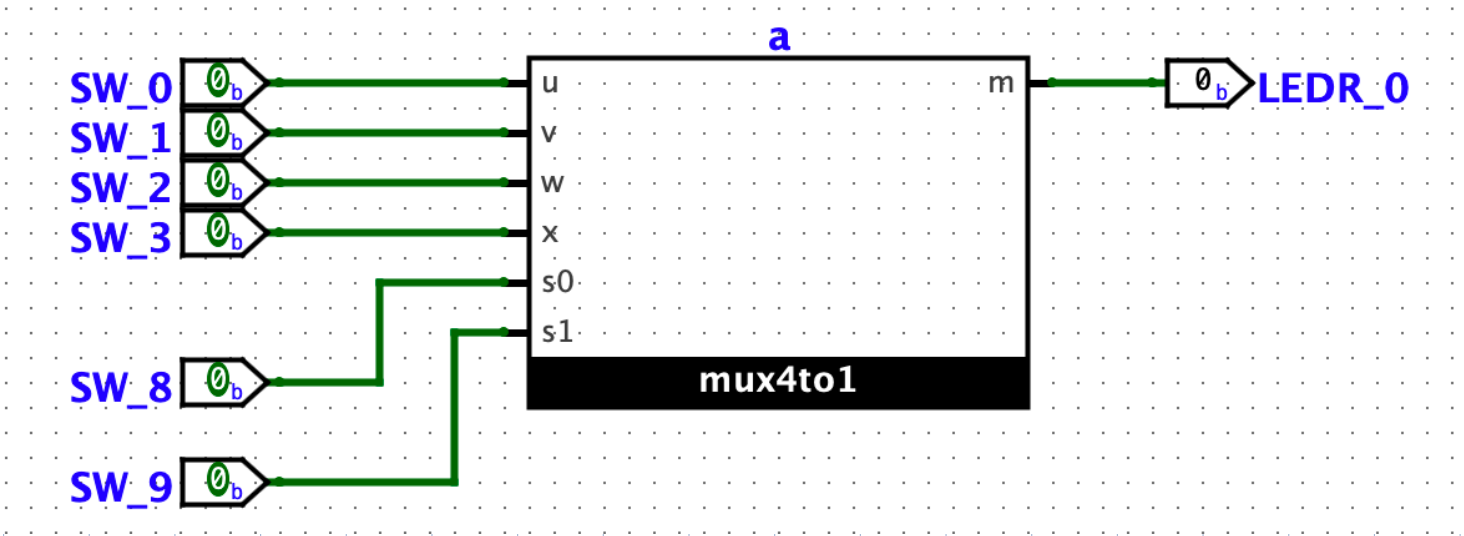


④ Test when $s_0 = 1$, $s_1 = 1 \Rightarrow m = x$

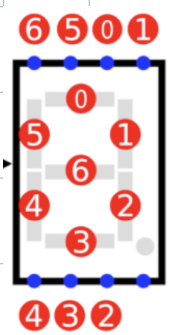


5.

Map your Logisim design to the DE1-SoC board inputs and outputs. Use switches SW_{9-8} as the 2-bits input, and switches SW_{0-3} as the data inputs (labeled as u,v,w,x in Figure 3). Connect the output m to $LEDR_0$. **(PRELAB)**

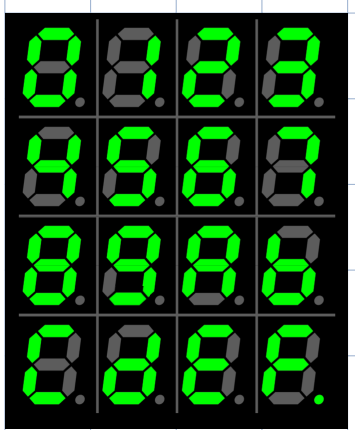


Part III



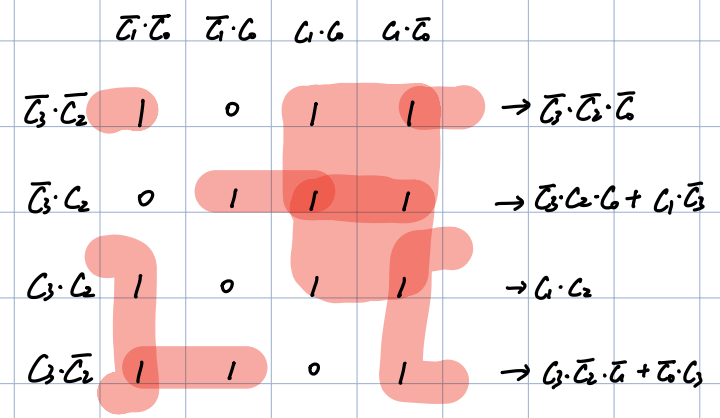
Combined truth table for 7 segments:

Character	c3	c2	c1	c0	HEX0	HEX1	HEX2	HEX3	HEX4	HEX5	HEX6
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
A	1	0	1	0	1	1	1	0	1	1	1
b	1	0	1	1	0	0	1	1	1	1	1
C	1	1	0	0	1	0	0	1	1	1	0
d	1	1	0	1	0	1	1	1	1	0	1
E	1	1	1	0	1	0	0	1	1	1	1
F	1	1	1	1	1	0	0	0	1	1	1

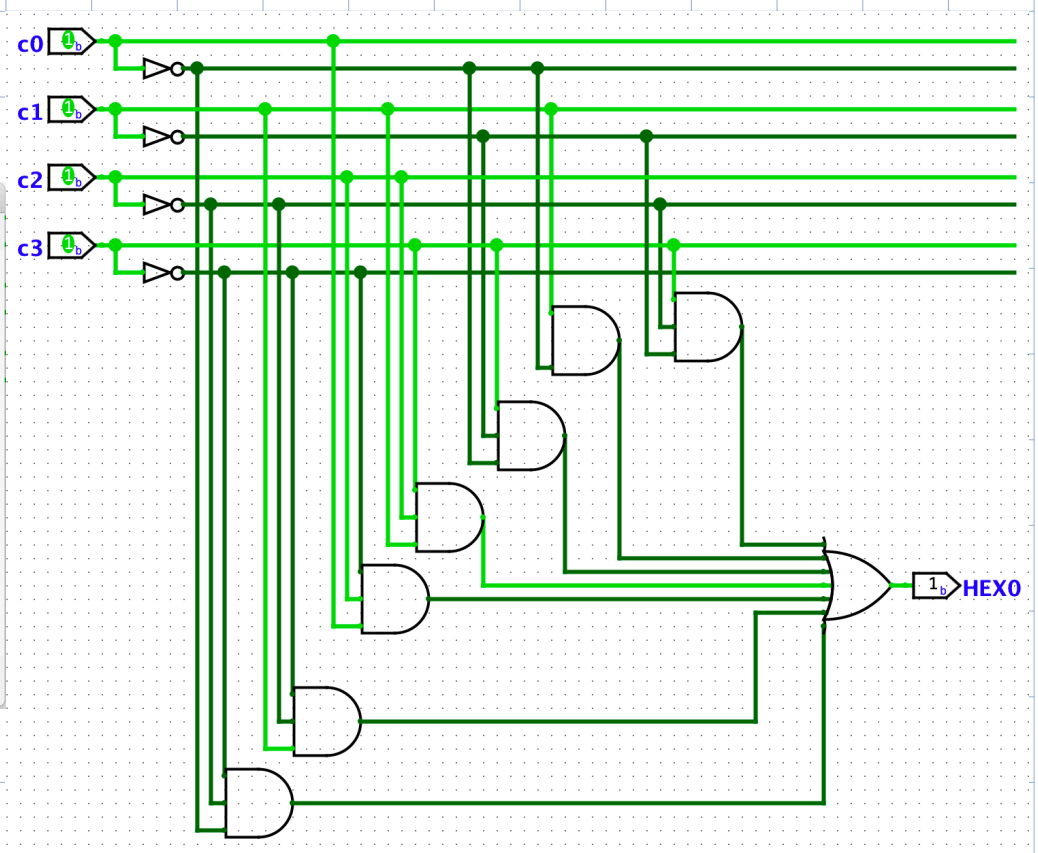


Segment 0

Segment 0					
Character	c3	c2	c1	c0	HEX0
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
A	1	0	1	0	1
b	1	0	1	1	0
C	1	1	0	0	1
d	1	1	0	1	0
E	1	1	1	0	1
F	1	1	1	1	1



Expression: $\bar{c}_3\bar{c}_2\bar{c}_0 + \bar{c}_3 c_2 c_0 + c_1\bar{c}_3 + c_1 c_2 + c_3\bar{c}_2\bar{c}_1 + \bar{c}_1 c_3$



Test Vector Segment0 of Lab2_Pat3

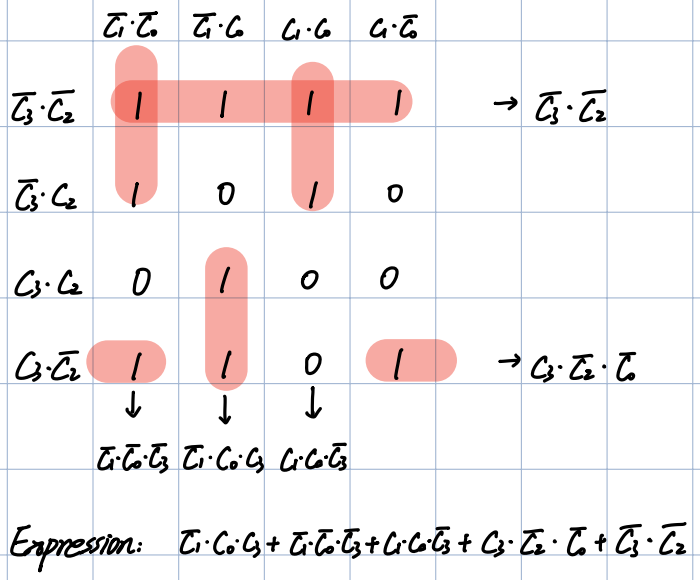
Passed: 16 Failed: 0

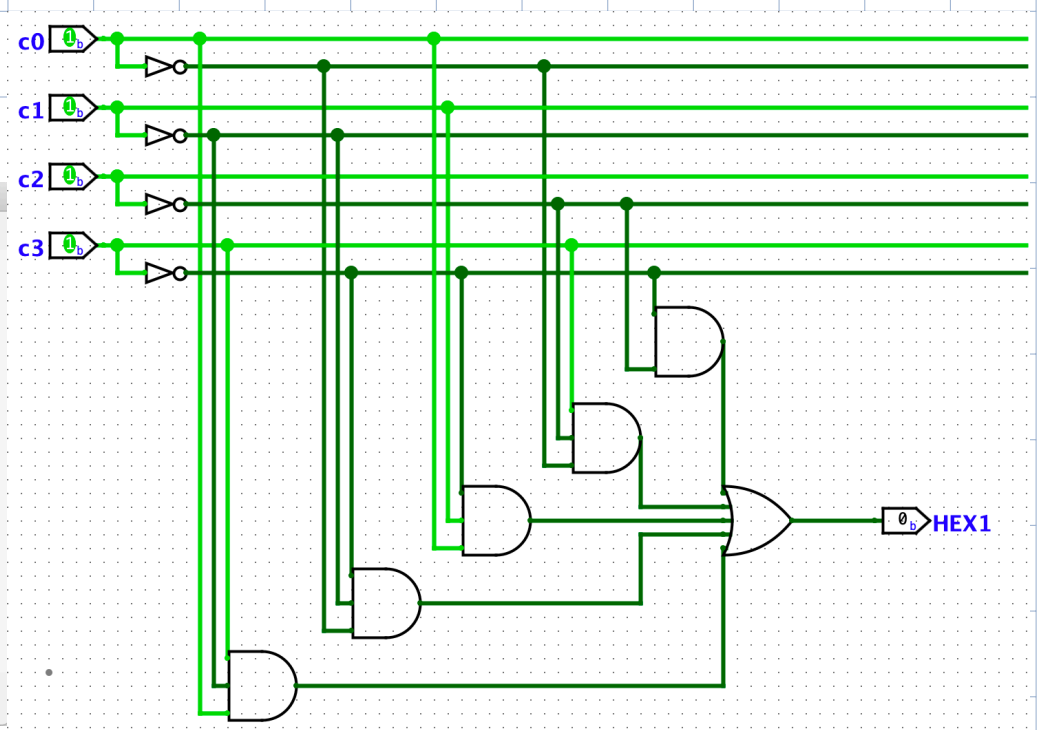
Status	c3	c2	c1	c0	HEX0
pass	0	0	0	0	1
pass	0	0	0	1	0
pass	0	0	1	0	1
pass	0	0	1	1	1
pass	0	1	0	0	0
pass	0	1	0	1	1
pass	0	1	1	0	1
pass	0	1	1	1	1
pass	1	0	0	0	1
pass	1	0	0	1	1
pass	1	0	1	0	1
pass	1	0	1	1	0
pass	1	1	0	0	1
pass	1	1	0	1	0
pass	1	1	1	0	1
pass	1	1	1	1	1

r Run Stop Reset Close Window

Segment 1

Segment 1					
Character	c3	c2	c1	c0	HEX1
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
A	1	0	1	0	1
b	1	0	1	1	0
C	1	1	0	0	0
d	1	1	0	1	1
E	1	1	1	0	0
F	1	1	1	1	0





Test Vector Segment1 of Lab2_Pat3

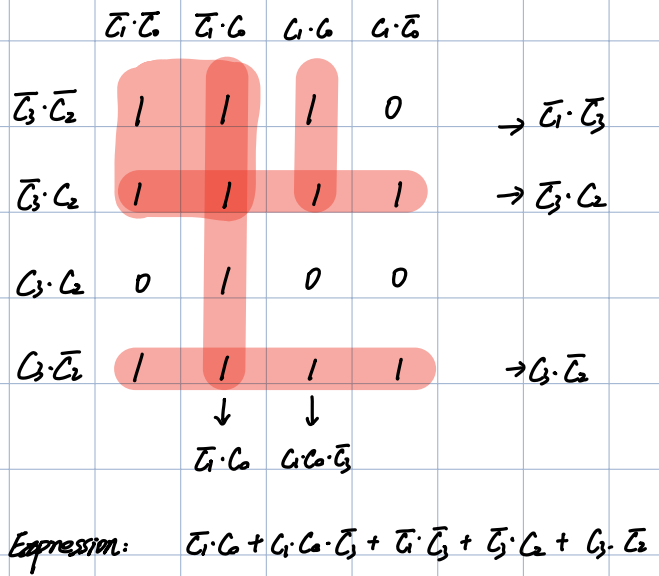
Passed: 16 Failed: 0

Status	c3	c2	c1	c0	HEX1
pass	0	0	0	0	1
pass	0	0	0	1	1
pass	0	0	1	0	1
pass	0	0	1	1	1
pass	0	1	0	0	1
pass	0	1	0	1	0
pass	0	1	1	0	0
pass	0	1	1	1	1
pass	1	0	0	0	1
pass	1	0	0	1	1
pass	1	0	1	0	1
pass	1	0	1	1	0
pass	1	1	0	0	0
pass	1	1	0	1	1
pass	1	1	1	0	0
pass	1	1	1	1	0

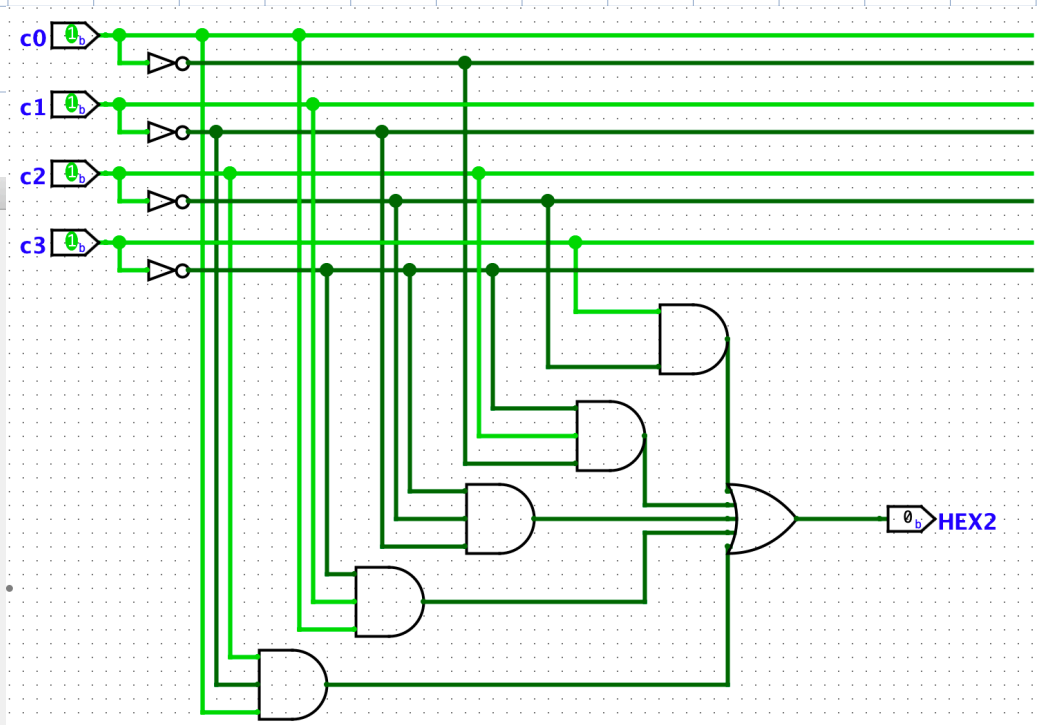
Run Stop Reset Close Window

Segment 2

Segment 2					
Character	c3	c2	c1	c0	HEX2
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
A	1	0	1	0	1
b	1	0	1	1	1
C	1	1	0	0	0
d	1	1	0	1	1
E	1	1	1	0	0
F	1	1	1	1	0



Expression: $\bar{C_1}\cdot C_0 + C_1\cdot C_0\cdot\bar{C_3} + \bar{C_1}\cdot\bar{C_3} + \bar{C_3}\cdot C_2 + C_3\cdot\bar{C_2}$



Test Vector Segment2 of Lab2_Pat3

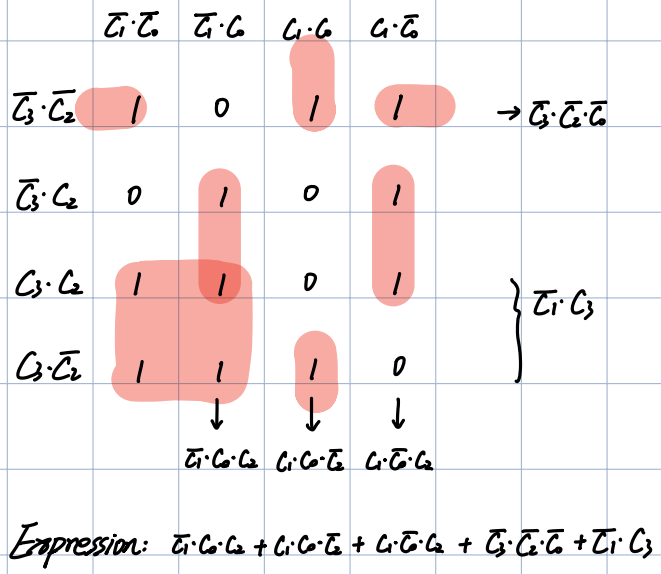
Passed: 16 Failed: 0

Status	c3	c2	c1	c0	HEX2
pass	0	0	0	0	1
pass	0	0	0	1	1
pass	0	0	1	0	0
pass	0	0	1	1	1
pass	0	1	0	0	1
pass	0	1	0	1	1
pass	0	1	1	0	1
pass	0	1	1	1	1
pass	1	0	0	0	1
pass	1	0	0	1	1
pass	1	0	1	0	1
pass	1	0	1	1	1
pass	1	1	0	0	0
pass	1	1	0	1	1
pass	1	1	1	0	0
pass	1	1	1	1	0

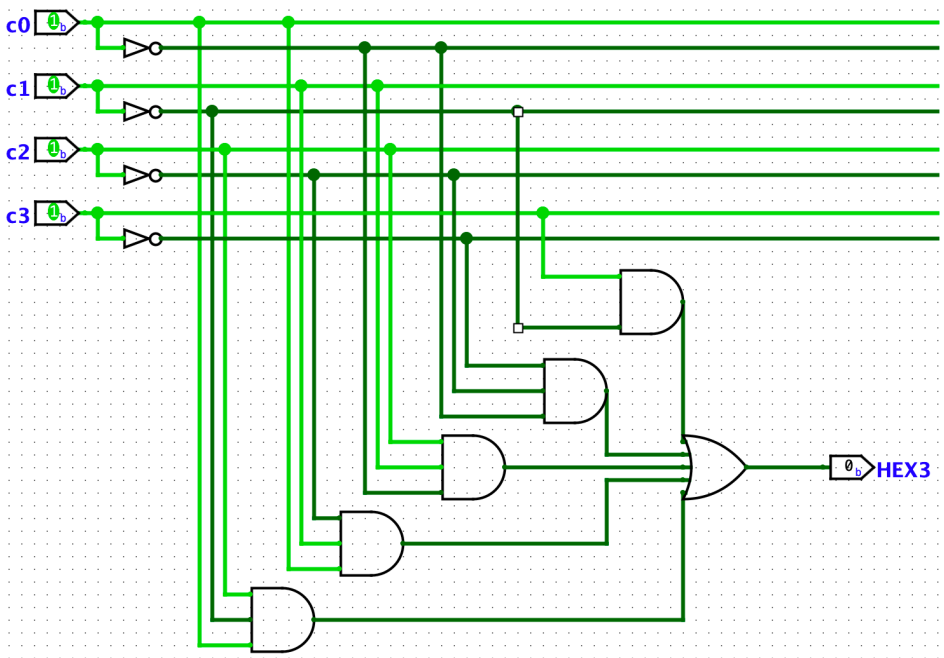
Run Stop Reset Close Window

Segment 3

Segment 3					
Character	c3	c2	c1	c0	HEX3
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	1
A	1	0	1	0	0
b	1	0	1	1	1
C	1	1	0	0	1
d	1	1	0	1	1
E	1	1	1	0	1
F	1	1	1	1	0



Expression: $\bar{c}_1 c_0 c_2 + c_1 c_0 \bar{c}_2 + c_1 \bar{c}_0 c_2 + \bar{c}_3\bar{c}_2\bar{c}_0 + \bar{c}_1 c_3$



Test Vector Segment3 of Lab2_Pat3

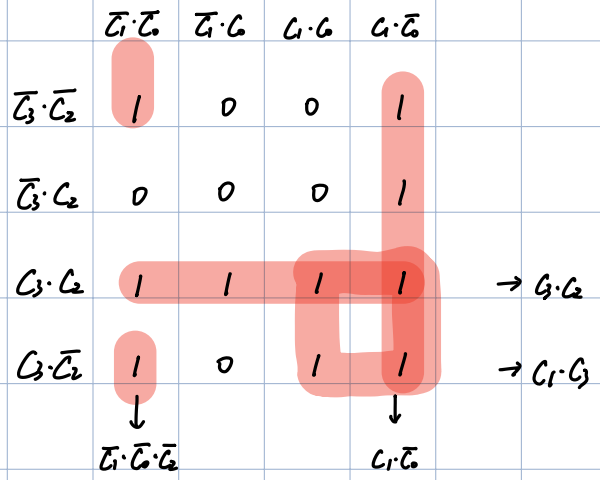
Passed: 16 Failed: 0

Status	c3	c2	c1	c0	HEX3
pass	0	0	0	0	1
pass	0	0	0	1	0
pass	0	0	1	0	1
pass	0	0	1	1	1
pass	0	1	0	0	0
pass	0	1	0	1	1
pass	0	1	1	0	1
pass	0	1	1	1	0
pass	1	0	0	0	1
pass	1	0	0	1	1
pass	1	0	1	0	0
pass	1	0	1	1	1
pass	1	1	0	0	1
pass	1	1	0	1	1
pass	1	1	1	0	1
pass	1	1	1	1	0

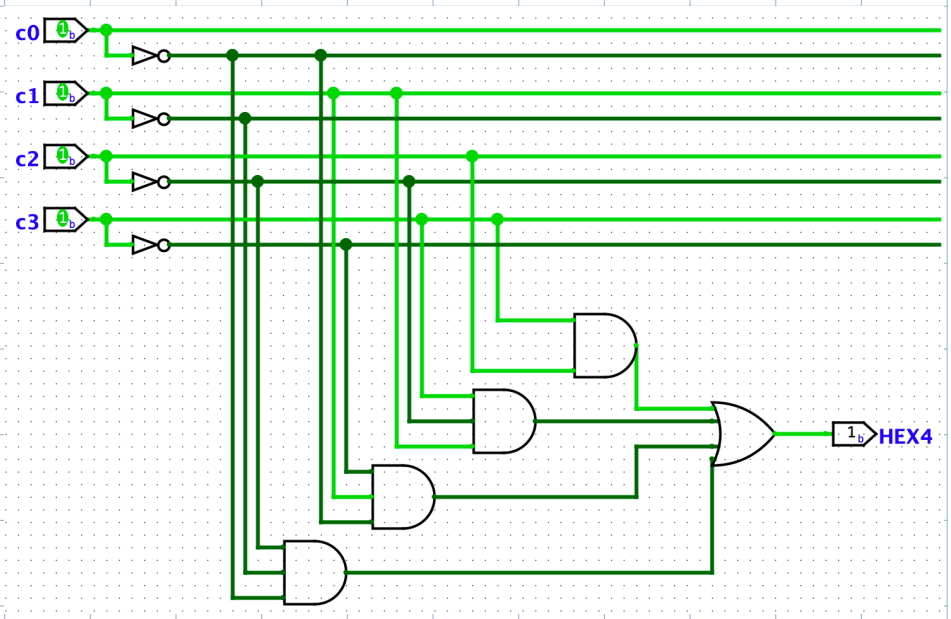
Run Stop Reset

Segment 4

Segment 4					
Character	c3	c2	c1	c0	HEX4
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	1
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	0
A	1	0	1	0	1
b	1	0	1	1	1
C	1	1	0	0	1
d	1	1	0	1	1
E	1	1	1	0	1
F	1	1	1	1	1



Expression: $\bar{c}_0\cdot\bar{c}_1\cdot\bar{c}_2 + \bar{c}_0\cdot c_1 + c_1\cdot c_3 + c_2\cdot c_3$



Test Vector Segment4 of Lab2_Pat3

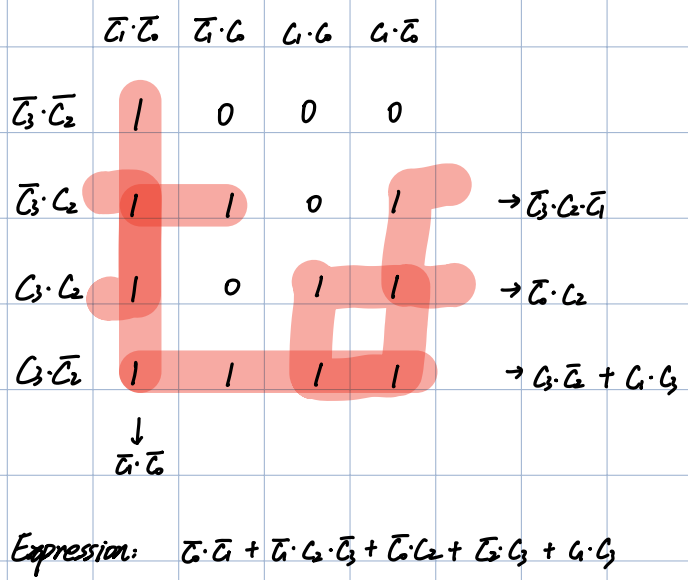
Passed: 16 Failed: 0

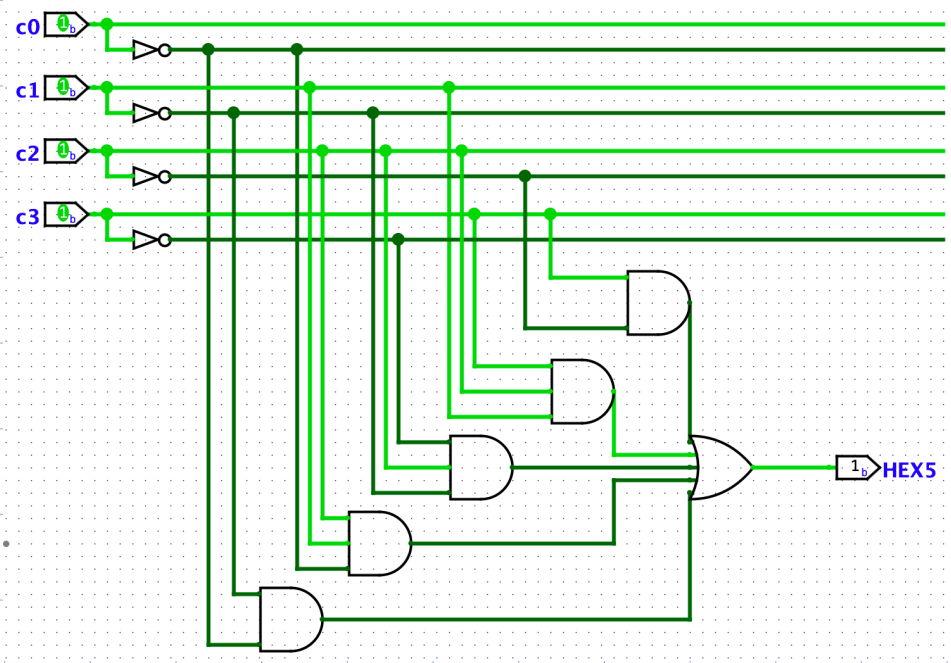
Status	c3	c2	c1	c0	HEX4
pass	0	0	0	0	1
pass	0	0	0	1	0
pass	0	0	1	0	1
pass	0	0	1	1	0
pass	0	1	0	0	0
pass	0	1	0	1	0
pass	0	1	1	0	1
pass	0	1	1	1	0
pass	1	0	0	0	1
pass	1	0	0	1	0
pass	1	0	1	0	1
pass	1	0	1	1	1
pass	1	1	0	0	1
pass	1	1	0	1	1
pass	1	1	1	0	1
pass	1	1	1	1	1

Run Stop Reset

Segment 5

Segment 5					
Character	c3	c2	c1	c0	HEX5
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	1
A	1	0	1	0	1
b	1	0	1	1	1
C	1	1	0	0	1
d	1	1	0	1	0
E	1	1	1	0	1
F	1	1	1	1	1





Test Vector Segment5 of Lab2_Pat3

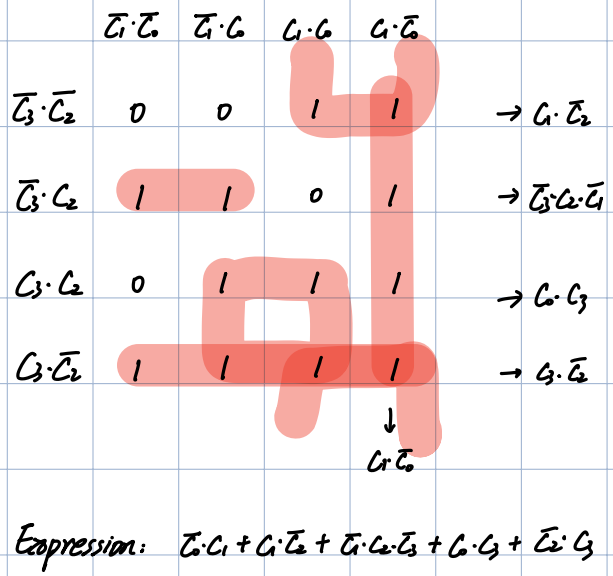
Passed: 16 Failed: 0

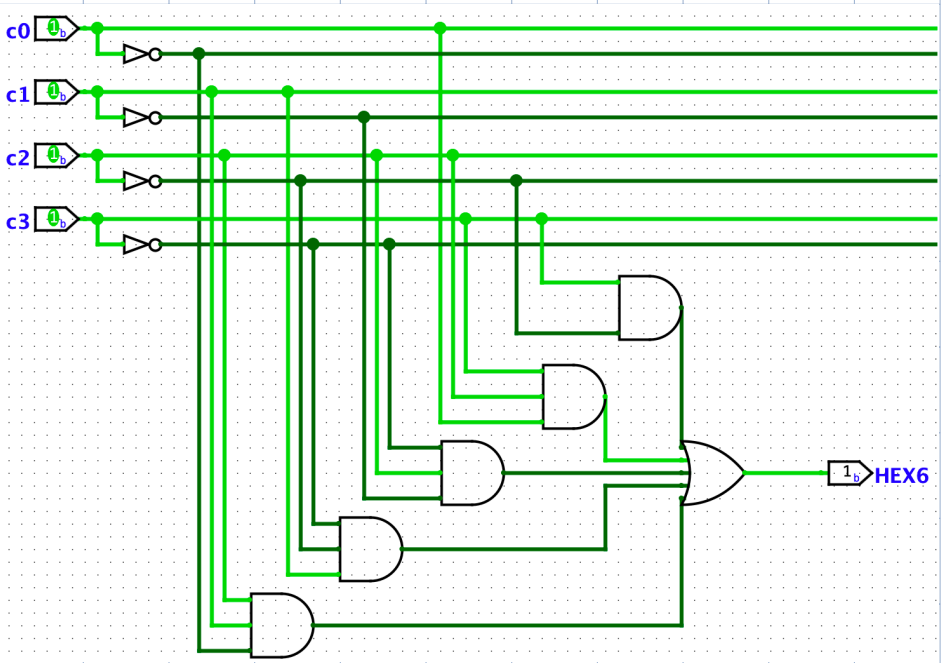
Status	c3	c2	c1	c0	HEX5
pass	0	0	0	0	1
pass	0	0	0	1	0
pass	0	0	1	0	0
pass	0	0	1	1	0
pass	0	1	0	0	1
pass	0	1	0	1	1
pass	0	1	1	0	1
pass	0	1	1	1	0
pass	1	0	0	0	1
pass	1	0	0	1	1
pass	1	0	1	0	1
pass	1	0	1	1	1
pass	1	1	0	0	1
pass	1	1	0	1	0
pass	1	1	1	0	1
pass	1	1	1	1	1

Run Stop Reset

Segment 6

Segment 6					
Character	c3	c2	c1	c0	HEX6
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	1
A	1	0	1	0	1
b	1	0	1	1	1
C	1	1	0	0	0
d	1	1	0	1	1
E	1	1	1	0	1
F	1	1	1	1	1





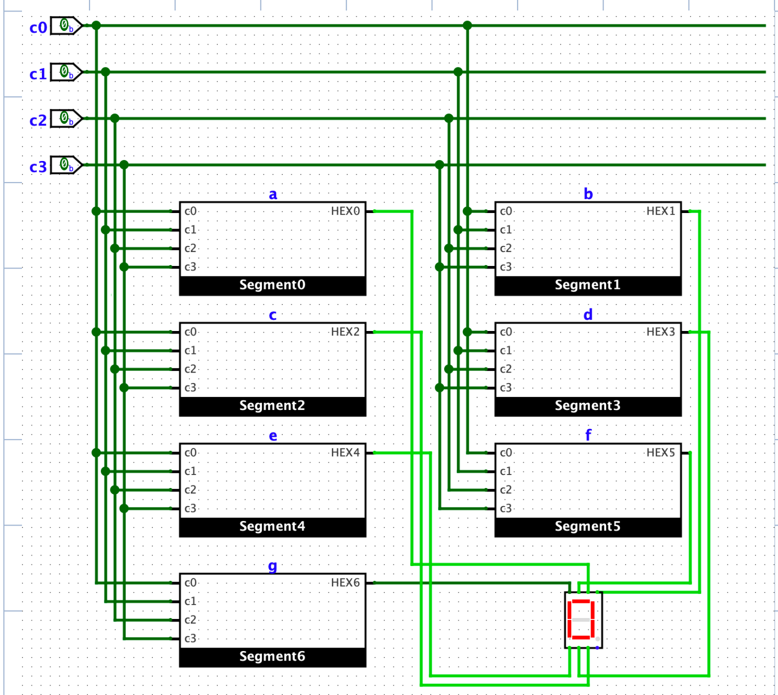
Test Vector Segment6 of Lab2_Pat3

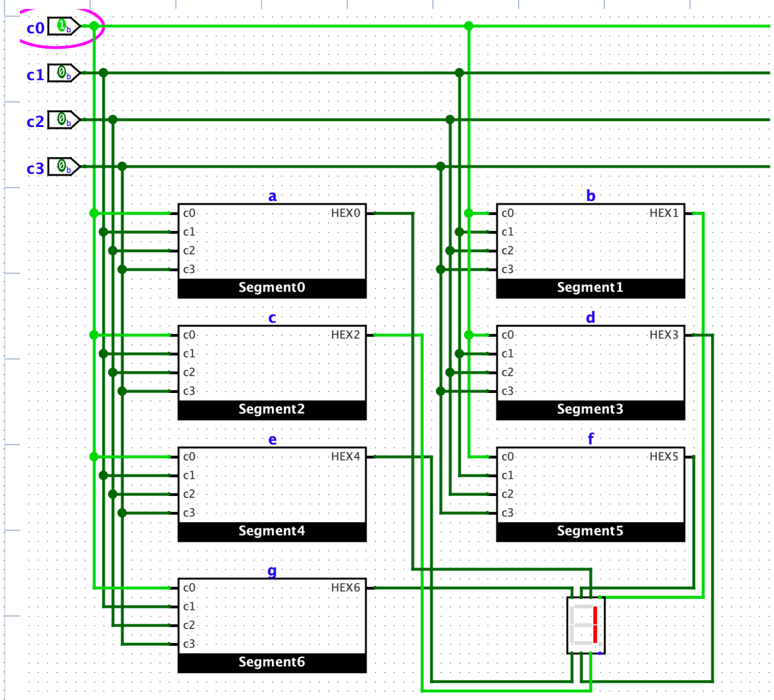
Passed: 16 Failed: 0

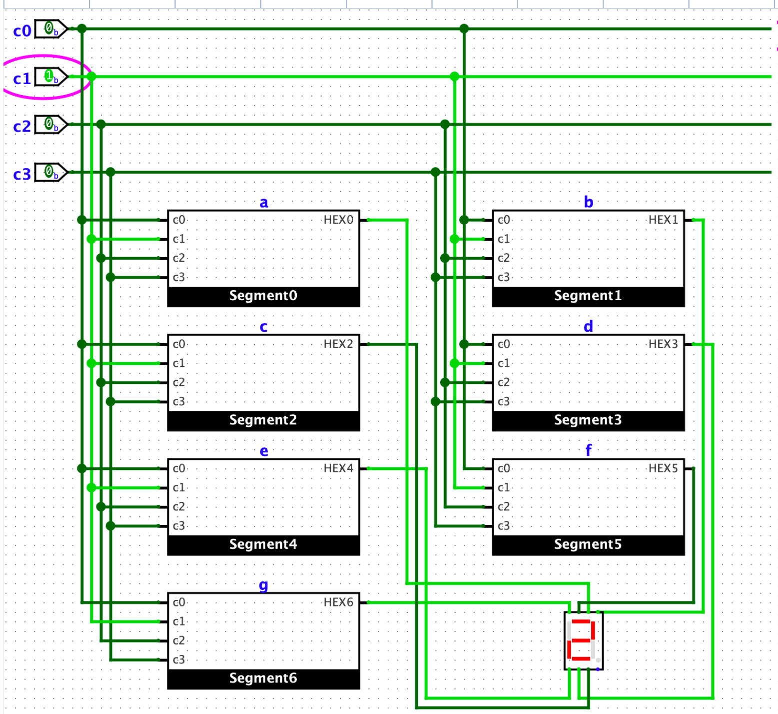
Status	c3	c2	c1	c0	HEX6
pass	0	0	0	0	0
pass	0	0	0	1	0
pass	0	0	1	0	1
pass	0	0	1	1	1
pass	0	1	0	0	1
pass	0	1	0	1	1
pass	0	1	1	0	1
pass	0	1	1	1	0
pass	1	0	0	0	1
pass	1	0	0	1	1
pass	1	0	1	0	1
pass	1	0	1	1	1
pass	1	1	0	0	0
pass	1	1	0	1	1
pass	1	1	1	0	1
pass	1	1	1	1	1

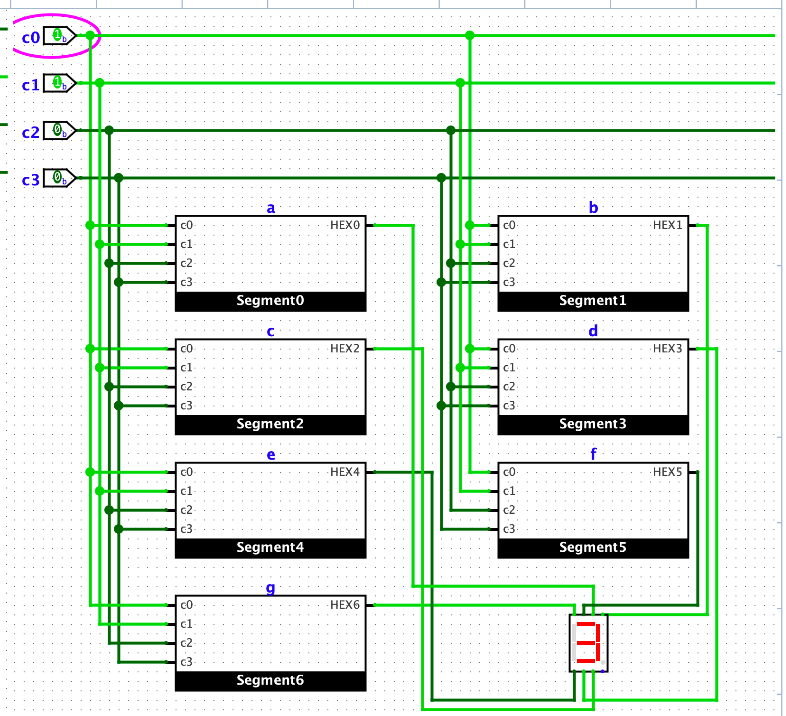
Run Stop Reset

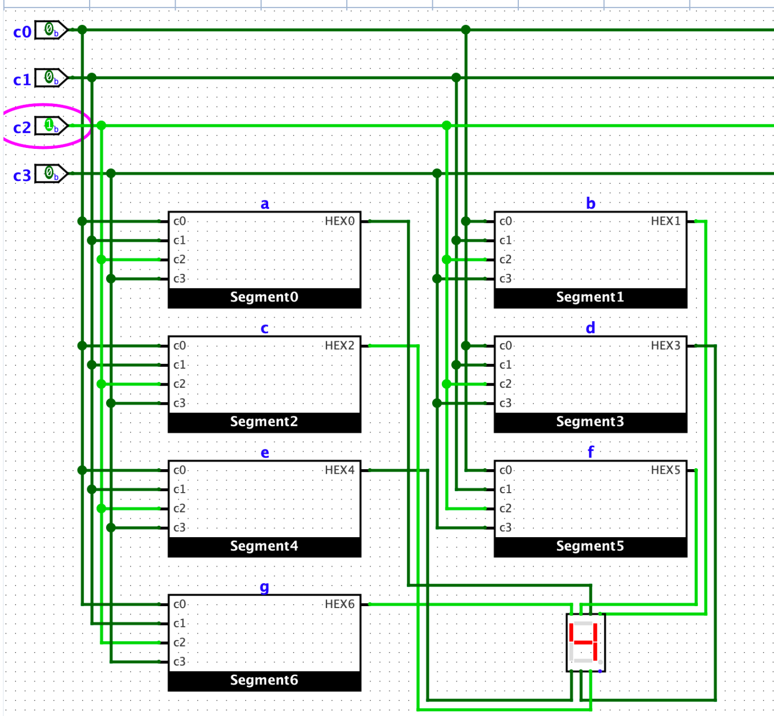
Test 7-Segment Display by using "Poke"

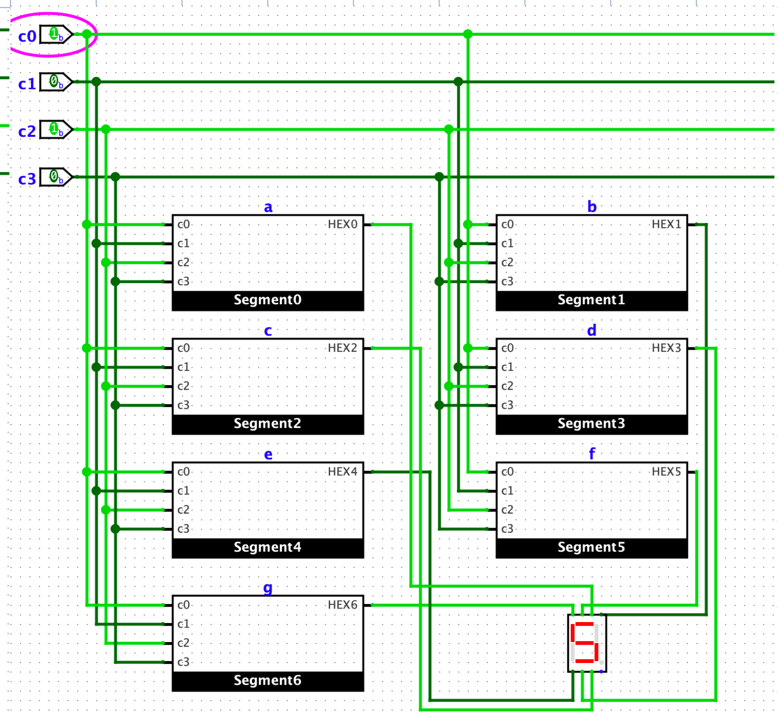









c0
c1
c2
c3
a
b
c
d
e
f
g
HEX0
HEX1
HEX2
HEX3
HEX4
HEX5
HEX6
Segment0
Segment1
Segment2
Segment3
Segment4
Segment5
Segment6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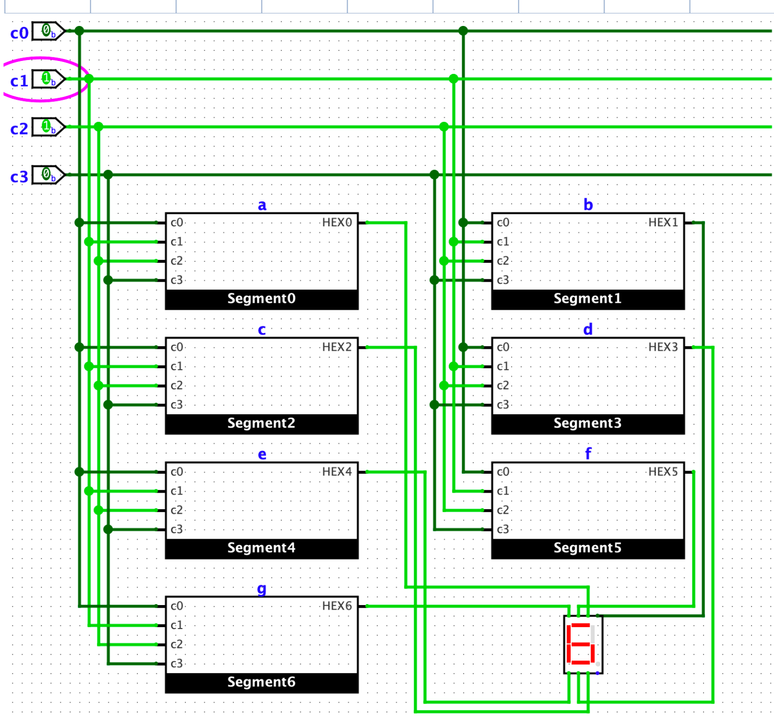
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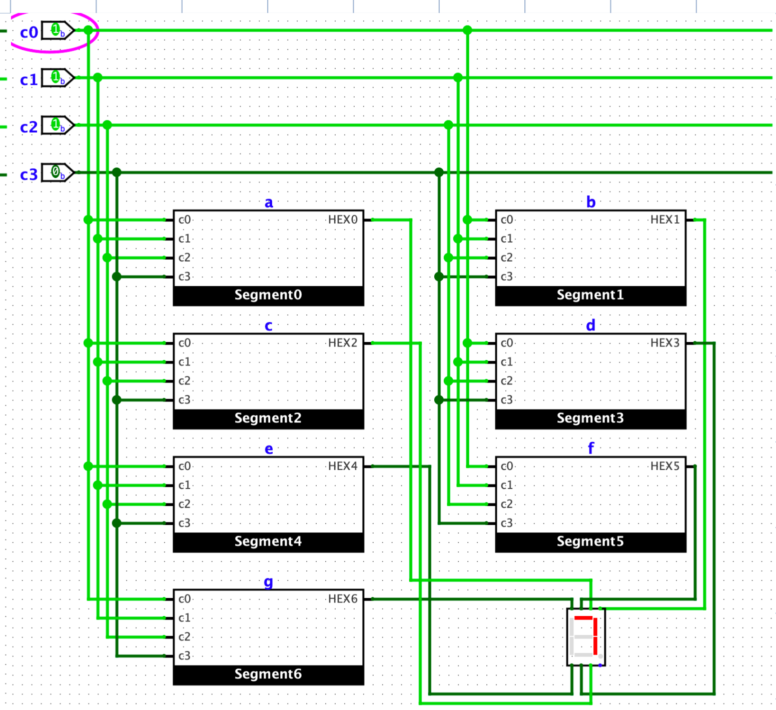
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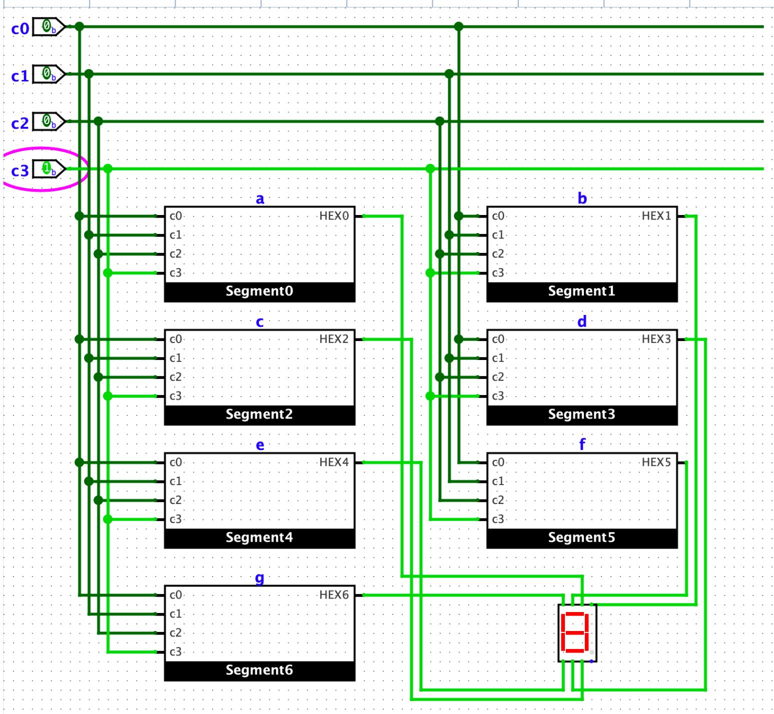
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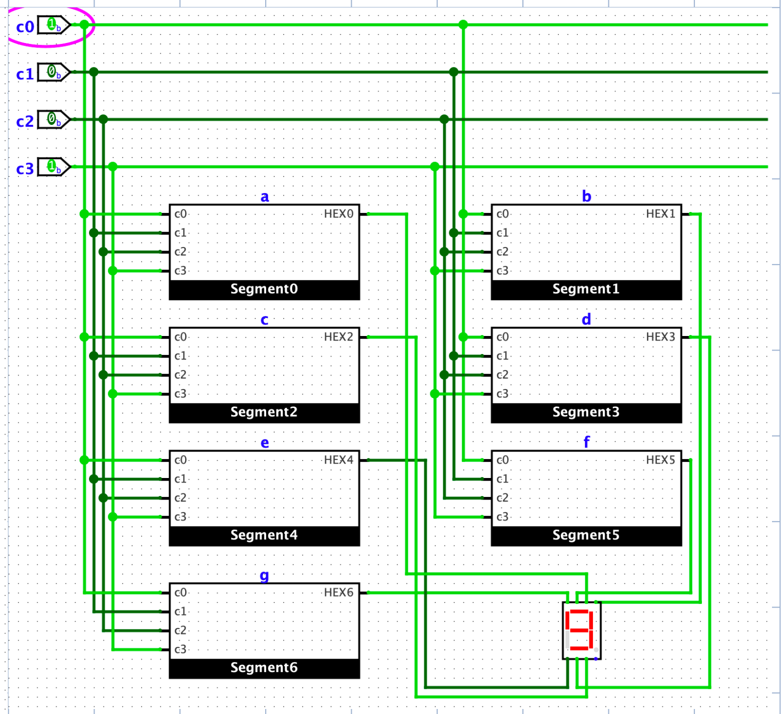
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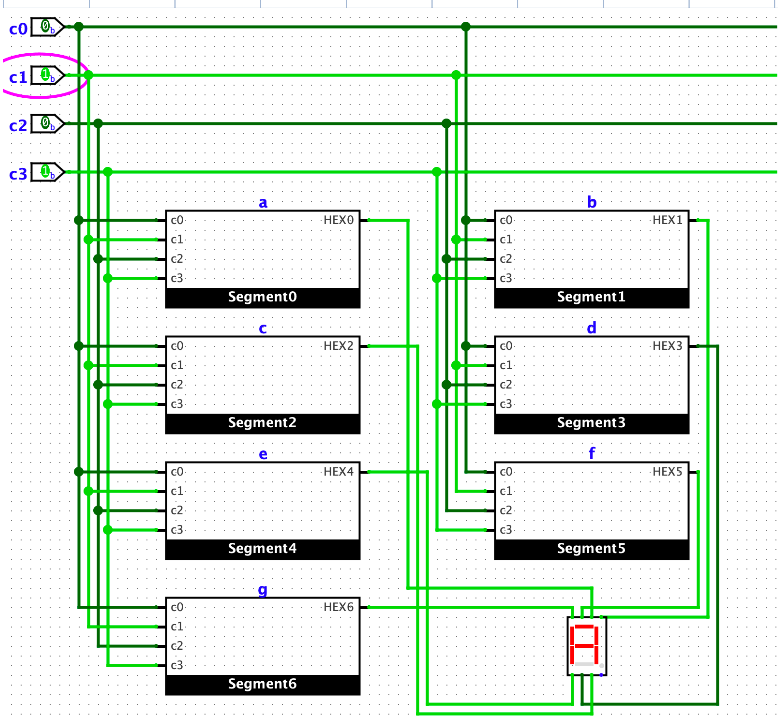
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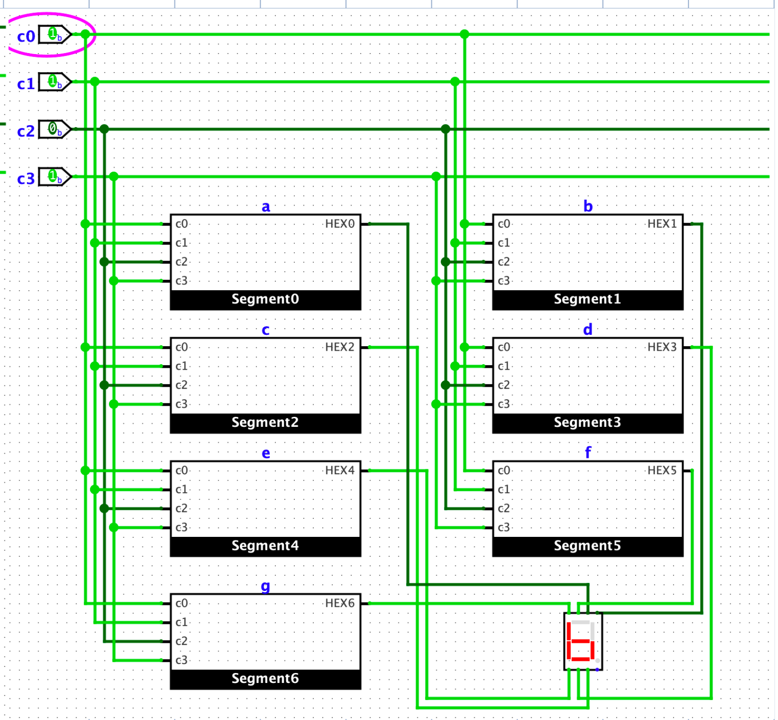
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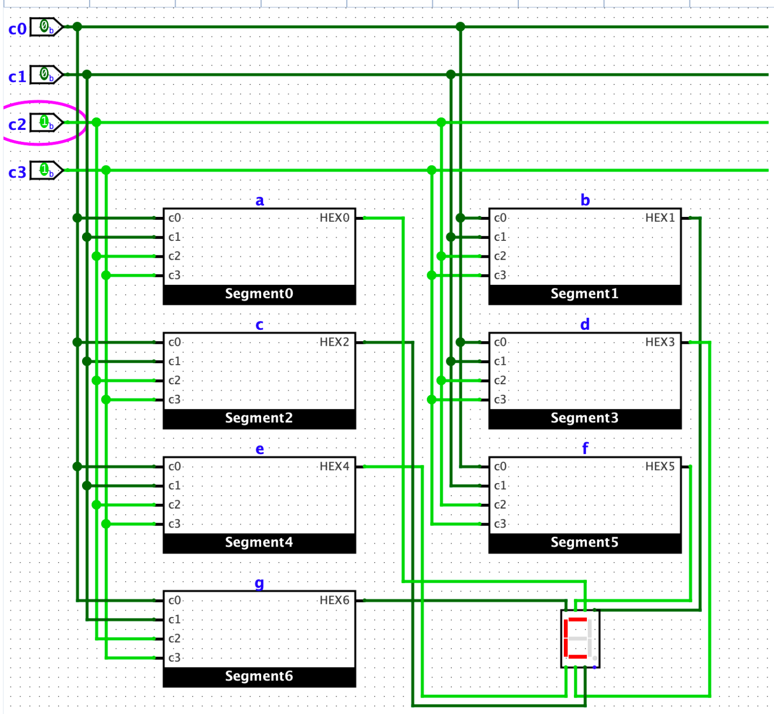
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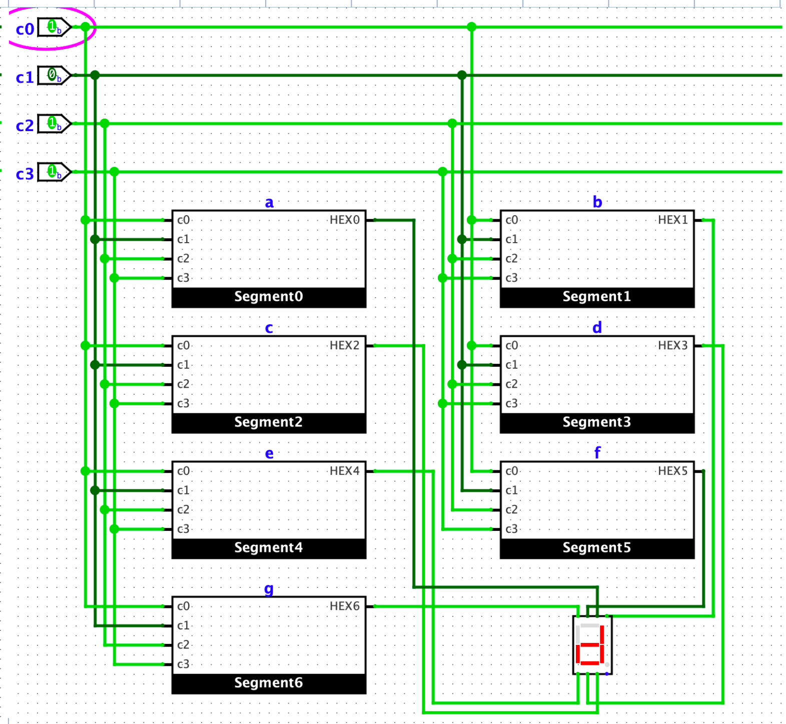
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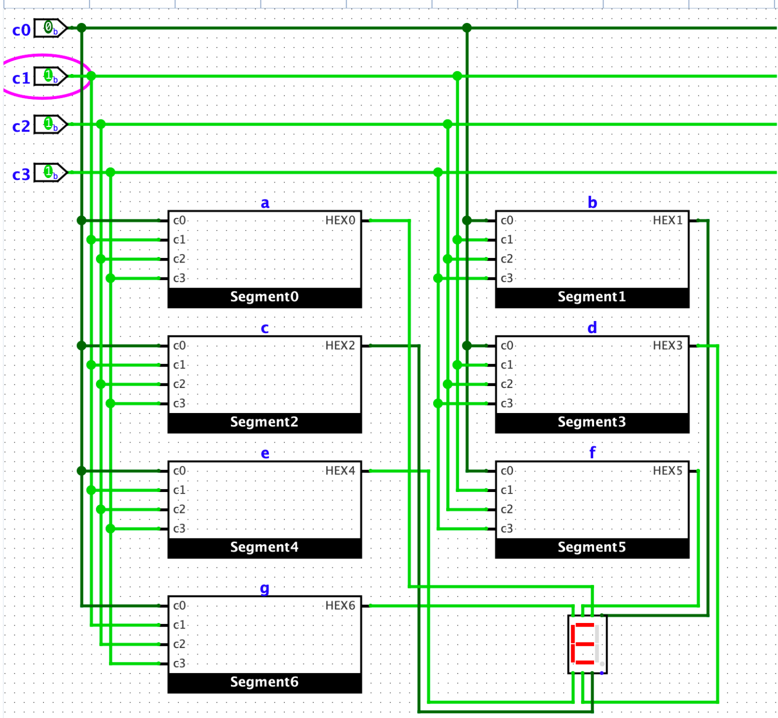
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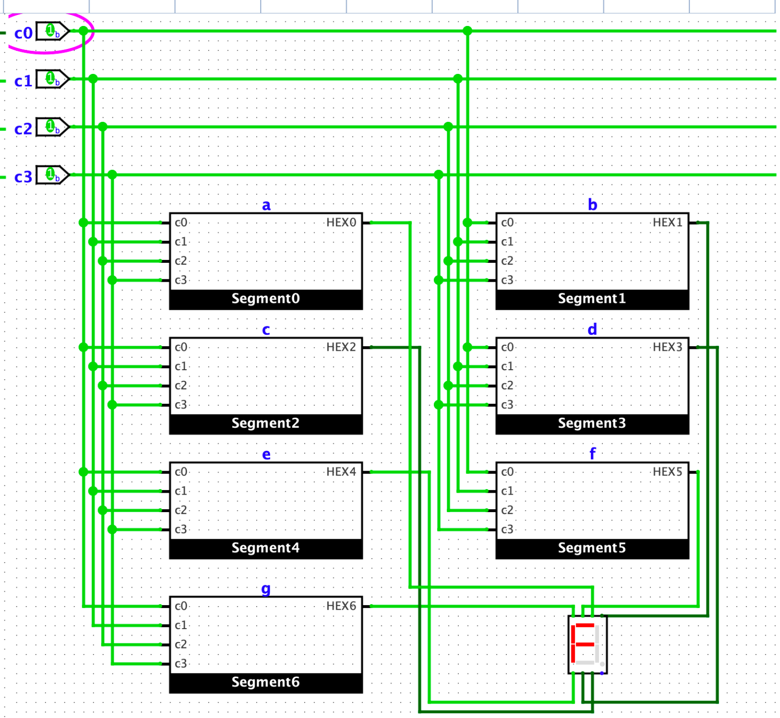
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Segment0
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4. Map your Logisim design to the inputs of the DE1-SoC board. Connect the $c_3c_2c_1c_0$ inputs to switches SW_{3-0} and test that changing the values on these switches creates the appropriate change in the seven segment display.