TCS3400

Color Light-to-Digital Converter

General Description

The TCS3400 device provides color and IR (red, green, blue, clear and IR) light sensing. The color sensing provides for improved accuracy lux and color temperature measurements typically used to adjust the backlight intensity and correct the display color gamut. Additionally it can be used for light source type detection as it reports the IR content of the light.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TCS3400, Color Light-to-Digital Converter are listed below:

Figure 1:
Added Value of Using TCS3400

Benefits	Features
• Single Device Integrated Optical Solution	• RGBC and ALS Support • Power Management Features
• Color Temperature and Ambient Light Sensing	• Programmable Gain & Integration Time • 1000000:1 Dynamic Range
• Equal Response to 360 degree Incident Light	• Circular Segmented RGBC Photodiode
• Ideal for Operation Behind Dark Glass	• Very High Sensitivity
• Light Source Detection	• RGBC + IR sensor

Applications

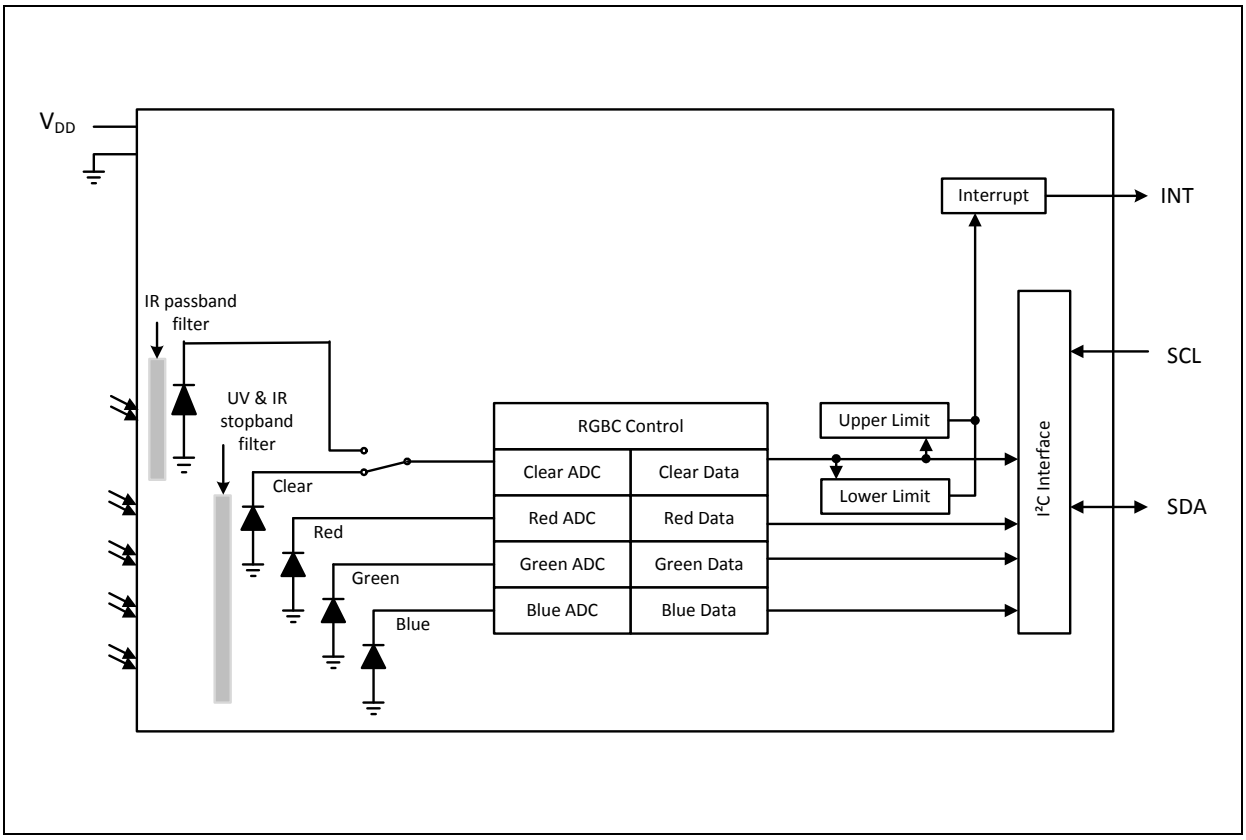
The TCS3400 applications include:

- Ambient light sensing
- Color temperature sensing
- Industrial process control
- Medical diagnostics

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TCS3400 Block Diagram



Pin Assignment

The TCS3400 pin assignments are described below.

Figure 3:
Pin Diagram

Pin Diagram (Top View):
Package FN Dual Flat No-Lead.
Package Drawing is not to scale.

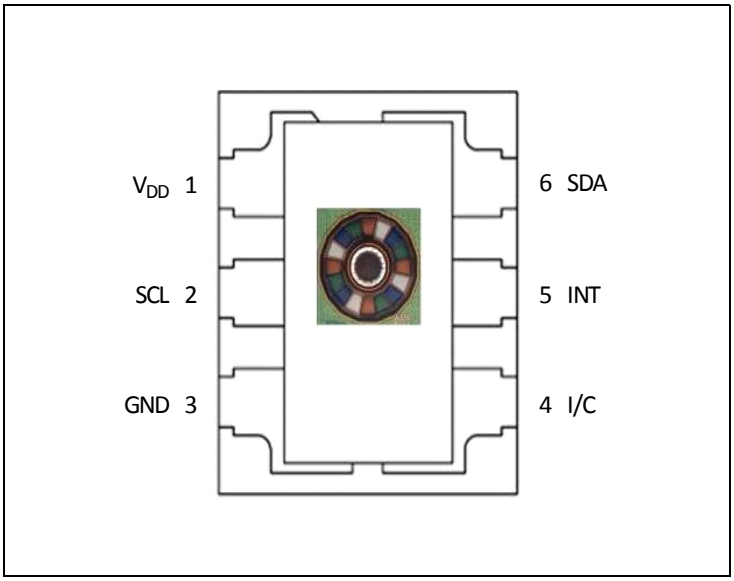


Figure 4:
Pin Description

Pin Number	Pin Name	Description
1	V_{DD}	Supply voltage
2	SCL	I^2C serial clock input terminal
3	GND	Power supply ground. All voltages are referenced to GND.
4	I/C	Internal connection, connect to ground or leave floating.
5	INT	Interrupt — open drain output (active low)
6	SDA	I^2C serial data I/O terminal – open drain

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Supply voltage, V_{DD}		3.8	V	All voltages are with respect to GND
Input terminal voltage	-0.5	3.8	V	
Output terminal voltage	-0.5	3.8	V	
Output terminal current (SDA, INT)	-1	20	mA	
Storage temperature range, T_{STRG}	-40	85	°C	
Input current (latch up immunity) JEDEC JESD78D Nov 2011	CLASS 1			
Electrostatic discharge HBM S-001-2014	±2000		V	
Electrostatic discharge CDM JEDEC JESD22-C101F Oct 2013	±500		V	

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply voltage	2.7	3	3.6	V
T_A	Operating free-air temperature (1)	-40		70	°C

Note(s):

1. While the device is operational across the temperature range, functionality will vary with temperature. Specifications are stated at 25°C unless otherwise noted.

Figure 7:
Operating Characteristics, V_{DD}=3V, T_A=25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Supply current	Active		235	330	µA
		Wait state		60		
		Sleep state - no I^2C activity		1.0	10	
V_{OL}	INT, SDA output low voltage	3 mA sink current	0		0.4	V
		6 mA sink current	0		0.6	
I_{LEAK}	Leakage current, SDA, SCL, INT pins		-5		5	µA
V_{IH}	SCL, SDA input high voltage	TCS34001, TCS34005	0.7 V_{DD}			V
		TCS34003, TCS34007	1.26			
V_{IL}	SCL, SDA input low voltage	TCS34001, TCS34005			0.3 V_{DD}	V
		TCS34003, TCS34007			0.54	

Figure 8:
Optical Characteristics (Clear Channel), V_{DD} = 3V, T_A = 25°C, AGAIN = 16x, ATIME = 0xF6 (27.8ms)

Parameter	Test Conditions	Min	Typ	Max	Unit
R_e Irradiance Responsivity (Clear Channel)	White LED, CCT = 2700K(1)	11.2	14.0	16.8	counts/ ($\mu W/cm^2$)
	Blue LED, λ_D = 465 nm(2)	9.5	11.8	14.2	
	Green LED, λ_D = 525 nm(3)	11.6	14.5	17.4	
	Red LED, λ_D = 615 nm(4)	13.6	17.0	20.4	

Note(s):

1. The white LED irradiance is supplied by a warm white light-emitting diode with a nominal color temperature of 2700K.
2. The 465 nm input irradiance is supplied by an InGaN light-emitting diode with the following typical characteristics: dominant wavelength λ_D = 465 nm, spectral halfwidth $\Delta\lambda$½ = 22 nm.
3. The 525 nm input irradiance is supplied by an InGaN light-emitting diode with the following typical characteristics: dominant wavelength λ_D = 525 nm, spectral halfwidth $\Delta\lambda$½ = 35 nm.
4. The 615 nm input irradiance is supplied by an AlInGaP light-emitting diode with the following typical characteristics: dominant wavelength λ_D = 615 nm, spectral halfwidth $\Delta\lambda$½ = 15 nm.

Figure 9:
Optical Characteristics (IR Channel), VDD = 3V, T_A = 25°C, AGAIN = 16x, ATIME = 0xF6 (27.8ms)

Parameter	Test Condition	Min	Typ	Max	Unit
R_e Irradiance Responsivity (IR Channel)	λ_P = 850 nm(1)	10.0	13.3	16.6	counts/ ($\mu W/cm^2$)

Note(s):

1. The 850 nm input irradiance is supplied by an AlGaAs light-emitting diode with the following characteristics: peak wavelength λ_P = 850 nm, spectral halfwidth $\Delta\lambda$1/2 = 42 nm.

Figure 10:
Optical Characteristics, V_{DD}=3V, T_A=25°C

Parameter	Test Conditions	Red / Clear Channel		Green / Clear Channel		Blue / Clear Channel		IR / Clear Channel	
		Min	Max	Min	Max	Min	Max	Min	Max
Color ADC count value ratio: Color / Clear	λ_D = 465 nm (1)	0%	13%	10%	38%	70%	91%		
	λ_D = 525 nm (2)	3%	22%	59%	86%	10%	40%		
	λ_D = 615 nm (3)	80%	110%	0%	15%	3%	26%	0%	5%
	λ_P = 850 nm (4)							667%	

Note(s):

1. The 465 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 465 nm, spectral halfwidth $\Delta\lambda$½ = 22 nm.
2. The 525 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 525 nm, spectral halfwidth $\Delta\lambda$½ = 35 nm.
3. The 615 nm input irradiance is supplied by a AlInGaP light-emitting diode with the following characteristics: dominant wavelength λ_D = 615 nm, spectral halfwidth $\Delta\lambda$½ = 15 nm.
4. The 850 nm input irradiance is supplied by an AlGaAs light-emitting diode with the following characteristics: peak wavelength λ_P = 850 nm, spectral halfwidth $\Delta\lambda$1/2 = 42 nm.

Figure 11:
RGBC Characteristics, V_{DD} = 3V, T_A = 25°C, AGAIN = 16x, AEN = 1 (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Dark ADC count value (Clear and RGB Channels)	E_e = 0, AGAIN = 64x, ATIME = 0xB8 (200ms)	0	1	4	counts
		0		2	counts (1)
Dark ADC count value (IR Channel)		0	1	6	counts
		0		4	counts (1)
Integration time step size		2.65	2.78	2.93	ms
Number of integration steps		1		256	steps
ADC count value	ATIME = 0xFF (2.78ms) to 0xC1 (175ms) (1 to 63 steps)	0		1024	counts/ step
	ATIME = 0xC0 (178ms) to 0x00 (712ms) (64 to 256 steps)	0		65535	counts
Gain scaling, relative to 16× gain setting	1x: AGAIN = 00	0.936	0.985	1.065	×
	4x: AGAIN = 01	3.66	3.85	4.16	
	16x: AGAIN = 10		16.0		
	64x: AGAIN = 11	59.6	62.7	67.8	

Note(s):

1. Based on typical 3-sigma distribution. Not 100% tested.

Figure 12:
Wait Characteristics, V_{DD} = 3V, T_A = 25°C, WEN = 1 (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Wait step size	WTIME = 0xFF		2.78		ms

Timing Characteristics

The timing characteristics of TCS3400 are given below.

Figure 13:
AC Electrical Characteristics, V_{DD} = 3V, T_A = 25°C (unless otherwise noted)

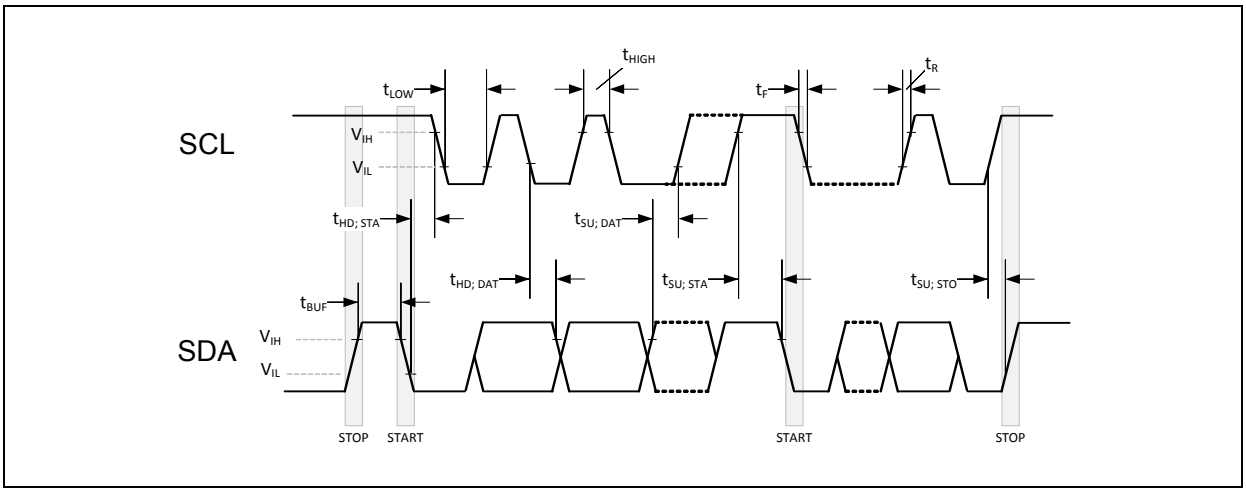
Parameter(1)	Conditions	Min	Max	Unit
f_{SCL}	Clock frequency (I^2C only)	0	400	kHz
t_{BUF}	Bus free time between start and stop condition	1.3		µs
$t_{HD;STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6		µs
$t_{SU;STA}$	Repeated start condition setup time	0.6		µs
$t_{SU;STO}$	Stop condition setup time	0.6		µs
$t_{HD;DAT}$	Data hold time	60		ns
$t_{SU;DAT}$	Data setup time	100		ns
t_{LOW}	SCL clock low period	1.3		µs
t_{HIGH}	SCL clock high period	0.6		µs
t_F	Clock/data fall time		300	ns
t_R	Clock/data rise time		300	ns
C_i	Input pin capacitance		10	pF

Note(s):

1. Specified by design and characterization; not production tested.

Timing Diagram

Figure 14:
Parameter Measurement Information



Typical Operating Characteristics

Figure 15:
Spectral Responsivity

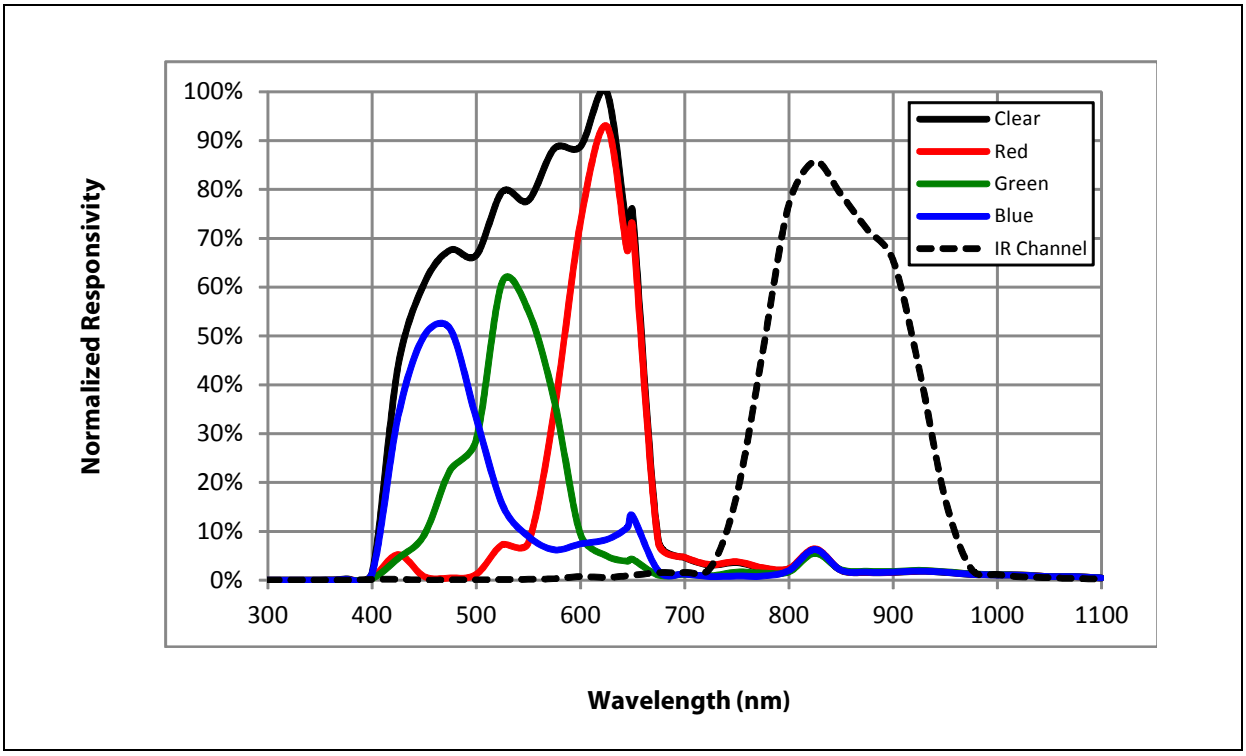


Figure 16:
Normalized Responsivity vs. Angular Displacement

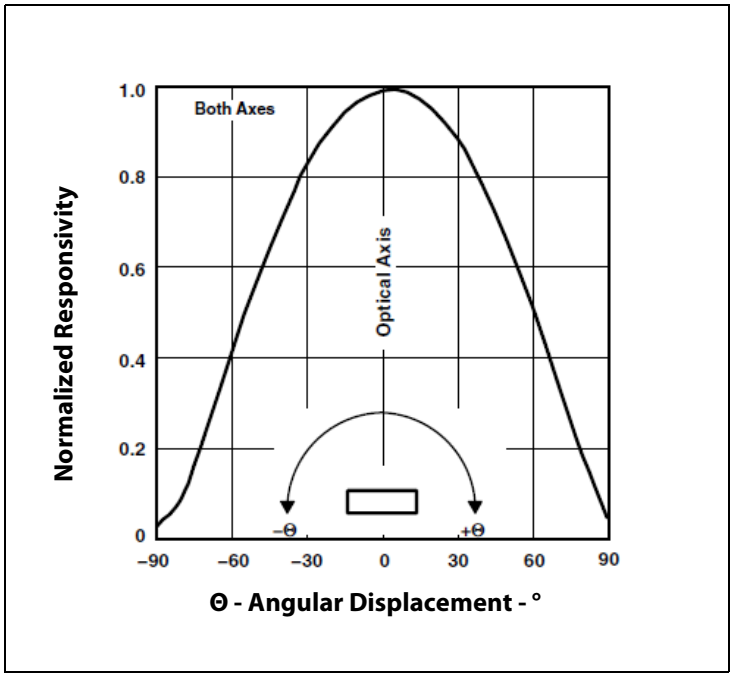


Figure 17:
Responsivity Temperature Coefficient

Wavelength	Temperature Coefficient
400 – 670nm	250 ppm/°C
850nm	2500 ppm/°C
950nm	5500 ppm/°C

Functional Description

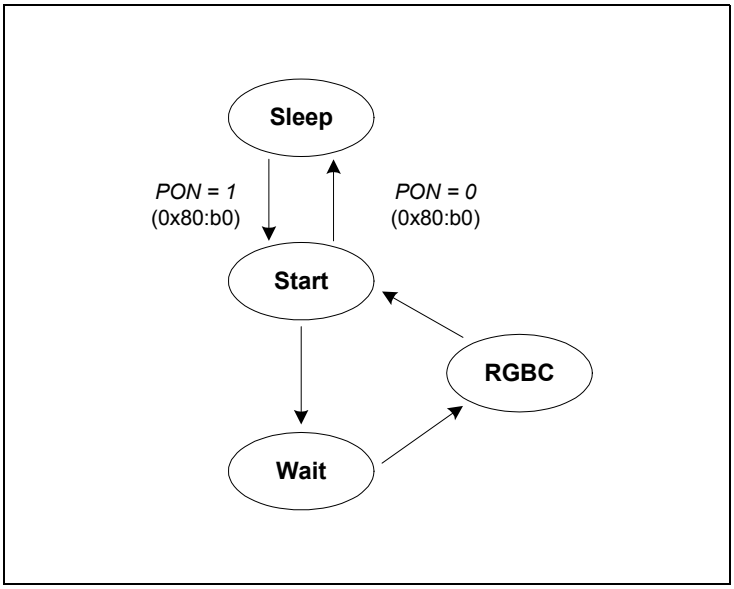
The TCS3400 device provides ambient light sensing and color temperature sensing. The internal state machine manages the operation of the device. It controls the ALS functionality and power down modes. Average power consumption is managed via control of variable endurance low power wait cycles.

The interrupt feature improves system efficiency by eliminating the need to poll the sensor. Two interrupt sources (ALS, ALS saturation) can activate the open drain output pin. Each interrupt source is enabled independently. ALS interrupts appear when upper or lower thresholds are exceeded for a consecutive number of sample readings.

The advanced digital color light sensor portion of the TCS3400 contains a segmented circular photodiode array used for color measurements. This architecture provides stable color sensing independent of the incident angle of light. Four integrating analog-to-digital converters (ADCs) integrate light energy from photodiodes simultaneously.

Communication with the device is accomplished through a fast (up to 400 kHz) two wire I^2C serial bus for easy connection to a microcontroller or embedded controller. The device typically draws only 235µA in color operation and 1uA during power down.

Figure 18:
Simplified ALS State Machine



Register Description

The device is controlled and monitored by registers accessed through the I^2C serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in the figure below.

Figure 19:
Register Map

Address	Register Name	R/W	Register Function	Reset Value
0x80	ENABLE	R/W	Enables states and interrupts	0x00
0x81	ATIME	R/W	RGBC integration time	0xFF
0x83	WTIME	R/W	Wait time	0xFF
0x84	AILTL	R/W	Clear interrupt low threshold low byte	0x00
0x85	AILTH	R/W	Clear interrupt low threshold high byte	0x00
0x86	AIHTL	R/W	Clear interrupt high threshold low byte	0x00
0x87	AIHTH	R/W	Clear interrupt high threshold high byte	0x00
0x8C	PERS	R/W	Interrupt persistence filter	0x00
0x8D	CONFIG	R/W	Configuration	0x40
0x8F	CONTROL	R/W	Gain control register	0x00
0x90	AUX	R/W	Auxiliary control register	0x00
0x91	REVID	R	Revision ID	Rev
0x92	ID	R	Device ID	ID
0x93	STATUS	R	Device status	0x00
0x94	CDATAL	R	Clear / IR channel low data register	0x00
0x95	CDATAH	R	Clear / IR channel high data register	0x00
0x96	RDATAL	R	Red ADC low data register	0x00
0x97	RDATAH	R	Red ADC high data register	0x00
0x98	GDATAL	R	Green ADC low data register	0x00
0x99	GDATAH	R	Green ADC high data register	0x00

Address	Register Name	R/W	Register Function	Reset Value
0x9A	BDATAL	R	Blue ADC low data register	0x00
0x9B	BDATAH	R	Blue ADC high data register	0x00
0xC0	IR	R/W	Access IR Channel	0x00
0xE4	IFORCE	W	Force Interrupt	0x00
0xE6	CICLEAR	W	Clear channel interrupt clear	0x00
0xE7	AICLEAR	W	Clear all interrupts	0x00

Enable Register (ENABLE 0 x 80)

The Enable Register is used primarily to power the device ON/OFF, and enable functions and interrupts.

Figure 20:
Enable Register

7	6	5	4	3	2	1	0
Reserved	SAI	Reserved	AIEN	WEN	Reserved	AEN	PON

Field	Bits	Description
Reserved	7	**Reserved.** Write as 0.
SAI	6	**Sleep After Interrupt.** When asserted, the device will power down at the end of a RGBC cycle if an interrupt is generated.
Reserved	5	**Reserved.** Write as 0.
AIEN	4	**ALS Interrupt Enable.** When asserted permits ALS interrupts to be generated, subject to the persist filter.
WEN	3	**Wait Enable.** This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
Reserved	2	**Reserved.** Write as 0.
AEN	1	**ADC Enable.** This bit activates the four-channel (RGBC) ADC. Writing a 1 enables the ADC. Writing a 0 disables the ADC.
PON	0	**Power ON.** This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator and puts the part into a low power sleep mode. During reads and writes over the I^2C interface, this bit is temporarily overridden and the oscillator is enabled, independent of the state of PON.

RGBC Integration Time Register (ATIME 0x81)

The ATIME register controls the internal integration time of the RGBC channel ADCs. Upon power up, the RGBC time register is set to 0xFF.

The maximum (or saturation) count value can be calculated based upon the integration time cycles as follows:

*min [CYCLES * 1024, 65535]*

Figure 21:
RGBC Integration Time Register

Field	Bits	Description			
		Value	Cycles	Time	Max Count
ATIME	7:0	0xFF	1	2.78 ms	1024
		0xF6	10	27.8 ms	10240
		0xDB	37	103 ms	37888
		0xC0	64	178 ms	65535
		0x00	256	712 ms	65535

Wait Time Register (WTIME 0x83)

The WTIME controls the amount of time in a low power mode. It is set 2.78 ms increments unless the WLONG bit is asserted in which case the wait times are 12× longer. WTIME is programmed as a 2's complement number. Upon power up, the wait time register is set to 0xFF.

Figure 22:
Wait Time Register

Field	Bits	Description			
		Register Value	Wait Time	Time (WLONG=0)	Time (WLONG=1)
WTIME	7:0	0xFF	1	2.78 ms	0.03 s
		0xAB	85	236 ms	2.84 s
		0x00	256	712 ms	8.54 s

Note(s):

1. The wait time register should be configured before AEN is asserted.

Clear Channel Interrupt Threshold Register (0x84 - 0x87)

The Clear Channel Interrupt Threshold Registers provide 16 bit values to be used as the high and low thresholds for comparison to the 16 bit CDATA values. If AIEN (0x80:b4) is enabled and CDATA is not between AILT and AIHT for the number of consecutive samples specified in APERS (0x8C:b[3:0]) an interrupt is asserted on the interrupt pin.

Figure 23:
Clear Channel Interrupt Threshold Registers

Register	Address	Bits	Description
AILTL	0x84	7:0	Clear Channel low threshold lower byte
AILTH	0x85	7:0	Clear Channel low threshold upper byte
AIHTL	0x86	7:0	Clear Channel high threshold lower byte
AIHTH	0x87	7:0	Clear Channel high threshold upper byte

Interrupt Register (0x8C)

The Interrupt Register controls the interrupt capabilities of the device.

Figure 24:
Interrupt Register

7	6	5	4	3	2	1	0
Reserved				APERS			

Field	Bits	Description	
Reserved	7:4	**Reserved.** Write as 0.	
APERS	3:0	**Clear Interrupt Persistence.** Controls rate of Clear channel interrupt to the host processor.	
		Field Value	**Persistence**
		0000	Every RGBC cycle generates an interrupt
		0001	Any value outside of threshold range
		0010	2 consecutive values out of range
		0011	3 consecutive values out of range
		0100	5 consecutive values out of range
		0101	10 consecutive values out of range
		0110	15 consecutive values out of range
		0111	20 consecutive values out of range
		1000	25 consecutive values out of range
		1001	30 consecutive values out of range
		1010	35 consecutive values out of range
		1011	40 consecutive values out of range
		1100	45 consecutive values out of range
		1101	50 consecutive values out of range
		1110	55 consecutive values out of range
		1111	60 consecutive values out of range

Configuration Register (CONFIG 0x8D)

The CONFIG register sets the wait long time. The registers is set 0x40 at power up.

Figure 25:
Configuration Register

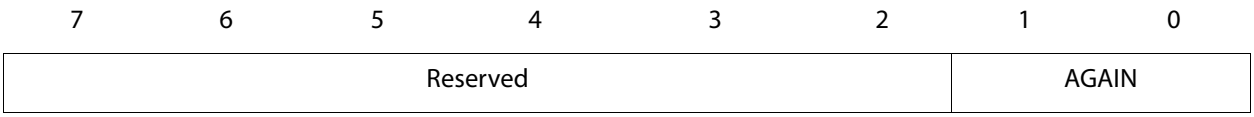
Field	Bits	Description
Reserved	7	**Reserved.** Write as 0.
Reserved (1)	6	**Reserved.** Write as 1.
Reserved	5:2	**Reserved.** Write all as 0.
WLONG	1	**Wait Long.** When asserted, the wait cycles are increased by a factor 12× from that programmed in the WTIME register.
Reserved	0	**Reserved.** Write as 0.

Note(s):

1. Bit 6 is reserved and has to be programmed = 1.

Control Register (CONTROL 0x8F)

Figure 26:
Control Register

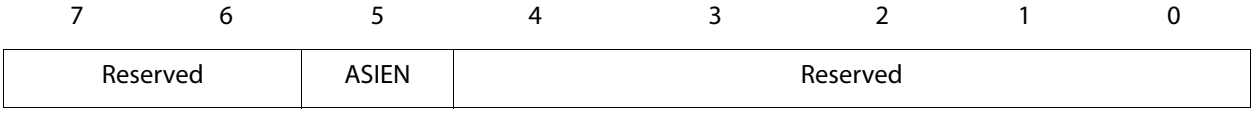


Field	Bits	Description	
Reserved	7:2	**Reserved.** Write all as 0.	
AGAIN	1:0	**RGBC Gain Control.**	
		FIELD VALUE	**RGBC GAIN VALUE**
		00	1X Gain
		01	4X Gain
		10	16X Gain
		11	64X Gain

Auxiliary Register (AUX 0x90)

The AUX register enables the ALS saturation detection interrupt. If ASIEN = 1 and an interrupt occurs it is cleared by accessing the Clear Interrupt registers at 0XE6 or 0XE7.

Figure 27:
Auxiliary Register

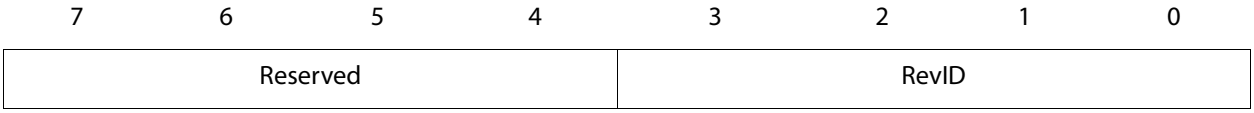


Field	Bits	Description
Reserved	7:6	**Reserved.** Write all as 0.
ASIEN	5	0 disables, 1 enables ALS Saturation Interrupt
Reserved	4:0	**Reserved.**

Revision ID Register (REVID 0x91)

This read-only register identifies the die revision level.

Figure 28:
Revision ID Register

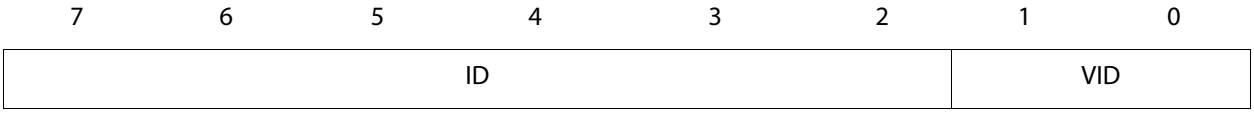


Field	Bits	Description
Reserved	7:4	**Reserved.**
RevID	3:0	Wafer die revision level

ID Register (ID 0x92)

The read-only ID register provides the device identification.

Figure 29:
ID Register

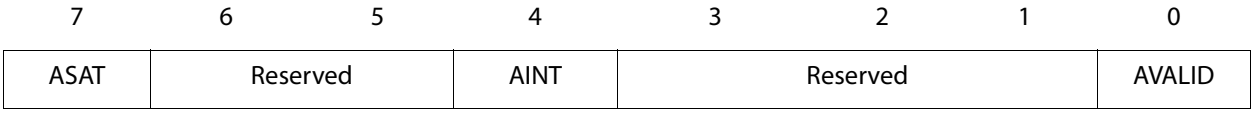


Field	Bits	Description
ID	7:2	Device Identification = 100100
VID	1:0	00b for TCS34001 & TCS34005 11b for TCS34003 & TCS34007

Status Register (STATUS 0x93)

The read-only Status Register provides the internal status of the device.

Figure 30:
Status Register



Field	Bits	Description
ASAT	7	**ALS Saturation.** When asserted, the analog sensor was at the upper end of its dynamic range. The bit can be de-asserted by sending a clear channel interrupt command (0xE6 CICLEAR) or by disabling the ALS ADC (AEN=0). ATIME and AGAIN are controls that can be adjusted to set when saturation happens. This bit triggers an interrupt if ASIEN in AUX is set.
Reserved	6:5	**Reserved.**
AINT	4	**ALS Interrupt.** If AEN is set, indicates that an ALS event that met the programmed ALS thresholds (AILT or AIHT) and persistence (APERS) occurred.
Reserved	3:1	**Reserved.**
AVALID	0	**RGBC Valid.** Indicates that the RGBC cycle has completed since AEN was asserted.

RGBC Data Registers (0x94 - 0x9B)

Clear, red, green, and blue data is stored as 16-bit values. The read sequence must read byte pairs (low followed by high) starting on an even address boundary (0x94, 0x96, 0x98, or 0x9A) inside the RGBC Data Register block. When the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Figure 31:
RGBC Data Registers

Register	Address	Bits	Description
CDATAL	0x94	7:0	Clear / IR data low byte
CDATAH	0x95	7:0	Clear / IR data high byte
RDATAL	0x96	7:0	Red data low byte
RDATAH	0x97	7:0	Red data high byte
GDATAL	0x98	7:0	Green data low byte
GDATAH	0x99	7:0	Green data high byte
BDATAL	0x9A	7:0	Blue data low byte
BDATAH	0x9B	7:0	Blue data high byte

IR Register (0xC0)

Access to IR channel; allows mapping of IR channel on clear channel.

Figure 32:
IR Register

7	6	5	4	3	2	1	0
IR	Reserved						

Field	Bits	Description
IR	7	**IR Sensor access.** If this bit is set the clear channel reports the measurement from the IR sensor (center diode).
Reserved	6:0	**Reserved.** Always write as 0.

Clear Interrupt Registers (0xE3, 0xE7)

Any dummy data byte (0x00 recommended) written to the specified register will clear the indicated interrupt.

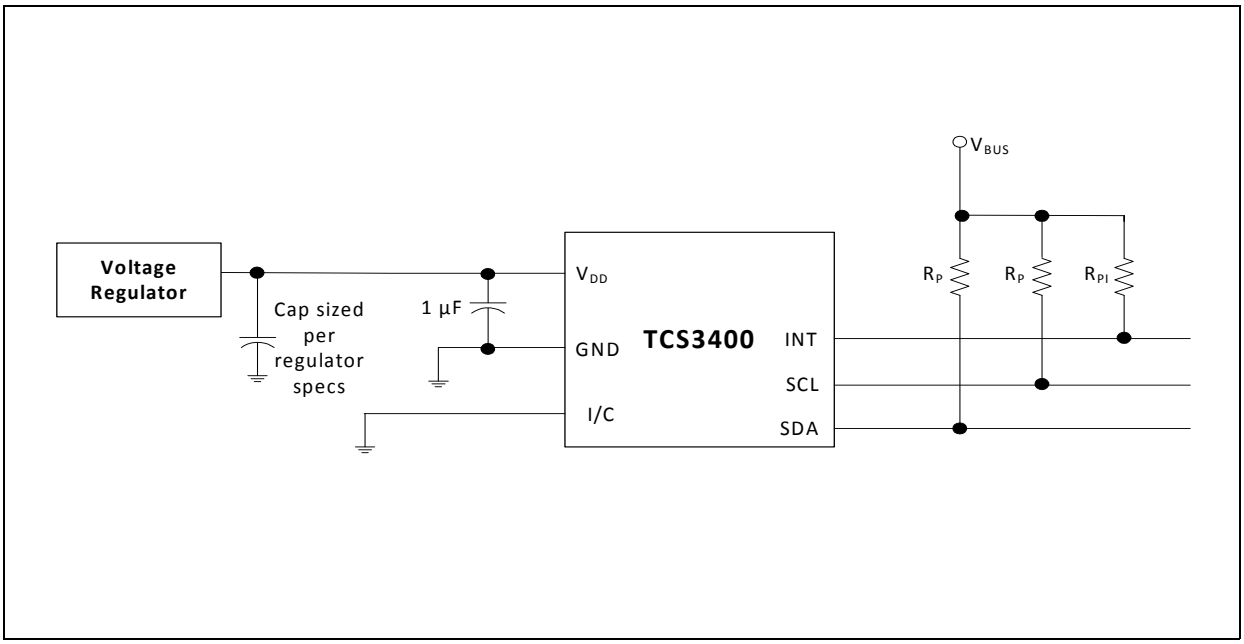
Figure 33:
Clear Interrupt Registers

Register	Address	Bits	Description
IFORCE	0xE4	7:0	Forces an interrupt (any value)
CICLEAR	0xE6	7:0	Clear channel interrupt clear (any value)
AICLEAR	0xE7	7:0	Clears all interrupts (any value)

Power Supply Considerations

Place a 1-µF low-ESR decoupling capacitor as close as possible to the V_{DD} pin.

Figure 34:
Typical Application Hardware Circuit



V_{BUS} in the above figures refers to the I^2C bus voltage which is either V_{DD} or 1.8V. Be sure to apply the specified I^2C bus voltage shown in the Ordering & Contact Information for the specific device being used.

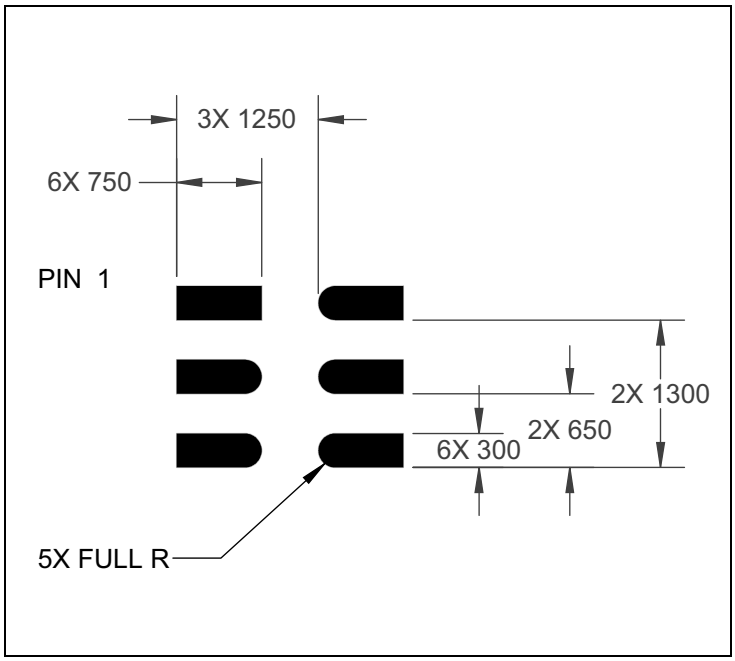
The I^2C signals and the Interrupt are open-drain outputs and require pull–up resistors. The pull-up resistor (RP) value is a function of the I^2C bus speed, the I^2C bus voltage, and the capacitive load. The **ams** EVM running at 400 kbit/s, uses 1.5-kΩ resistors. A 10-kΩ pull-up resistor (RPI) can be used for the interrupt line.

PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown. Flash Gold is recommended as a surface finish for the landing pads.

Figure 35:
Suggested PCB Layout

PCB Layout: Suggested land pattern based on the IPC-7351B Generic Requirements for Surface Mount Design and Land Pattern Standard (2010) for the small outline no-lead (SON) package.

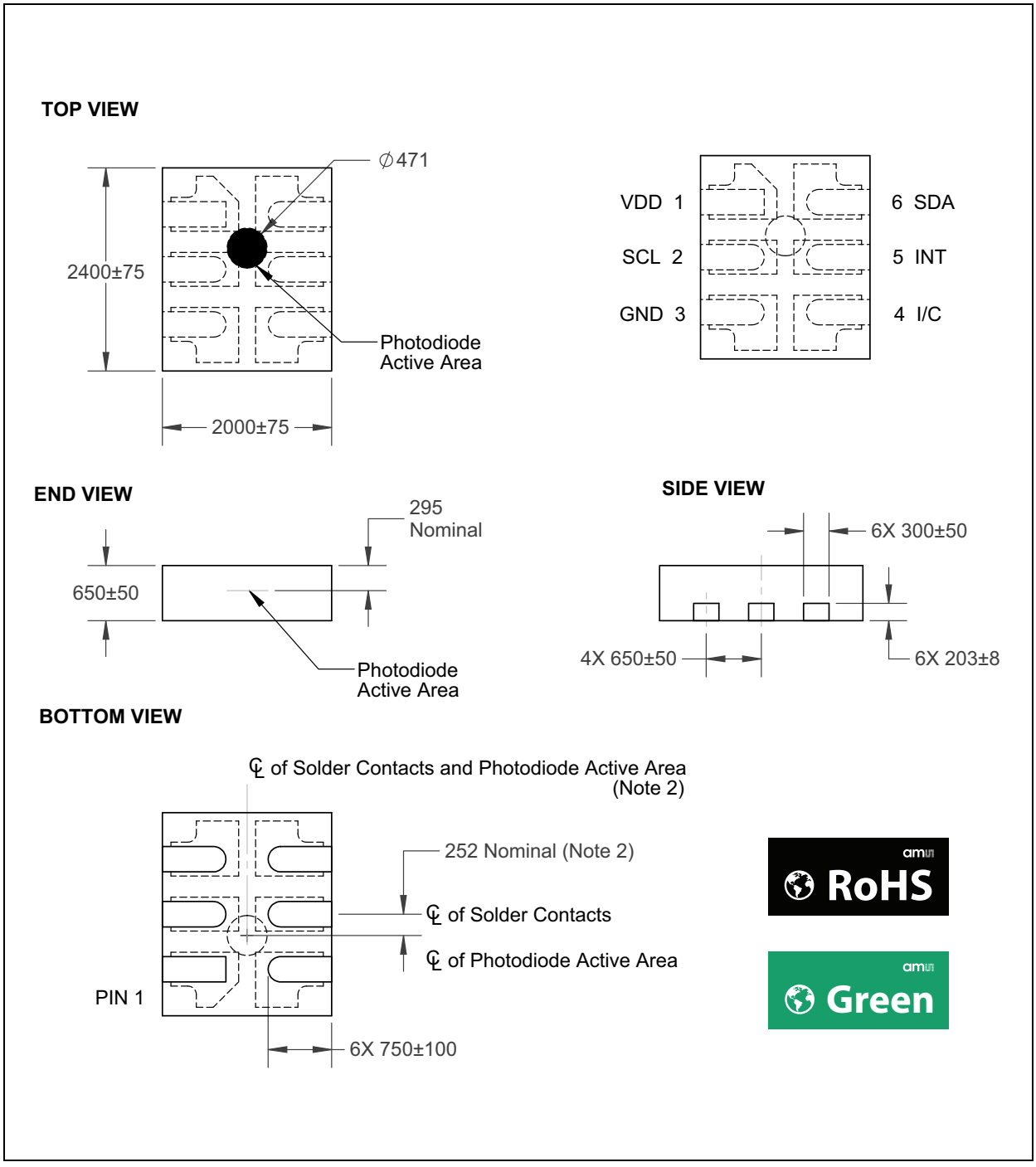


Note(s):

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

Package Drawings & Markings

Figure 36:
IC Package Mechanical Drawing

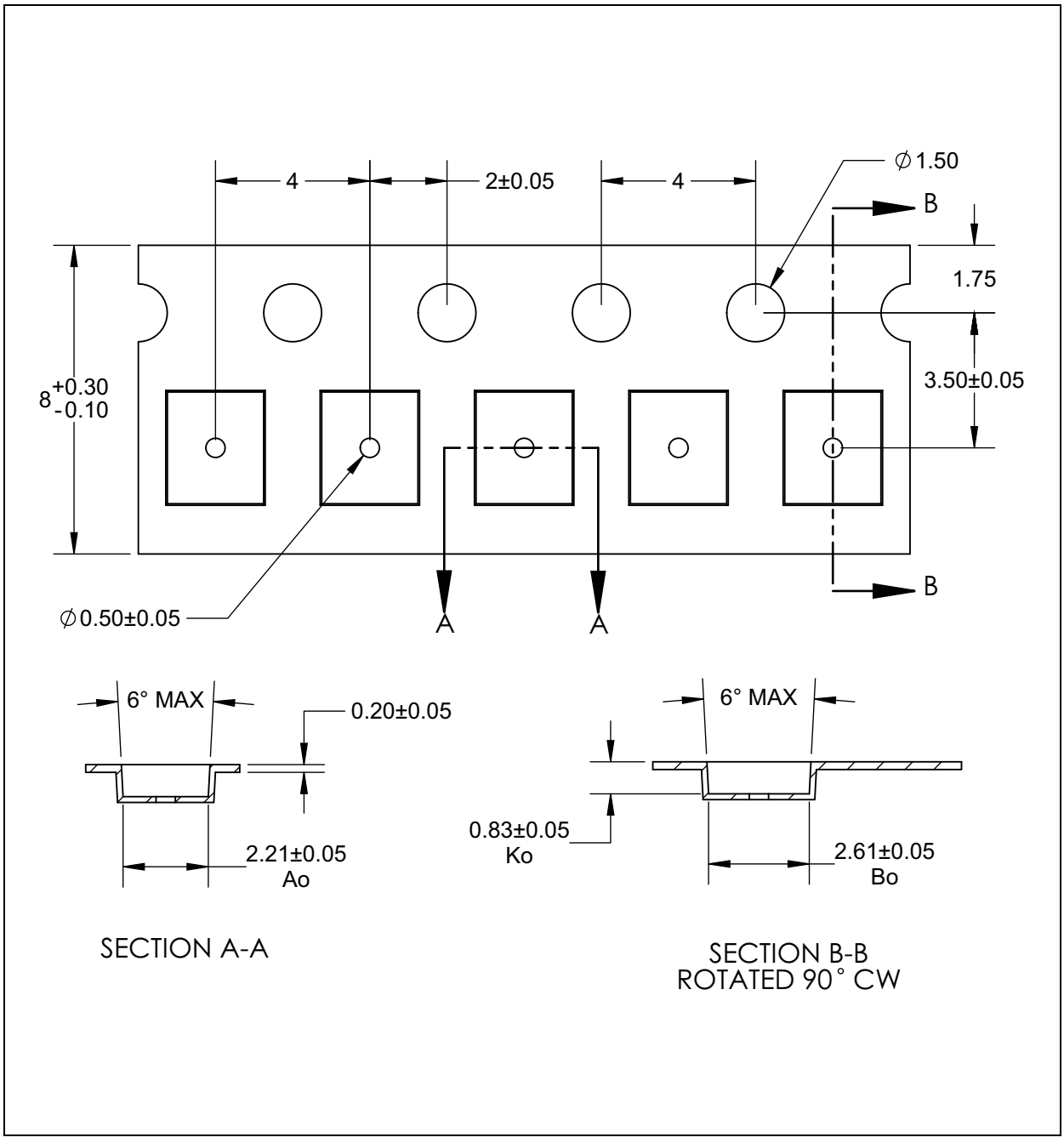


Note(s):

1. All linear dimensions are in micrometers. Dimension tolerance is ±20 µm unless otherwise noted.
2. The die is centered within the package within a tolerance of ±75 µm.
3. Package top surface is molded with an electrically non-conductive clear plastic compound having an index of refraction of 1.55.
4. Contact finish is Copper Alloy A194 with pre-plated NiPdAu lead finish.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.

Package Mechanical Data

Figure 37:
Carrier Tape & Reel Information



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing Ao, Bo, and Ko are defined in ANSI EIA Standard 481–B 2001.
4. Each reel is 330 millimeters in diameter.
5. Packaging tape and reel conform to the requirements of EIA Standard 481–B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.
8. The device pin 1 is located in the upper left corner inside the T&R pockets.

Soldering & Storage Information

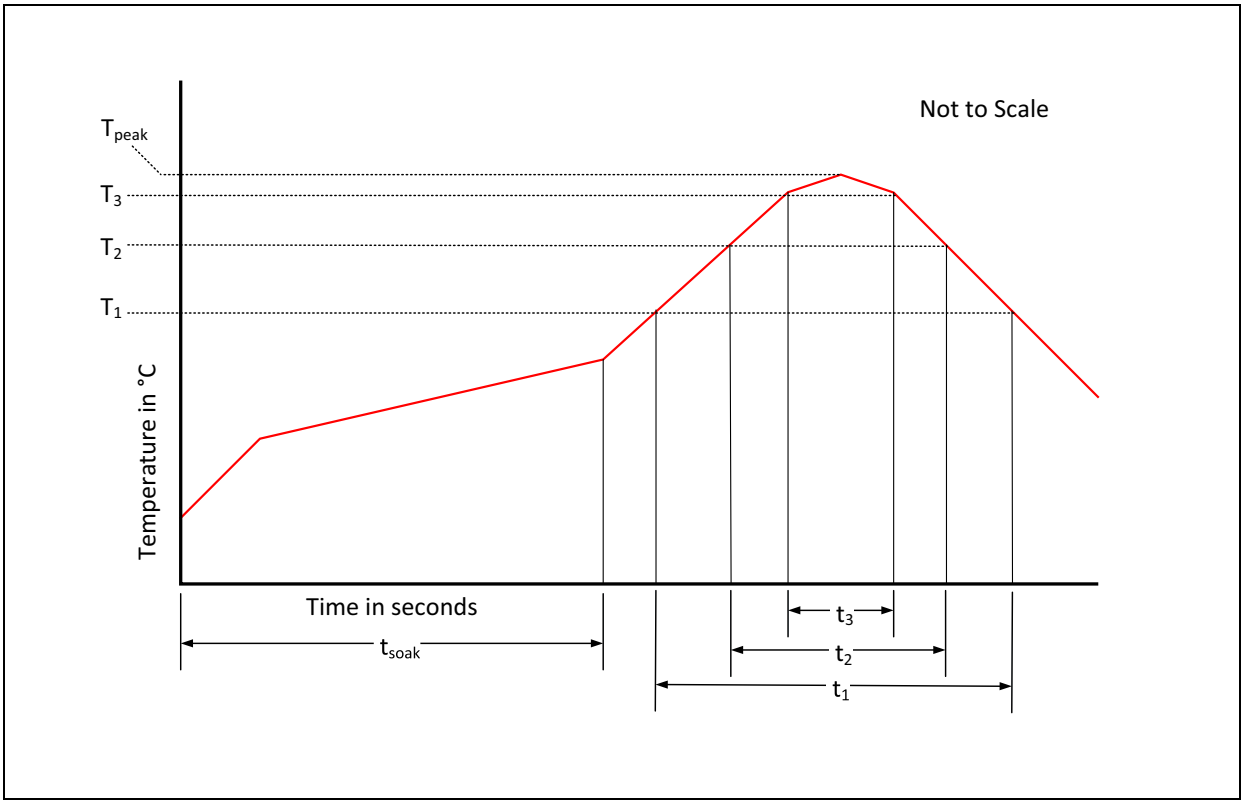
The FN package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 38:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T_1)	t_1	Max 60 s
Time above 230 °C (T_2)	t_2	Max 50 s
Time above T_{peak} - 10 °C (T_3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260 °C
Temperature gradient in cooling		Max -5 °C/s

Figure 39:
Solder Reflow Profile Graph



Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping.

Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: < 40°C
- Relative Humidity: < 90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The FN package has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: < 30°C
- Relative Humidity: < 60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

The device is packaged in a small OFN (Optical FN) package which is 2mm x 2.4mm.

Figure 40:
Ordering Information

Ordering Code	Address	Interface	Delivery Form	Delivery Quantity
TCS34001FN	0x39	I^2C $V_{BUS} = V_{DD}$ Interface	FN-6	12000 pcs/reel
TCS34001FNM	0x39	I^2C $V_{BUS} = V_{DD}$ Interface	FN-6	500 pcs/reel
TCS34003FN	0x39	I^2C bus = 1.8V Interface	FN-6	12000 pcs/reel
TCS34003FNM	0x39	I^2C bus = 1.8V Interface	FN-6	500 pcs/reel
TCS34005FN (1)	0x29	I^2C $V_{BUS} = V_{DD}$ Interface	FN-6	12000 pcs/reel
TCS34005FNM (1)	0x29	I^2C $V_{BUS} = V_{DD}$ Interface	FN-6	500 pcs/reel
TCS34007FN	0x29	I^2C bus = 1.8V Interface	FN-6	12000 pcs/reel
TCS34007FNM	0x29	I^2C bus = 1.8V Interface	FN-6	500 pcs/reel

Note(s):

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Revision Information

Changes from 1-05 (2016-Aug-11) to current revision 1-06 (2017-Oct-10)	Page
Updated Figure 40	29

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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