座位号 考场教室 任课教师 学号 姓名 学院 密 封 线 以 内 答 题 无 效

电子科技大学 2020-2021 学年第 一 学期期末考试 A 卷

考试科目： 数字逻辑设计及应用 考试形式： 闭卷 考试日期： 2021 年 1 月 14 日

本试卷由 六 部分构成，共 7 页。考试时长： 120 分钟

成绩构成比例：平时成绩 60 %， 期末成绩 40 %

（可以使用中文解答；禁止使用计算器；题中所用器件功能表见试卷后附录（Appendix））

题号	I	II	III	IV	V	VI	合计
得分							

得分

I. Please put the correct answers in the brackets "( )" .(3' X 8 = 24')

1. A sequential circuit with 4 flip-flops can store (16) states at most.
2. A modulo-288 counter circuit can be built by (3) 4-bit counters of 74x163 at least.
3. To design a "001010" serial sequence generator by shift registers, (4) flip-flops are required at least.
4. There is a state transition equation Q*=JQ'+K'Q. If we use a D flip-flop for state memory, the D input of the D flip-flop can be given as: D = (JQ'+K'Q).
5. An *n*-bit Johnson counter has (2^n-2n) abnormal states.
6. Two common types of ripple counter are ripple up counter and ripple down counter. The circuit shown in Figure1-1 is a 2-bit ripple (up) counter.
7. A 74×194 can be used as a sequence detector. When Z shown in Figure 1-2 is asserted, the sequence detected is (10110).

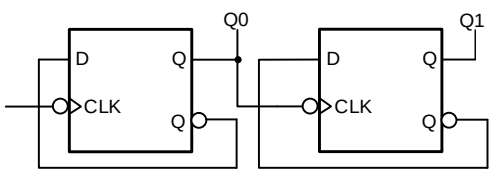


Figure 1-1

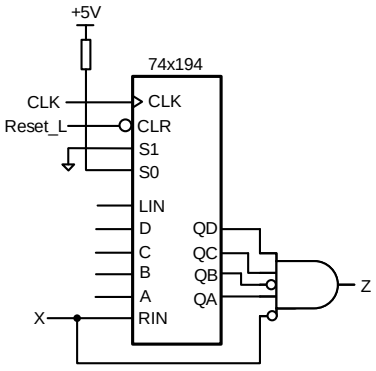


Figure 1-2

8. If a ROM has 13 address inputs and 8 data outputs, its capacity is (__8__)Kbyte.

得分

II. Choose the correct answer and put the item number in the brackets. (3' X 5=15')

1. Which of the following statements is correct? (A)

A. Both outputs of Mealy and Moore machine depend on states.

B. The outputs of a Mealy machine depend only on the states.

C. The outputs of a Moore machine depend on the inputs and states.

D. Both outputs of Mealy and Moore machine depend on inputs.

2. A temperature test system whose temperature measurement range is -45℃~125℃. If the A/D converter in the system needs to recognize a temperature change of 0.1°C, an A/D converter with (B) bits is required at least.

A. 10 B. 11 C. 12 D. 13

3. A logic diagram is shown in Figure 2 and the current state Q3Q2Q1Q0=1111. If the CONTROL terminal is connected to HIGH level and LOW level respectively, the next state Q3*Q2*Q1*Q0* should be (C).

A. 0000 and 1111 B. 1111 and 0000

C. 0000 and 0000 D. 1111 and 1111

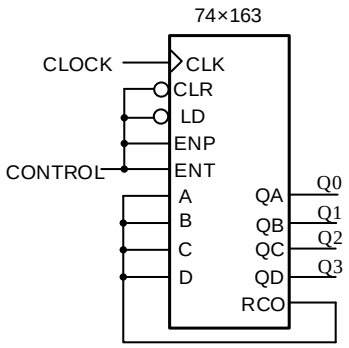


Figure 2

4. A 4×4 unsigned binary multiplication can be built with a (D) ROM.

A. 128×4 B. 256×4

C. 128×16 D. 256×8

5. In the following circuits, only (C) is a sequential logic circuit.

A. Three-State Buffers B. Comparators C. shift registers D. Decoders

得分

III. Analyze the sequential circuit shown in Figure3-1. (10')

(1) Assuming the initial state Q1Q2=00, draw the timing diagrams for Q1, Q2 and Z shown in Figure 3-2. [7']

(2) According to the frequencies of the waveforms in Figure 3-2, what is the relation between Z and CLK? [3']

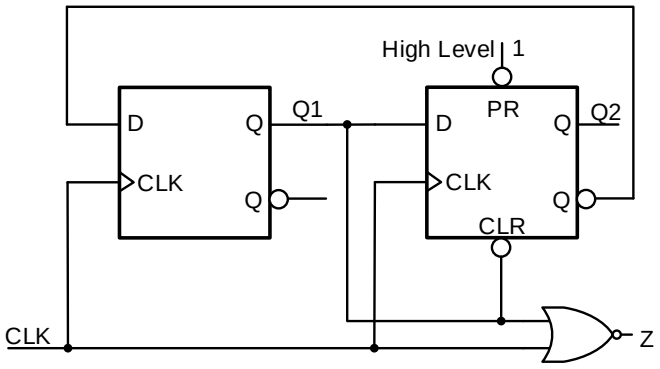


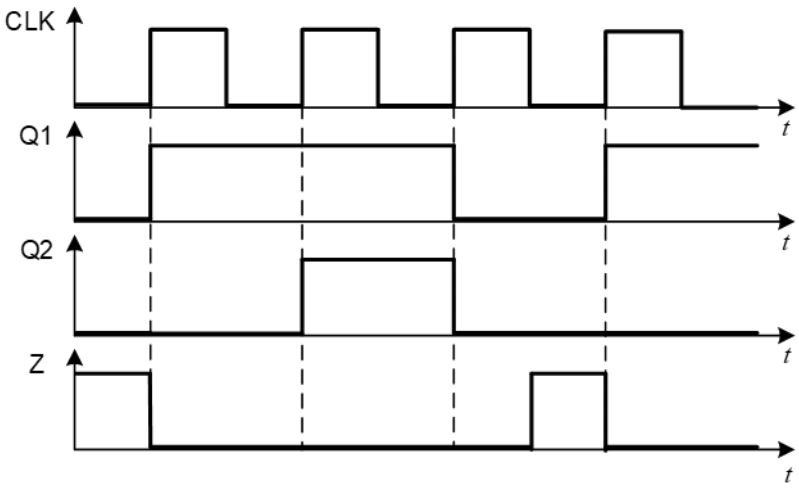
Figure 3-1

清零信号是否需要按照异步复位和同步复位两种情况分别考虑？（这道题没有明确提出是异步复位）

答案及参考评分：

(1) 从 CLK 的第一个上升沿开始，波形 Q1，Q2，Z 各 2 分（每时钟周期错误扣 0.5 分），共 6 分；初始段 Z 正确给 1 分

(2) Z 对 CLK 进行 3 分频。回答正确 3 分。



得分

IV. Analyze the sequential circuit shown in Figure 4. (17')

(1) Draw the state diagram of the sequential circuit whose state is QD QC QB QA. [16']

(2) According to the state diagram obtained from above, is the sequential circuit self-correcting or not? (yes/self-correcting/自校正/自启动/) [1']

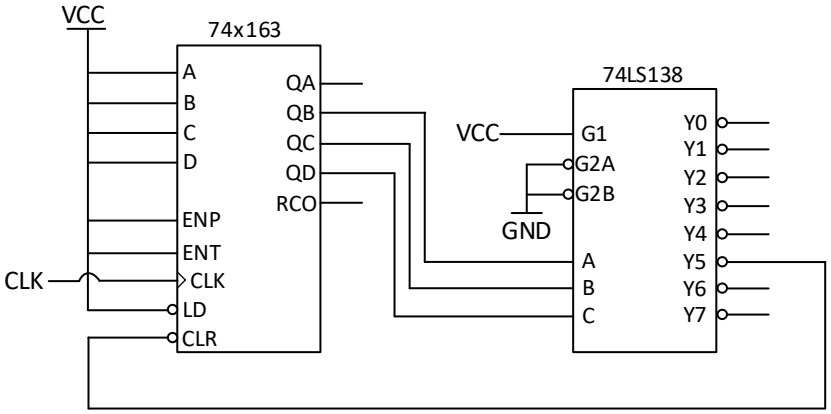
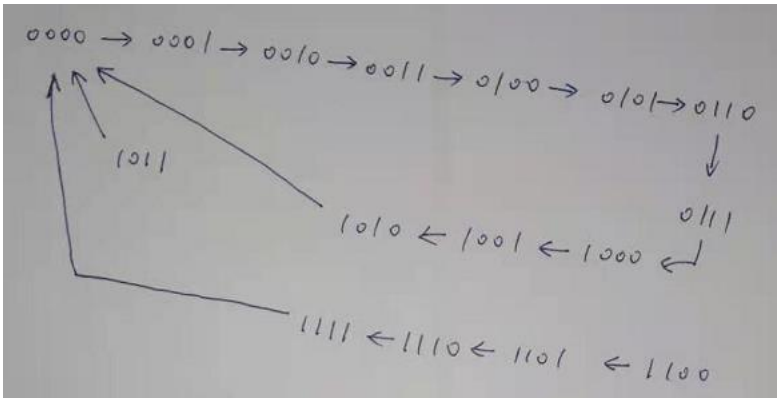


Figure 4

QD QC QB QA



每个状态位置正确给 1 分。

得分

V. Design a clocked synchronous state machine with D flip-flops to obtain the output waveforms shown in Figure 5, where Q2, Q1 and Q0 are outputs of D flop-flops. (16’)

(1) Give the transition table of the state machine based on Figure 5. (choose the approach of minimal cost for unused states). [6’]

(2) List the unused states Q2Q1Q0 and their next states Q2*Q1*Q0* to show that whether or not the circuit is self-correcting. [5’]

(3) Give the logic diagram. [5’]

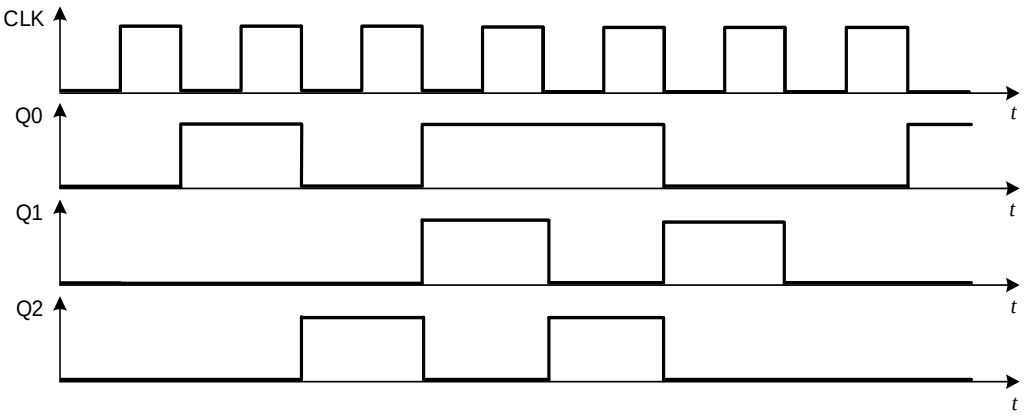
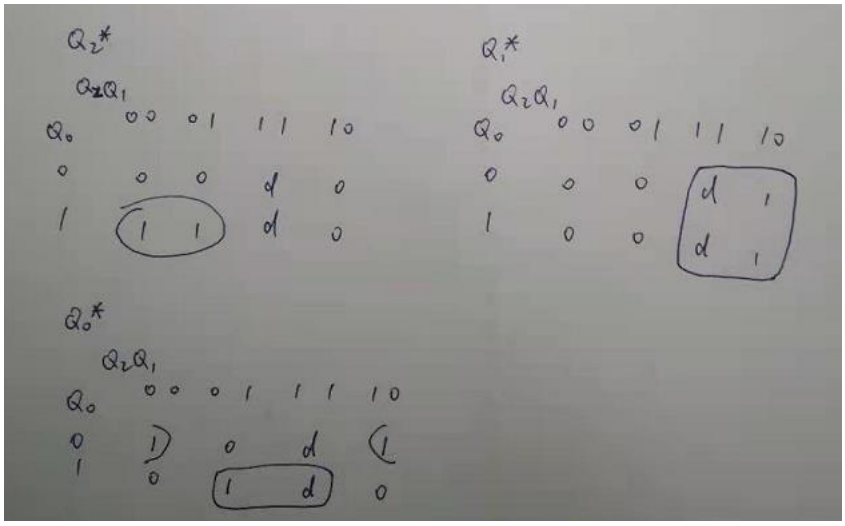


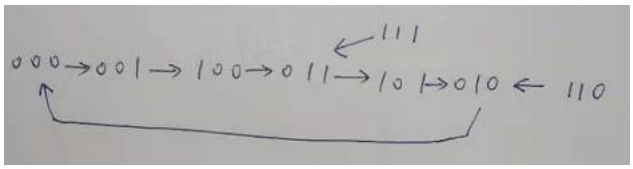
Figure 5

(1)



每个状态转换表正确给 2 分；

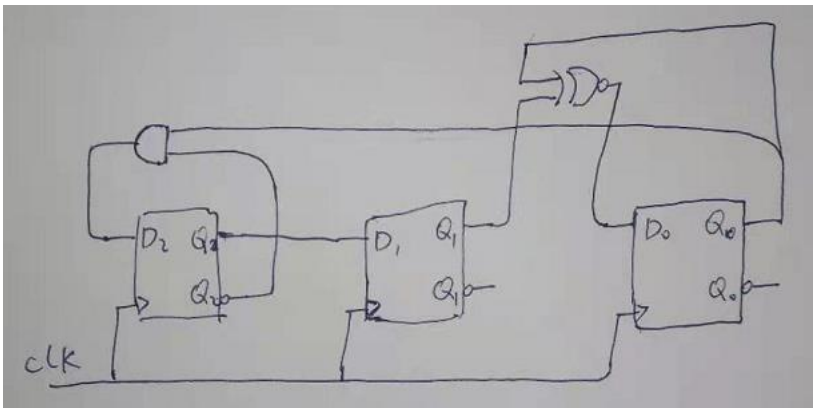
(2)



具有自较正功能。

正确给出 011、111 之间的状态关系得 1 分；010、110 之间的状态关系得 1 分；回答出具有自较正功能给 1 分；正确画出状态图其他部分得 2 分。

(3)D2=Q2’Q0;　D1=Q2;　D0=Q1Q0+Q1’Q0’;



正确给出逻辑图得 5 分；否则正确给出一个驱动方程给 1 分。

得分

VI. Design a "0111010001" sequence generator with a 4-bit shift register 74x194. (18')

(1) Complete the Table 2 to realize the above sequence generator. Q3, Q2, Q1 and Q0 in Table 2 represent the corresponding signals in Figure 6. Choose the approach of minimal risk for unused states. [8']

(2) If Q0* is obtained by an 8-input, 1-bit multiplexer 74x151, please give the values of D0~D7 in Figure 6. [8']

(3) Give the values of the other signals or connect them in Figure 6 to make the circuit work properly. [2']

答案及参考评分：

(1) 每行 1 分，共 8 分；

(2) 每输入端 1 分，共 8 分。

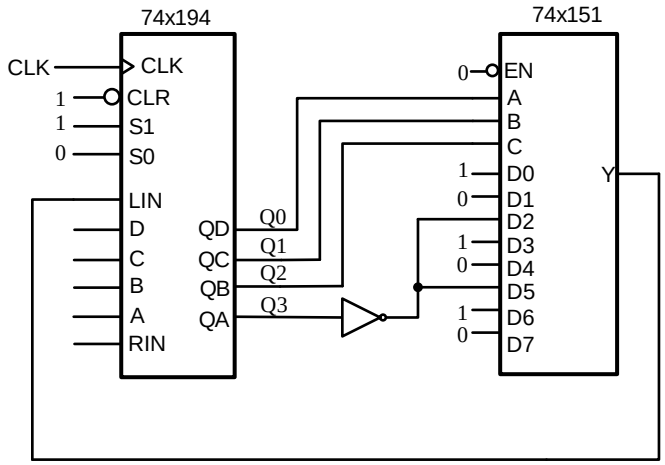
(3) Y 连接至 LIN，1 分

S1S0=10，1 分

其它端子连接不正确，适当扣分，扣完为止。

Table 2 Transition table

Q3	Q2	Q1	Q0	Q3*	Q2*	Q1*	Q0*
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	1
0	1	0	0	1	0	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	1	0
1	1	1	0	1	1	0	1
1	1	1	1	1	1	1	0


74x194
CLK
CLK
1
CLR
1
S1
0
S0
LIN
D
C
B
A
RIN
QD
QC
QB
QA
Q0
Q1
Q2
Q3
74x151
0
EN
A
B
C
1
D0
0
D1
D2
1
D3
0
D4
D5
1
D6
0
D7
Y

Appendix: functional tables for some integrated circuits

Function table for a 74x138 decoder

Inputs							Outputs							
G1	G2A_L	G2B_L	C	B	A	Y7_L	Y6_L	Y5_L	Y4_L	Y3_L	Y2_L	Y1_L	Y0_L
0	x	x	x	x	x	1	1	1	1	1	1	1	1
x	1	x	x	x	x	1	1	1	1	1	1	1	1
x	x	1	x	x	x	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	1	0	1	1	1	1	1
1	0	0	1	1	0	1	0	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1	1

Function table for a 74x194 4-bit universal shift register

Inputs		Next state				Function
S1	S0	QA*	QB*	QC*	QD*	
0	0	QA	QB	QC	QD	Hold
0	1	RIN	QA	QB	QC	Shift right
1	0	QB	QC	QD	LIN	Shift left
1	1	A	B	C	D	Load

Truth table for a 74x151 8-input 1-bit multiplexer

Inputs				Outputs	
EN_L	S2	S1	S0	Y	Y_L
1	x	x	x	0	1
0	0	0	0	D0	D0’
0	0	0	1	D1	D1’
0	0	1	0	D2	D2’
0	0	1	1	D3	D3’
0	1	0	0	D4	D4’
0	1	0	1	D5	D5’
0	1	1	0	D6	D6’
0	1	1	1	D7	D7’

Function table for a 74x163 4-bit binary counter

Inputs				Current State	Next state	Output
CLR_L	LD_L	ENT	ENP	Q_D Q_C Q_B Q_A	Q_D* Q_C* Q_B* Q_A*	RCO
0	X	X	X	X X X X	0 0 0 0	0
1	0	X	X	X X X X	D C B A	0
1	1	0	X	X X X X	Q_D Q_C Q_B Q_A	0
1	1	X	0	X X X X	Q_D Q_C Q_B Q_A	0
1	1	1	1	0 0 0 0	0 0 0 1	0
1	1	1	1	0 0 0 1	0 0 1 0	0
1	1	1	1	0 0 1 0	0 0 1 1	0
1	1	1	1	0 0 1 1	0 1 0 0	0
1	1	1	1	……	……	0
1	1	1	1	1 1 1 1	0 0 0 0	1

Truth table for a 74x85 magnitude comparator

Inputs							Outputs		
A3,B3	A2,B2	A1,B1	A0,B0	A>BIN	A<BIN	A=BIN	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	0	1	0
A3=B3	A2>B2	X	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	0	1	0

A3=B3	**A2=B2**	**A1>B1**	**X**	**X**	**X**	**X**	**1**	**0**	**0**
A3=B3	**A2=B2**	**A1<B1**	**X**	**X**	**X**	**X**	**0**	**1**	**0**
A3=B3	**A2=B2**	**A1=B1**	**A0>B0**	**X**	**X**	**X**	**1**	**0**	**0**
A3=B3	**A2=B2**	**A1=B1**	**A0<B0**	**X**	**X**	**X**	**0**	**1**	**0**
A3=B3	**A2=B2**	**A1=B1**	**A0=B0**	**X**	**X**	**X**	**A>BIN**	**A<BIN**	**A=BIN**