学院 姓名 学号 任课教师 考场教室 座位号

密 封 线 内 以 答 题 无 效

电子科技大学 2016-2017 学年第 二 学期期 末 考试 A 卷

考试科目： 数字逻辑设计及应用 考试形式： 闭卷 考试日期： 2017 年 7 月 5 日

成绩构成比例：平时 30/20 %， 期中 30/20 %， 小班研讨 20 %， 期末 40 %

本试卷由 V 部分构成，共 5 页。考试时长： 120 分钟 注：

题号	I	II	III	IV	V	合计
得分						

得 分

I. Please fill out the correct answers in the brackets "( )". (4' X 10 = 40')

1. The 74x148 is an 8-input priority encoder with active low inputs and outputs. If its I0, I2 and I4 inputs are activated then the output code is (011).
2. If a 74x283 4-bit binary adder has A=1011 and B=1100 and C0=0 on its inputs, the 74x283's outputs C4S3S2S1S0 is (10111).
3. If a D flip-flop is constructed by a T flip-flop with an enable input EN, then the input EN=(D⊕Q).
4. To design a "110111" serial sequence generator by shift-register, (5 或 3) flip-flops are need at least.
5. To build a modulus-191 counter, it requires at least (3) 74x162s, if its initial count is 808, its terminal count is (998).
6. A sequential circuit whose output depends only on its state is called a (Moore) state machine.
7. If an odd number of shift-register outputs are connected to the odd-parity circuit in an n-bit LFSR counter, its modulus is(2^n 或 2^n-1 或 2^n-2 或 2^{n-1}).
8. The capacity of a memory that has 20 bits address bus and can store 8 bits at each address is (1)MB.
9. When the input is 00001000 of an 8 bit DAC, the corresponding output voltage is -2V. The output voltage range for the DAC is (-63.75 ~ 0 或等值表达式)V.

得 分

I I. Choose the only one correct answer and fill the item number in the brackets. (3' X 5=15')

1. If use a 74x85 magnitude comparator to compare only two 4-bits binary numbers, the 74x85's cascading inputs should be (B).

A) ALTBIN=0, AEQBIN=0, AGTBIN=1 B) ALTBIN=0, AEQBIN=1, AGTBIN=0

C) ALTBIN=1, AEQBIN=0, AGTBIN=0 D) ALTBIN=1, AEQBIN=0, AGTBIN=1

2. For an edge-triggered D flip-flop, (D) is incorrect.

A) A change in the state of the flip-flop can only at a clock pulse edge

B) The state that the flip-flop goes to depends on the D input

C) The output follows the input at each clock pulse

D) None of the above answers

3. An asynchronous counter differs from a synchronous counter in (B).

A) The value of the modulus B) The method of clocking

C) The type of flip-flops used D) The number of states in its sequence

4. With a 100KHz clock frequency for the decade counter 74x162 free-running mode, (A) is correct.

A) f_{QA}= 50KHz B) f_{QB}= 25KHz C) f_{QC}= 12.5KHz D) f_{QD}=6.25KHz

5.When an 8-bit serial in/serial out shift register is used for a 16μ s time delay, the clock frequency must be (C).

A)5KHz B) 50KHz C) 500KHz D) 50Hz

得 分

III. A sequential circuit is shown in Fig. 1, where the frequency of CLK is 1MHz. Assume the initial state for Q2Q1Q0 is 000. (20')

(1) Write out the excitation equation and the transition equation for the circuit. (6')

(2) Draw the timing diagram for Q2, Q1 and Q0. （6'）

(3) Indicate the modulus of the circuit, and check whether it is self-correction. (6')

(4) What is the frequency for Q2 ? （2'）

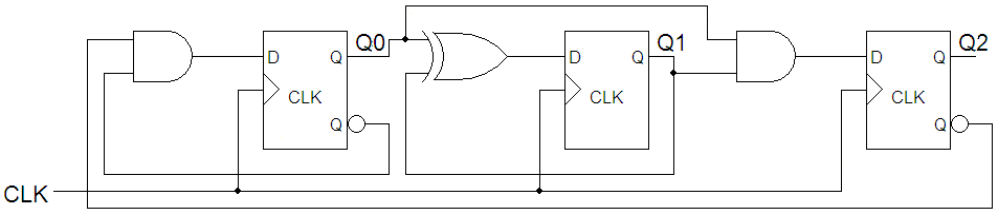
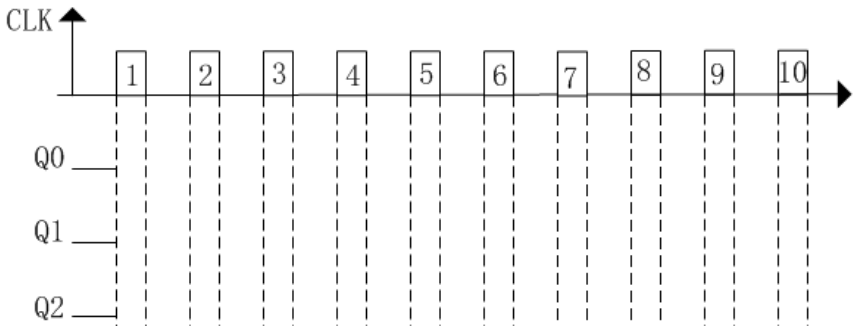


Fig. 1



【参考答案】

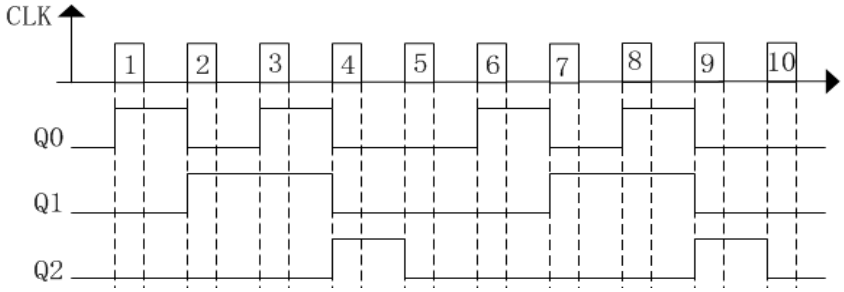
（1） Excitation equation: （共 3 分，每个激励方程正确得 1 分，错扣 1 分）

$$D0=(Q0+Q2)' \qquad D1=Q0\oplus Q1 \qquad D2=Q0\cdot Q1$$

Transition equation:（共 3 分，每个转移方程正确得 1 分，错扣 1 分）

$$Q0^*=(Q0+Q2)' \qquad Q1^*=Q0\oplus Q \qquad Q2^*=Q0\ Q$$

（2）本小题 6 分，每个波形 2 分。每个波形错一处扣 0.5 分，扣完该波形的 2 分为止。



（3）该电路的模是 5。（得 3 分）

Q2Q1Q0 状态转移关系是：000->001->010->011->100->000, 101->010, 110->010, 111->100 没有无效循环，因此该电路能自启动。（得 3 分）

（4）由于 Q2 的频率是 CLK 的 1/5，因此 Q2 的频率是 200kHz。（得 2 分）

得 分

IV. The output timing diagram of a synchronous sequential circuit is shown in Fig. 2. Design the circuit only using one 74163, one 74138 and necessary NAND gates. Assume the initial state QDQCQBQA for 74163 is 0000, and the output F1F2F3 is 101. (15')

(1) Indicate the modulus of the counter, and write out LD_L(QC，QB，QA). (6')

(2) Write out the minterm list for F1(QC, QB, QA)，F2(QC, QB, QA)和 F3(QC, QB, QA). (6')

(3) Draw the schematic diagram. (3')

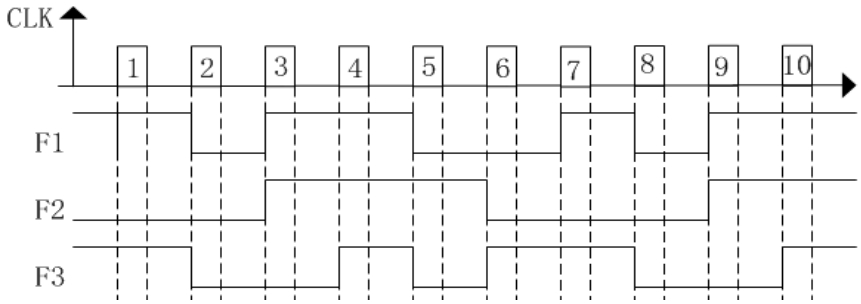
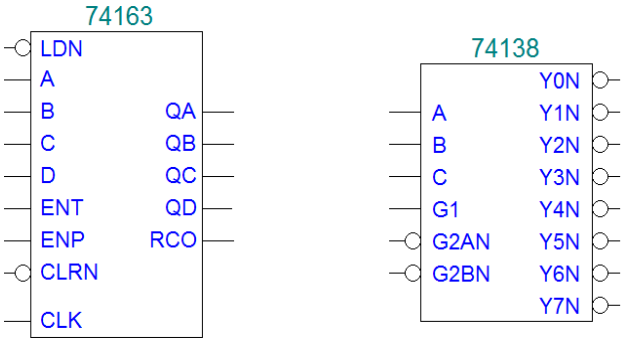


Fig. 2



Function table for 74163

Inputs				Current State	Next state	Output
CLR_L	LD_L	ENT	ENP	Q_D Q_C Q_B Q_A	Q_D* Q_C* Q_B* Q_A*	RCO
0	X	X	X	X X X X	0 0 0 0	0
1	0	X	X	X X X X	D C B A	0
1	1	0	X	X X X X	QD QC QB QA	0
1	1	X	0	X X X X	QD QC QB QA	0
1	1	1	1	0 0 0 0	0 0 0 1	0
1	1	1	1	0 0 0 1	0 0 1 0	0
1	1	1	1	0 0 1 0	0 0 1 1	0
1	1	1	1	0 0 1 1	0 1 0 0	0
1	1	1	1	……	……	0
1	1	1	1	1 1 1 1	0 0 0 0	1

【参考答案】

（1）根据波形图得到 F1 F2 F3 状态转移关系为：101->000->110->111->010->001->101，因此，该电路是一个模 6 计数器。（得 2 分）

用 74163 设计一个模 6 计数器，QC QB QA 计数顺序（不唯一）为：

000->001->010->011->100->101->000

$LD\_L(QC,QB,QA)=(QC\cdot QA)'$ （表达式正确，得 4 分）

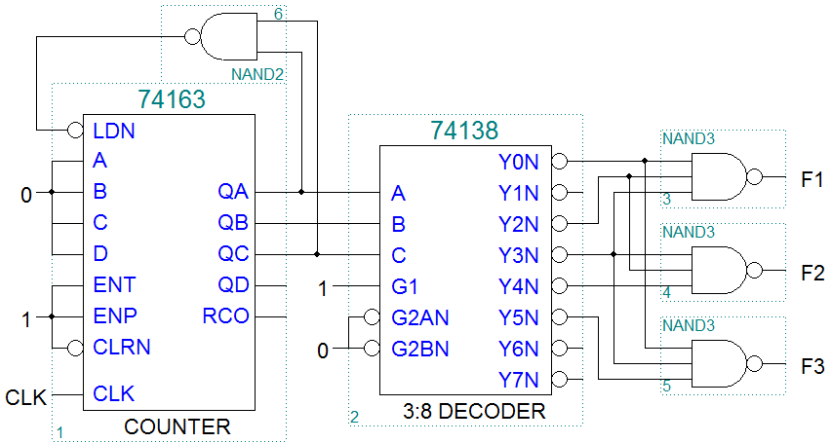
（2）列出 QC QB QA 与 F1 F2 F3 的关系表（不唯一）

QCQBQA	F1F2F3
000	101
001	000
010	110
011	111
100	010
101	001

$F1(QC,QB,QA)=\sum_{QCQBQA}(0,2,3)$　　$F2(QC,QB,QA)=\sum_{QCQBQA}(2,$

$F3(QC,QB,QA)=\sum_{QCQBQA}(0,3,5)$　（每个表达式正确得 2 分；错一处扣 1 分，扣完为止）

（3）（电路连线正确得 3 分，错一处扣 0.5 分，扣完 3 分为止）



V. Analyze the circuit shown in Fig. 3.　　(10')

(1) Draw the whole state diagram of (QA QB QC) for 74194.　　(6')

(2) Write out the logic function F1(QA,QB,QC) and F2(QA,QB,QC).　　(4')

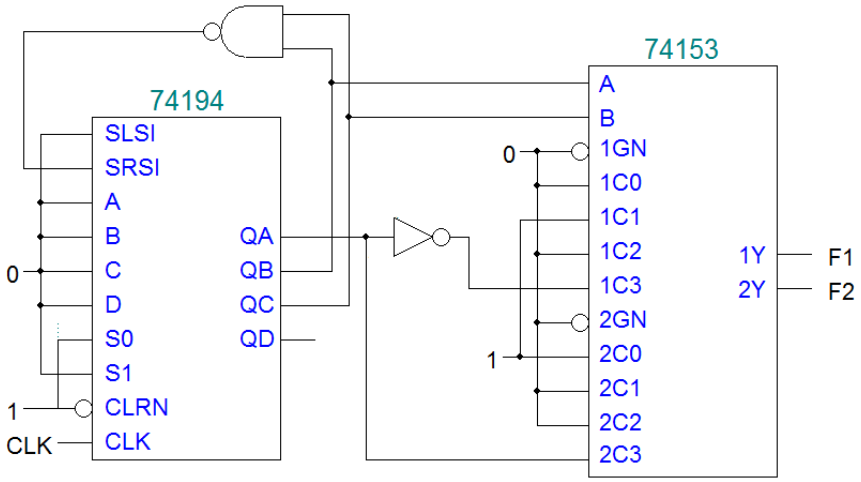


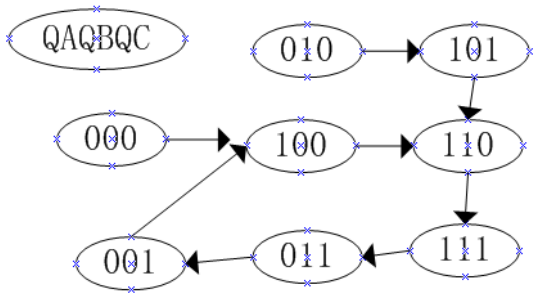
Fig. 3

The function table for 74194

Iutputs		Next state				Function
S1	S0	QA*	QB*	QC*	QD*	
0	0	QA	QB	QC	QD	Hold
0	1	RIN	QA	QB	QC	Shift right
1	0	QB	QC	QD	LIN	Shift left
1	1	A	B	C	D	Load

【参考答案】

（1）本小题 6 分（错一个状态转换扣 1 分，扣完为止）



（2）本小题 4 分（每个表达式正确得 2 分，错一项扣 1 分，扣完为止）

F1 = QB QC'+ QA' QB QC 或 QB QC'+ QA' QB

或 $\sum_{QAQBQC}(2, 3, 6)$ 或 $\sum_{QCQBQA}(2, 3, 6)$

F2 = QB' QC'+ QA QB QC 或 $\sum_{QAQBQC}(0, 4, 7)$ 或 $\sum_{QCQBQA}(0, 1, 7)$