期中考试示例

1. Which of the following four unsigned numbers is the **largest**? (C)

A. $(101001110)_2$ B. $(517)_8$ C. $(337)_{10}$ D. $(14D)_{16}$

2. The 8-bit two's-complement representation for the decimal number $(-52)_{10}$ is(B).

A. 10110100 B. 11001100 C. 11110100 D. 10001100

3. In a positional number system, the radix is r. If we have 300/13=20, then r=(C).

A. 4 B. 5 C. 6 D. 7

4. If number $[A]_{\text{two's-complement}}=(10010011)$, which of the following expressions is correct? (D)

A. $[A]_{\text{ones'-complement}}=(01101100)$ B. $[A]_{\text{ones'-complement}}=(11101101)$

C. $[A]_{\text{signed-magnitude}}=(01101101)$ D. $[A]_{\text{signed-magnitude}}=(11101101)$

5. In an 8-bit digital system, if number $[A]_{\text{two's-complement}}=11111001$ and $[B]_{\text{two's-complement}}=01111101$, then $[A+B]_{\text{two's-complement}}=$(D).

A. (01110110, overflow) B. (10000111, not overflow)

C. (10000111, overflow) D. (01110110, not overflow)

6. For the Decimal number 17, Which one is **NOT** correct in the following codes? (D)

A. $(0001\ 0111)_{8421}$ B. $(0100\ 1010)_{\text{Excess-3}}$ C. $(11001)_{\text{Gray}}$ D. $(0001\ 0111)_{2421}$

7. An open-drain output cannot output (B) level directly.

A. LOW B. HIGH C. Hi_Z D. all above are wrong

8. If the parameters of gate A are defined as follows: V_{OLmax} = 0.5 V, V_{OHmin} = 2.7 V, V_{ILmax} = 0.8 V, V_{IHmin} = 2.0 V, the parameters of gate B are defined as follows: V_{OLmax} = 0.33 V, V_{OHmin} = 3.84V, V_{ILmax} = 1.35 V, V_{IHmin} = 3.15 V, then which of the following statements is **WRONG** based on noise margin? (B)

A. Gate A can drive gate A. B. Gate A can drive gate B.

C. Gate B can drive gate B. D. Gate B can drive gate A.

9. Assigning 0 to Low and 1 to High is called positive logic. A CMOS 2-input NAND gate in positive logic is called (C) gate in negative logic.

A. AND B. OR C. NOR D. NAND

10. If you are allowed to choose only one kind of logic gate to design a combinational circuit, which gates are the proper choices? (C)

A. AND B. OR C. NAND D. NOT

11. Given that $F = \Sigma_{ABC}(0, 1, 4, 7)$, then the maxterm list for F^D is (B).

A. $\Sigma_{ABC}(1, 2, 4, 5)$ B. $\Pi_{ABC}(0, 3, 6, 7)$ C. $\Pi_{ABC}(1, 2, 4, 5)$ D. $\Pi_{ABC}(2,3,5,6)$

12. What is the logic function for the following circuit shown in Figure 1? (A)

A. F=AB B. F=A+B C. F= (AB)' D. F= (A+B)'

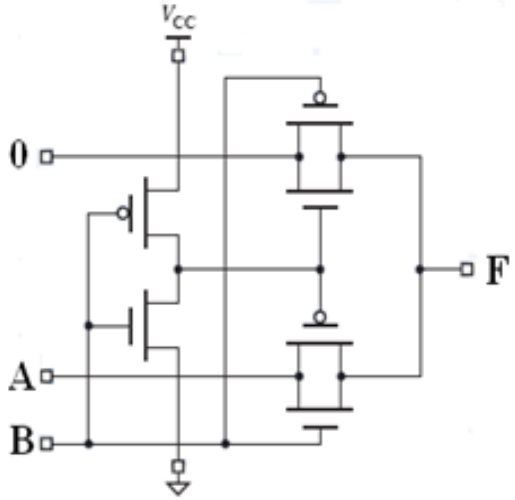


Figure 1

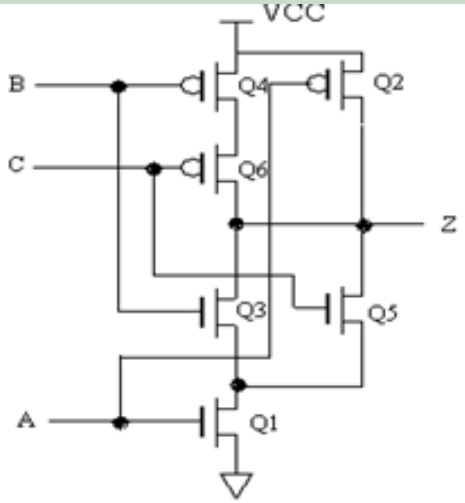
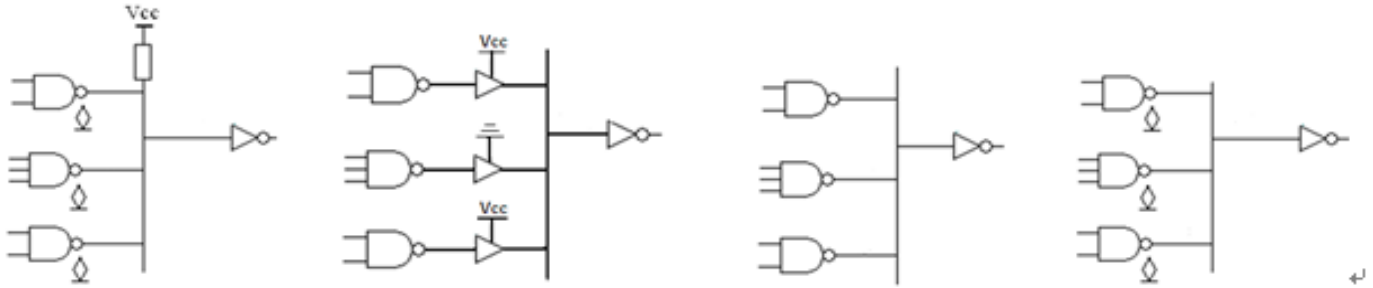


Figure 2

13. A CMOS logic circuit is showing as Figure 2. The logic expression of output Z is (D).

A. A'B'+A'C' B. AB+AC C. A+BC D. A'+B'C'

14. Which of the following connection is correct? (A)



A. B. C. D.

15. If logic function $F=\sum_{ABC}(1,2,3,6)$, $G=\sum_{ABC}(0,2,3,4,5,7)$, then F•G=(C) 。

A. 0 B. 1 C. A'B D. AB'

16. For a combination logic circuit, the timing waveforms of inputs A, B, C and output F are shown as Figure 3. The standard representations of the logic function is F=(A).

A. $\Sigma_{ABC}(2, 3, 6, 7)$ B. $\Sigma_{ABC}(1, 2, 5, 6)$ C. $\Sigma_{ABC}(0, 1, 4, 5)$ D. $\Sigma_{ABC}(0, 1, 6, 7)$

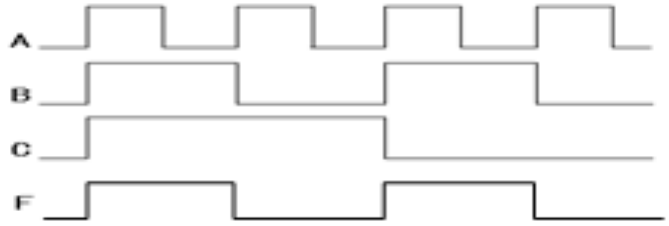


Figure 3

17. Given the circuit shown in Figure 4, the output enables A and B of three-state buffers will meet some constraint condition. Its constraint equation is (D).

A. X+Y=1 B. X+Y=0 C. XY=1 D. XY=0

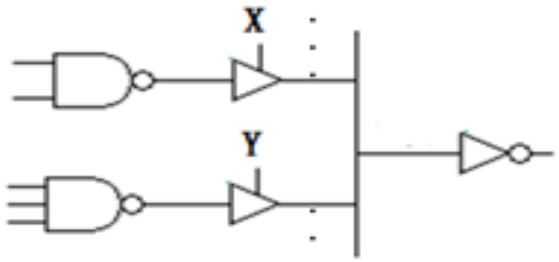


Figure 4

18. The output signal of (A) circuit is 1-out-of-M code.

A. binary decoder　　B. binary encoder

C. seven-segment decoder　　D. decimal encoder

19. According to the circuit as shown in Figure 5, the output F is (B)

A. $\Sigma_{ABCD}(1, 3, 4, 6, 8, 11, 12, 13, 14)$　　B. $\Sigma_{ABCD}(1, 4, 5, 6, 8, 11, 12, 13, 14)$

C. $\Sigma_{ABCD}(1, 2, 3, 4, 9, 11, 12, 13, 14)$　　D. all above are wrong

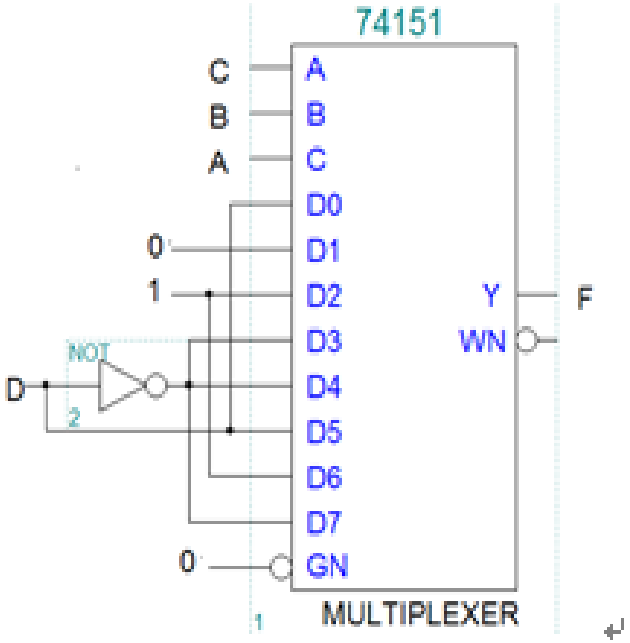


Figure 5

20. Which of the following expressions has no hazard? (B).

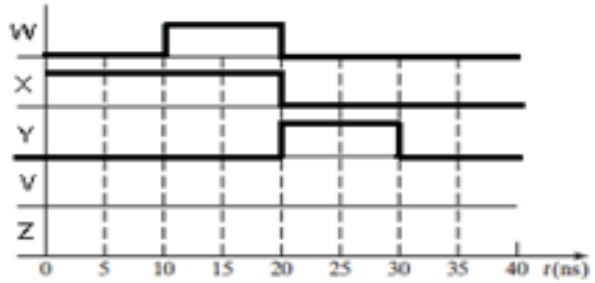
A. F=A•C+A'•D'+B•C'•D

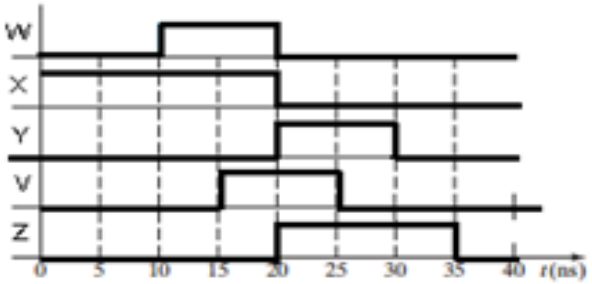
B. F=A•B+A'•D'+B•D'

C. F=A•C+A'•D'+B•C'•D+C•D'

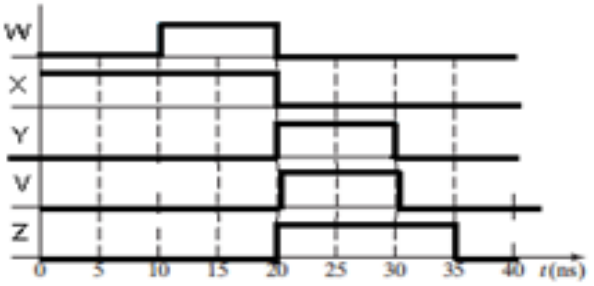
D. F=A•C+A'•D'+B•C'•D+A'•B•C'.

21. Complete the timing diagram for the given circuit. Assume that both gates have a propagation delay of 5 ns. (A).

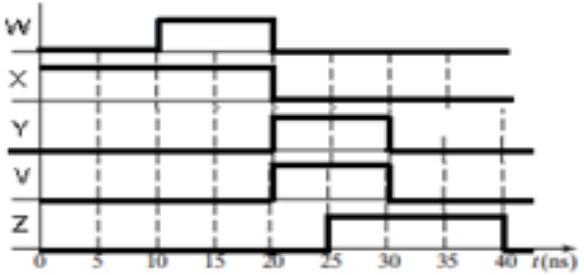




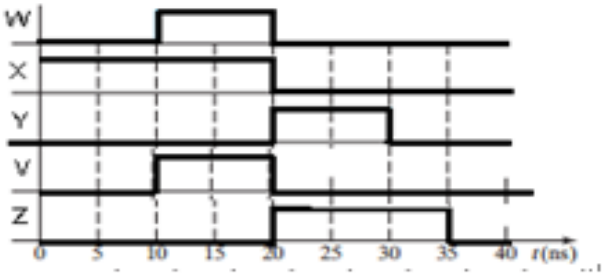
A



B.



C



D.

22. Given the circuit shown in Figure 6, when the inputs on DATA_L is 0010, the outputs DST1 and DST2 are

(D)

A. 0010, 1111 B. 0010, 0000 C. 0000, 0010 D. 1111, 0010

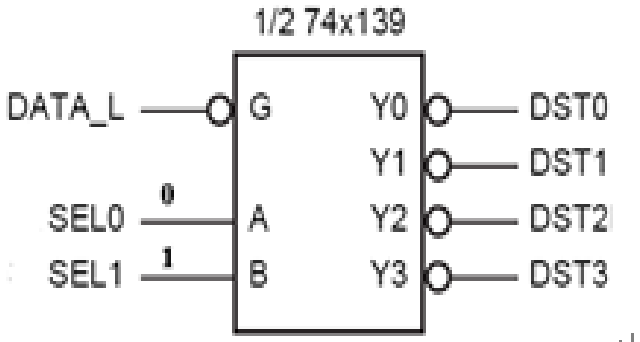


Figure 6

23. The solutions for the following logic equation ACD+BD=B+CD is (D)

A. $\sum_{A,B,C,D}(5,7,11,14,15)$ B. $\sum_{A,B,C,D}(0,1,2,8,9,10)$

C. $\sum_{A,B,C,D}(0,1,2,5,7,8,9,10,11,14,15)$ D. all above are wrong

24. The 74x148 is a MSI 8-input priority encoder that resolves priority among eight active-low inputs, I0_L-I7_L, where I7_L has the highest priority. It produces active-low address output A2_L-A0_L. The output A2-L,A1-L,A0-L of the circuit in Figure 7 is(A)

A. 001 B. 010 C. 110 D. 101

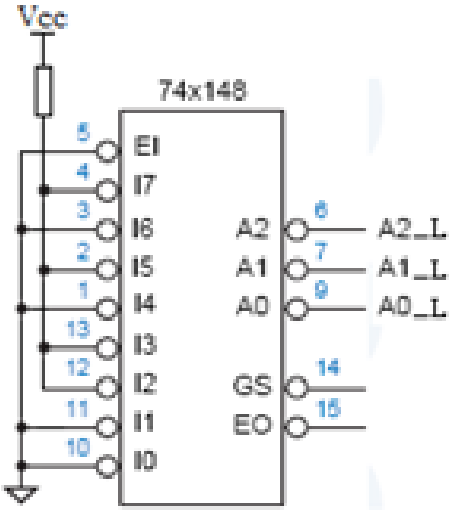


Figure 7

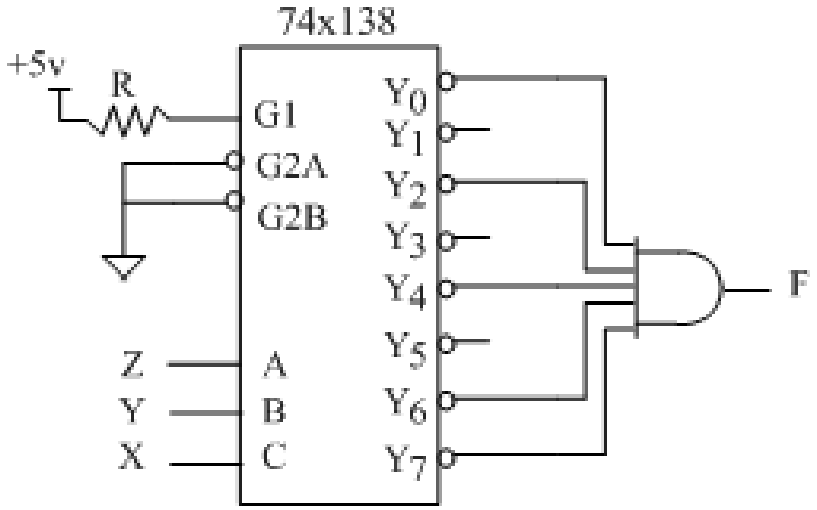


Figure 8

25. The output logic function of the circuit shown as Figure 8 can be expressed by F(X,Y,Z) =(D).

A. $\prod_{XYZ}(0,1,3,5,7)$ B. $\prod_{XYZ}(1,3,5)$ C. $\prod_{XYZ}(2,4,6)$ D. $\prod_{XYZ}(0,2,4,6,7)$

得 分

二、多项选择题（每小题4分，共20分）

下面各小题中，每小题有多个选项是正确的，请把正确选项的字母**按题号顺序填在下面的横线上。（评分标准：每小题4分，全对得4分，选得不全得2分，选项有错或不选不得分）**

Among the four options given in each question, there are multiple options that are correct. 4 points for all selections, 2 points for incomplete selections, and 0 points for wrong choices or no answers.

1. Given the circuit shown in Figure 9, its output expression F=(**A C D**).

A. F=(ABCD)'　　B. F=(AB)'·(CD)'

C. F=A'+B'+C'+D'　　D. F=((A'+B')'·(C'+D')')'

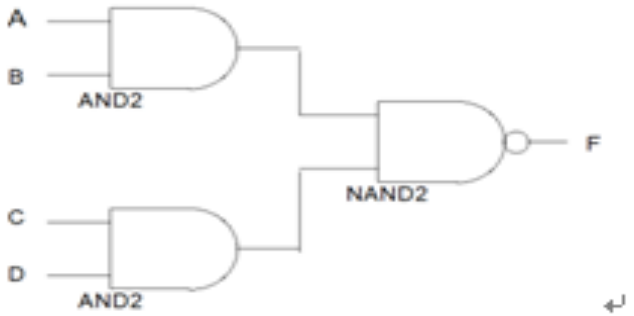


Figure 9

2. The unused inputs for CMOS NOR Gate should be connected(BC D).

A. VCC B. GND C. 0.5KΩ to GND D. Tie to the used input

3. Which statements are correct? (B C)

A. One truth table is only corresponding to one logic function and its expression

B. There is no static 1 hazards in complete sum form.

C. Two logic function can not be the same if they have different truth table.

D. There must be essential prime implicant in K-map.

4. Under minimal cost principle, which expression is the minimal sum for $F=\sum_{ABCD}(0,1,2,3,10)+d(4,5,8,11,12)$?

(A B C)

A. F= A'C'+B'C B. F= A'B'+B'C' C. F= A'B'+B'D' D. F= A'D+B'D'

5. Which statements are incorrect? (A B C D)

A. The minimal expression is the minimal form with sum of products.

B. Circuits only composed by AND, OR and NOT gates must be combinational logic circuit.

C. The sum of essential prime implicants must be the minimal sum.

D. There is only one form of the minimal sum for a logic function.

三、组合电路设计（共5分）

Combinational Circuit Design

Design a combinational circuit with a 3-bit unsigned numbers inputs A($A=A_2A_1A_0$), and a 6-bit unsigned number output Y ($Y=Y_5Y_4Y_3Y_2Y_1Y_0$), and to realize the function $Y=A^2+1$. Finished the truth table.

A_2	A_1	A_0	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	**0**	**0**	**0**	**0**	**0**	**1**
0	0	1	**0**	**0**	**0**	**0**	**1**	**0**
0	1	0	**0**	**0**	**0**	**1**	**0**	**1**
0	1	1	**0**	**0**	**1**	**0**	**1**	**0**
1	0	0	**0**	**1**	**0**	**0**	**0**	**1**
1	0	1	**0**	**1**	**1**	**0**	**1**	**0**
1	1	0	**1**	**0**	**0**	**1**	**0**	**1**
1	1	1	**1**	**1**	**0**	**0**	**1**	**0**