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密 封 线 以 内 答 题 无 效

（可以使用中文解答；禁止使用计算器；题中所用器件功能表见试卷后附录（Appendix））

题号	I	II	III	IV	V	VI	VII	合计
得分								

得 分

I. Please put the correct answers in the brackets "( )" . (2' X 10 = 20')

1. Using a 4-bit adder chip 74×283 to complete a code conversion. One addend is the 8421 BCD code, and the other addend is the binary number 0011. If the carry-input bit is 0, the sum is the (excess-3) code .

2. To complete the 4-bit two's-complement subtraction operation, X(X3X2X1X0)-Y(Y3Y2Y1Y0), using a 4-bit adder chip 74×283, we can add the two's complement of Y to X, that needs to take the bit-by-bit complement of Y and connect the carry-input bit C0 of 74×283 to (1).

3. For an even-parity code, if there are an odd number of 1s among the information bits, the parity bit should be (1).

4. The output voltage range of an 8-bit DAC is 0V~2.55V. If the DAC's output voltage is 1.29V, the corresponding input is (10000001).

5. In order to convert an 4-bit unsigned binary number to its corresponding Gray code,we need a (16*4) ROM at least.

6. The input voltage range of a 10-bit ADC is from 0V to 1V. The ADC can distinguish voltage differences as small as (0.001) V. (Three decimal digits after decimal point are required.)

7. Based on flip-flops and some logic gates, a shift register is built to periodically generate the sequence "0100101". At least (6) flip-flops are required in the shift register.

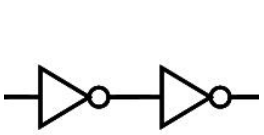
8. A ring counter consisting of four flip-flops has at most (4) states.

9. There is a state transition equation Q*= EN ⊕ Q. If we use a J-K flip-flop to implement the equation，the flip-flop's excitation equations are expressed as: J=(EN), K=(EN).

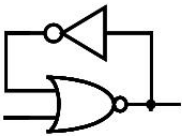
得 分

II. Choose the correct answer and fill the item number in the brackets. (2' X 3=6')

1. Which of the following circuits is NOT a combinational circuit? (B).

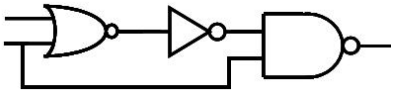


A.



B.

C.

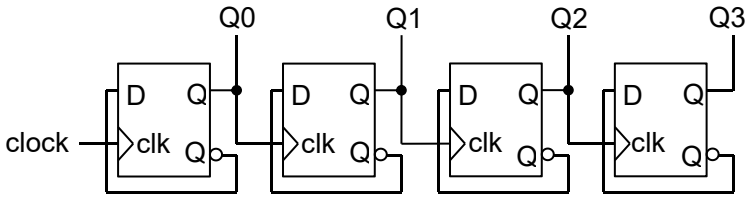


D.

2. Turn off the power and then on, the content in a ROM will（ C ）.

A. change B. be 1s C. remain unchanged D. be uncertain

3. A 4-bit ripple counter is shown as follows. Please judge which of the following descriptions is correct? (C)



A. It's a 4-bit up counter.
B. It's a 4-bit twisted-ring counter.
C. It's a 4-bit down counter.
D. It's a 4-bit ring counter.

得 分

III. Analyze the sequential circuit shown in Figure 1. (14')

(1) Write the excitation equations and the output equation. [3']

(2) Construct the transition/output table. [4']

(3) Assuming that the initial state Q1Q0=00, draw the timing diagram for Q1 ,Q0 and Z. [6']

(4) Explain the logic function of the circuit. [1']

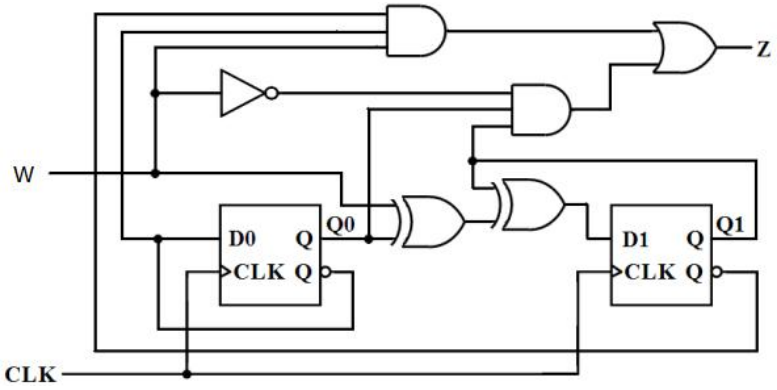
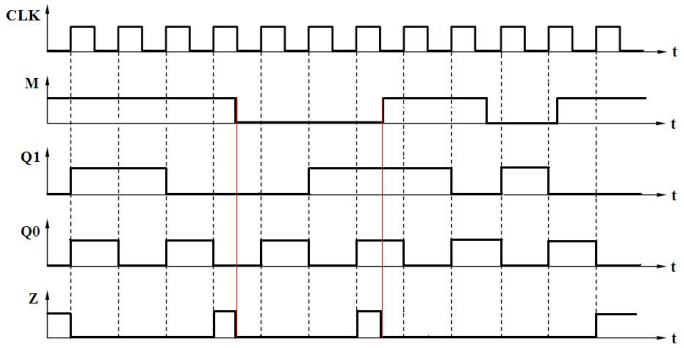


Figure 1

Transition/output table

Q1Q0	W = 0	W = 1
0 0	01, 0	11, 1
0 1	10, 0	00, 0
1 0	11, 0	01, 0
1 1	00, 1	10, 0
	Q1*Q0*, Z	



1. 激励方程: D0= Q0'（1 分），D1= X⊕Q1⊕Q0（1 分），
   输出方程 Z= MQ1'Q0'+M'Q1Q0（1 分）
2. 转移/输出表
   （每行全对得 1 分，局部错扣 0.5 分，共 4 分）
3. 时序图（Q1,Q0,Z 每个波形各 2 分，共 6 分）
4. 功能描述：模 4 加减计数器 （正确得 2 分）

得 分

IV. Design a sequence generator by a 3-bit (Q0 Q1Q2) shift-register counter. Assume that only one 74x194 , one 74x138 and one 5-input NAND gate can be used. The output Z of the circuit periodically produces the sequence “1100101”. (15’)

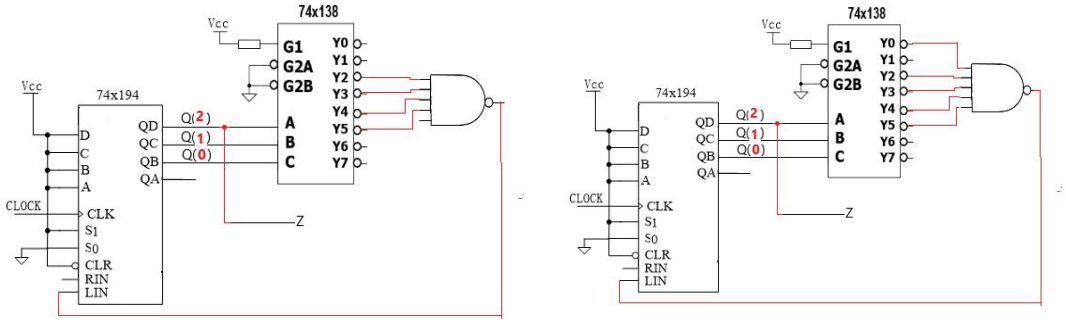
(1) Complete the table 1. (5’)

You must determine whether the input is RIN or LIN according to the circuit.

Table 1 State of counter

Q0	Q1	Q2	Input(LIN)
1	1	0	0
1	0	0	1
0	0	1	0
0	1	0	1
1	0	1	1
0	1	1	1
1	1	1	0

(2) Complete the circuit below. You also need to fill in the blanks after Q like Q(2). (8’)



self-correction

（3）Whether the circuit you designed is self-correction? (2’)

YES( )

NO( ), if It’s not ,how to modify it?

1、 一行 1 分，共 5 分，错一行扣 1 分。

2、 Q2Q1Q0 填对得 2 分，错一个扣 1 分。与非门输入正确得 4 分，错一个扣 1 分。Z 可以连 Q2Q1Q0 得任意一个，得 1 分。与非门输出连 LIN 得 1 分。

3、 回答 yes，应画图如右图。回答 NO，应画图为左图，并说明应处理 000 状态时的 LIN=1.

得 分

V. Analyze the sequential circuit shown in Figure 3. (15')

(1) Assuming that the 74x163 counter starts in state 0000, write the output sequence on QD QC QB QA for the next 8 clock ticks.

0000→ (0001) → (0010) → (0011) → (1100) → (1101) → (1110) → (1111) → (0000) [8']

(2) The modulus of this counter is 8 . [2']

(3) Write the output sequence on Z when the counter starts in state 0000.

Z=00011111 . [3']

(4) Is the circuit you designed self-correcting? [2']

YES( )

NO (√)

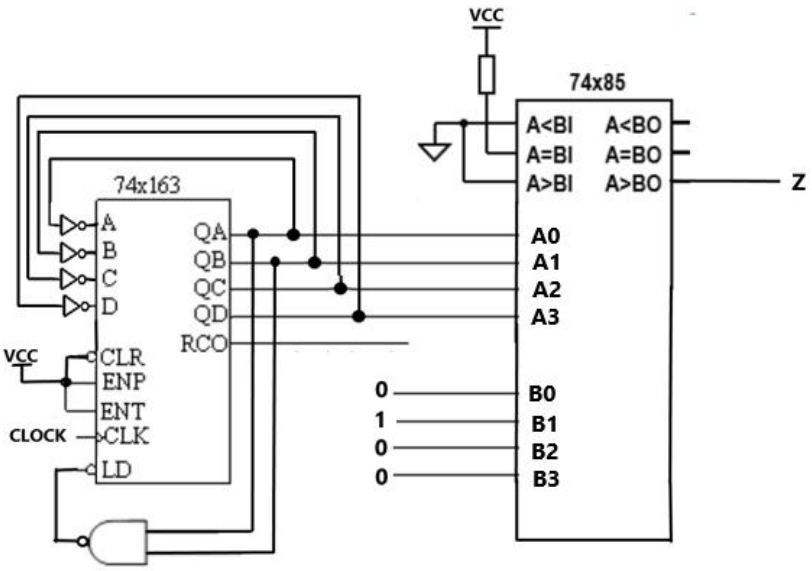


Figure 3

得 分

VI. Design a clocked synchronous state machine with the state diagram shown in Figure 4, using D flip-flops. The input is X and the output is Z. Use two state variables, Q1 Q0, with the state assignment A=00, B=01, C=10. (15’)

(1) The state machine will produce 1 on Z when the input sequence ___101___ on X is detected. [2’]

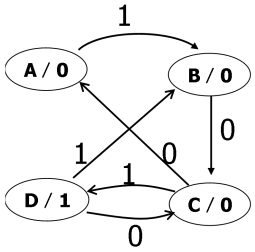
(2) Is overlap allowed for the sequence detector?(Yes or No) _____Yes_____. [1’]

(3) Assuming that the minimal-cost design approach is used, please write the excitation equations. [4’]

(4) Assuming that the invalid outputs are prohibited, please write the output equation. [2’]

(5) If the current state Q1Q0=11, the next state would be__10__when X=0, or__01__when X=1. [2’]

(6) Please redesign this state machine with the same function and make it a Moore machine. Only draw the state diagram. [4’]



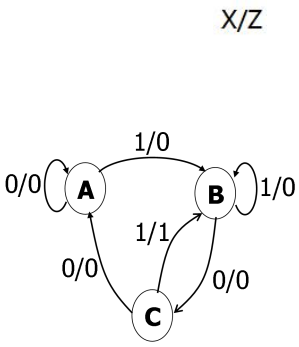


Figure 4

3. Solution:

1=Q1*=X’Q0 (2’)

D0=Q0*=X (2’)

4.Solution

Z=XQ1Q0’ (2’)

6.

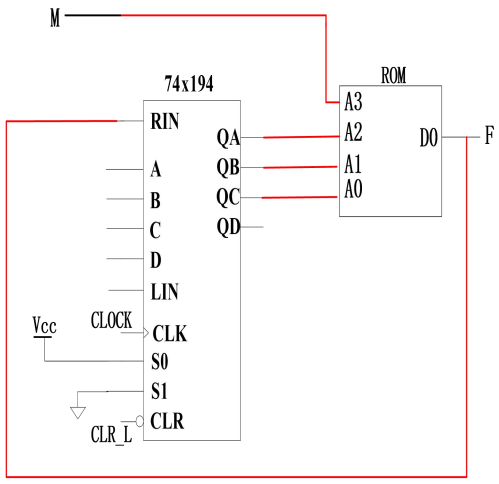
solution:

X	Q1	Q0	Q1*	Q0*	Z
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	1	d	d	0
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	0	1	1
1	1	1	d	d	0

得 分

VII. Design a periodic sequence generator **only** using one 74x194 whose "CLR" input is asynchronous, and one ROM. **M** is the control signal. If **M**=0,the output **F** produces the periodic sequence 0001011. If **M**=1,the output **F** produces the periodic sequence 110100. The generator must be self-correcting.(15')

(1) Please complete the circuit connection. [2']

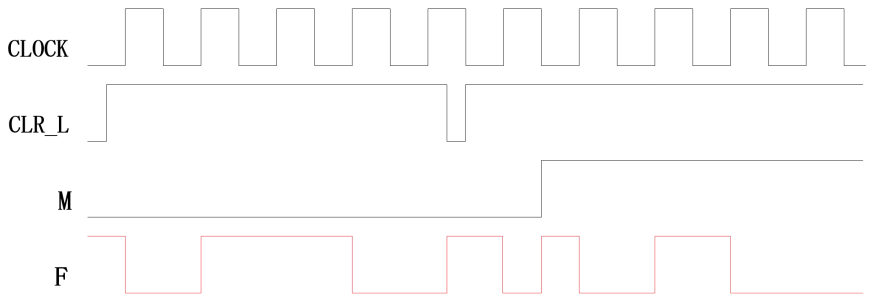


(2) Please give the content in the ROM.[8']

(

A3 A2 A1 A0	D0
0000	1
0001	0
0010	1
0011	0
0100	0
0101	1
0110	0
0111	0
1000	1
1001	1
1010	0
1011	0
1100	1
1101	0
1110	1
1111	0

(3) Complete the timing diagram below. Assume that the transition time and propagation delay of all devices in the circuit are zero.[5']



Appendix: functional tables for some integrated circuits

Function table for a 74x138 decoder

Inputs							Outputs						
G1	G2A_L	G2B_L	C	B	A	Y7_L	Y6_L	Y5_L	Y4_L	Y3_L	Y2_L	Y1_L	Y0_L
0	x	x	x	x	x	1	1	1	1	1	1	1	1
x	1	x	x	x	x	1	1	1	1	1	1	1	1
x	x	1	x	x	x	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	1	0	1	1	1	1	1
1	0	0	1	1	0	1	0	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1	1

Function table for a 74x194 4-bit universal shift register

Inputs		Next state				Function
S1	S0	QA*	QB*	QC*	QD*	
0	0	QA	QB	QC	QD	Hold
0	1	RIN	QA	QB	QC	Shift right
1	0	QB	QC	QD	LIN	Shift left
1	1	A	B	C	D	Load

Truth table for a 74x151 8-input 1-bit multiplexer

Inputs				Outputs	
EN_L	S2	S1	S0	Y	Y_L
1	x	x	x	0	1
0	0	0	0	D0	D0’
0	0	0	1	D1	D1’
0	0	1	0	D2	D2’
0	0	1	1	D3	D3’
0	1	0	0	D4	D4’
0	1	0	1	D5	D5’
0	1	1	0	D6	D6’
0	1	1	1	D7	D7’

Function table for a 74x163 4-bit binary counter

Inputs				Current State	Next state	Output
CLR_L	LD_L	ENT	ENP	Q_D Q_C Q_B Q_A	Q_D* Q_C* Q_B* Q_A*	RCO
0	X	X	X	X X X X	0 0 0 0	0
1	0	X	X	X X X X	D C B A	0
1	1	0	X	X X X X	Q_D Q_C Q_B Q_A	0
1	1	X	0	X X X X	Q_D Q_C Q_B Q_A	0
1	1	1	1	0 0 0 0	0 0 0 1	0
1	1	1	1	0 0 0 1	0 0 1 0	0
1	1	1	1	0 0 1 0	0 0 1 1	0
1	1	1	1	0 0 1 1	0 1 0 0	0
1	1	1	1	……	……..	0
1	1	1	1	1 1 1 1	0 0 0 0	1

Truth table for a 74x85 magnitude comparator

Inputs							Outputs		
A3,B3	A2,B2	A1,B1	A0,B0	A>BIN	A<BIN	A=BIN	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	0	1	0
A3=B3	A2>B2	X	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	0	1	0
A3=B3	A2=B2	A1>B1	X	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	0	1	0
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	X	X	X	A>BIN	A<BIN	A=BIN