## 电子科技大学 2020-2021 学年第 一 学期期末考试 A 卷

考试科目: 数字逻辑设计及应用 考试形式: 闭卷 考试日期: 2021年 1 月 14 日

本试卷由 六 部分构成, 共 7 页。考试时长: 120 分钟

成绩构成比例:平时成绩 60 %, 期末成绩 40 %

## (可以使用中文解答;禁止使用计算器;题中所用器件功能表见试卷后附录(Appendix))

是	页号	I	II	III	IV	V	VI	合计
得	寻分							

得分

- I. Please put the correct answers in the brackets "( )" .( 3' X 8 = 24' )
- 1. A sequential circuit with 4 flip-flops can store ( ) states at most.
- 2. A modulo-288 counter circuit can be built by ( ) 4-bit counters of 74x163 at least.
- 3. To design a "001010" serial sequence generator by shift registers, ( ) flip-flops are required at least.
- 4. There is a state transition equation  $Q^*=JQ'+K'Q$ . If we use a D flip-flop for state memory, the D input of the D flip-flop can be given as: D=(
- 5. An *n*-bit Johnson counter has ( ) abnormal states.
- 6. Two common types of ripple counter are ripple up counter and ripple down counter. The circuit shown in Figure 1-1 is a 2-bit ripple ( ) counter.
- 7. A  $74 \times 194$  can be used as a sequence detector. When Z shown in Figure 1-2 is asserted, the sequence detected is ( ).

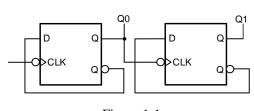


Figure 1-1

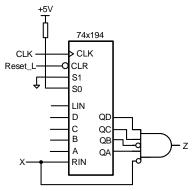


Figure 1-2

8. If a ROM has 13 address inputs and 8 data outputs, its capacity is ( )Kbyte. 得分 II. Choose the correct answer and put the item number in the brackets. (3' X 5=15') 1. Which of the following statements is correct? ( ) A. Both outputs of Mealy and Moore machine depend on states. B. The outputs of a Mealy machine depend only on the states. C. The outputs of a Moore machine depend on the inputs and states. D. Both outputs of Mealy and Moore machine depend on inputs. 2. A temperature test system whose temperature measurement range is -45°C ~125°C. If the A/D converter in the system needs to recognize a temperature change of 0.1°C, an A/D converter with ( ) bits is required at least. A. 10 B. 11 C. 12 D. 13 3. A logic diagram is shown in Figure 2 and the current state Q3Q2Q1Q0=1111. If the CONTROL terminal is connected to HIGH level and LOW level respectively, the next state Q3\*Q2\*Q1\*Q0\* should be ( ). 74×163 A. 0000 and 1111 B. 1111 and 0000 C. 0000 and 0000 D. 1111 and 1111 CLR LD ENP 4. A 4×4 unsigned binary multiplication can be built with a CONTROL ENT Q0 QΑ ( ) ROM. Q1 В QB Q2 A. 128×4  $B.256\times4$ С QC Q3 D QD C. 128×16 D.  $256 \times 8$ RCO Figure 2 5. In the following circuits, only ( ) is a sequential

logic

circuit.

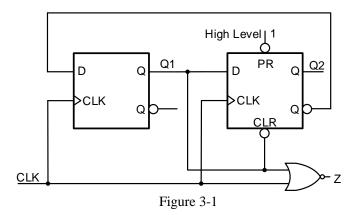
A. Three-State Buffers B. Comparators C. shift registers D. Decoders

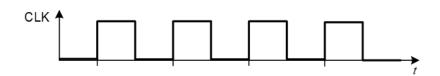


得分

III. Analyze the sequential circuit shown in Figure 3-1. (10')

- (1) Assuming the initial state Q1Q2=00, draw the timing diagrams for Q1, Q2 and Z shown in Figure 3-2. [7']
- (2) According to the frequencies of the waveforms in Figure 3-2, what is the relation between Z and CLK? [3']







**IV.** Analyze the sequential circuit shown in Figure 4. (17')

- (1) Draw the state diagram of the sequential circuit whose state is QD QC QB QA. [16']
- (2) According to the state diagram obtained from above, is the sequential circuit self-correcting or not? (  $$\ \ )$  [1']

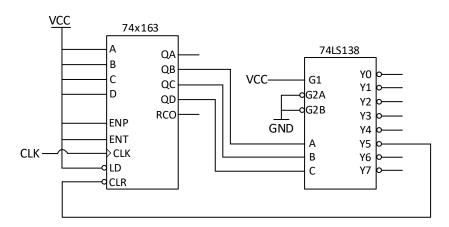


Figure 4



得分\_\_\_

- **V.** Design a clocked synchronous state machine with D flip-flops to obtain the output waveforms shown in Figure 5, where Q2, Q1 and Q0 are outputs of D flop-flops. (16')
- (1) Give the transition table of the state machine based on Figure 5. (choose the approach of minimal cost for unused states). [6']
- (2) List the unused states Q2Q1Q0 and their next states Q2\*Q1\*Q0\* to show that whether or not the circuit is self-correcting. [5']
- (3) Give the logic diagram. [5']

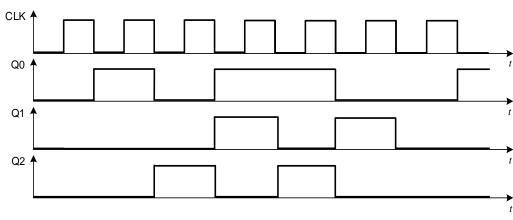


Figure 5

(2)

(3)

考场教室

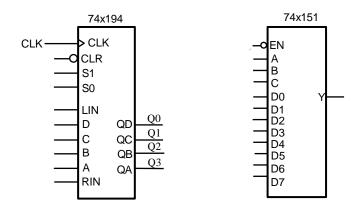
得分

**VI.** Design a "0111010001" sequence generator with a 4-bit shift register 74x194. (18')

- (1) Complete the Table 2 to realize the above sequence generator. Q3, Q2, Q1 and Q0 in Table 2 represent the corresponding signals in Figure 6. Choose the approach of minimal risk for unused states. [8']
- (2) If Q0\* is obtained by an 8-input, 1-bit multiplexer 74x151, please give the values of D0~D7 in Figure 6. [8']
- (3) Give the values of the other signals or connect them in Figure 6 to make the circuit work properly. [2']

Table 2 Transition table

Q3	Q2	Q1	Q0	Q3*	Q2*	Q1*	Q0*
0	0	0	0				
0	0	0	1	0	0	1	0
0	0	1	0	0	1	0	1
0	0	1	1				
0	1	0	0	1	0	0	0
0	1	0	1	1	0	1	1
0	1	1	0				
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	1	,			
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	1
1	1	0	0				
1	1	0	1	-			
1	1	1	0				
1	1	1	1				



## Appendix: functional tables for some integrated circuits

Function table for a 74x138 decoder

	i unction tuble for a 74x130 decoder													
		Input				Outputs								
G1	G2A_L	G2B_L	С	В	Α	Y7_L	Y6_L	Y5_L	Y4_L	Y3_L	Y2_L	Y1_L	Y0_L	
0	X	X	X	X	X	1	1	1	1	1	1	1	1	
X	1	X	X	X	X	1	1	1	1	1	1	1	1	
X	X	1	X	X	X	1	1	1	1	1	1	1	1	
1	0	0	0	0	0	1	1	1	1	1	1	1	0	
1	0	0	0	0	1	1	1	1	1	1	1	0	1	
1	0	0	0	1	0	1	1	1	1	1	0	1	1	
1	0	0	0	1	1	1	1	1	1	0	1	1	1	
1	0	0	1	0	0	1	1	1	0	1	1	1	1	
1	0	0	1	0	1	1	1	0	1	1	1	1	1	
1	0	0	1	1	0	1	0	1	1	1	1	1	1	
1	0	0	1	1	1	0	1	1	1	1	1	1	1	

Function table for a 74x194 4-bit universal shift register

Inp	outs		Nex	Function			
S1	SO	QA*	QB*	QC*	QD*	Function	
0	0	QA	QB	QC	QD	Hold	
0	1	RIN	QA	QB	QC	Shift right	
1	0	QB	QC	QD	LIN	Shift left	
1	1	A	В	C	D	Load	

Truth table for a 74x151 8-input 1-bit multiplexer

	Inpu	Outputs			
EN_L	S2	S1	S0	Y	Y_L
1	X	X	X	0	1
0	0	0	0	<b>D</b> 0	D0'
0	0	0	1	D1	D1'
0	0	1	0	D2	D2'
0	0	1	1	D3	D3'
0	1	0	0	D4	D4'
0	1	0	1	D5	D5'
0	1	1	0	D6	D6'
0	1	1	1	D7	D7'

Function table for a 74x163 4-bit binary counter

					•	
	Inputs			Current State	Next state	Output
CLR_L LD_L ENT ENP				QD QC QB QA	QD* QC* QB* QA*	RCO
0	X	X	X	XXXX	0 0 0 0	0
1	0	X	X	XXXX	D C B A	0
1	1	0	X	XXXX	Q <sub>D</sub> Q <sub>C</sub> Q <sub>B</sub> Q <sub>A</sub>	0
1	1	X	0	XXXX	QD QC QB QA	0
1	1	1	1	0 0 0 0	0 0 0 1	0
1	1	1	1	0 0 0 1	0 0 1 0	0
1	1	1	1	0 0 1 0	0 0 1 1	0
1	1	1	1	0 0 1 1	0 1 0 0	0
1	1	1	1		•••••	0
1	1	1	1	1 1 1 1	0 0 0 0	1

Truth table for a 74x85 magnitude comparator

		Outputs							
A3,B3	A2,B2	A1,B1	A0,B0	A>BIN	A <bin< td=""><td>A=BIN</td><td>A&gt;B</td><td>A<b< td=""><td>A=B</td></b<></td></bin<>	A=BIN	A>B	A <b< td=""><td>A=B</td></b<>	A=B
A3>B3	X	X	X	X	X	X	1	0	0
A3 <b3< td=""><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td><td>0</td></b3<>	X	X	X	X	X	X	0	1	0
A3=B3	A2>B2	X	X	X	X	X	1	0	0
A3=B3	A2 <b2< td=""><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td><td>0</td></b2<>	X	X	X	X	X	0	1	0

A3=B3	A2=B2	A1>B1	X	X	X	X	1	0	0
A3=B3	A2=B2	A1 <b1< td=""><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td><td>0</td></b1<>	X	X	X	X	0	1	0
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	1	0	0
A3=B3	A2=B2	A1=B1	A0 <b0< td=""><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td><td>0</td></b0<>	X	X	X	0	1	0
A3=B3	A2=B2	A1=R1	A0=B0	X	X	X	A>RIN	A <bin< td=""><td>A=RIN</td></bin<>	A=RIN