TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T6A04A

Column and Row Driver LSI for a Dot Matrix Graphic LCD

The T6A04A is a driver for a small-to-medium-sized scale dot matrix graphic LCD. It includes the functions of the T9841B (column driver) and the T9842B (row driver). It has an 8-bit interface circuit and can be operated with an 80-Series MPU. It generates all the timing signals for the display with an on-chip oscillator. It receives 8-bit data from an MPU, latches the data to an on-chip RAM, and displays the image on the LCD (the data in the display RAM correspond to the dots on the display). The device has 120 column driver outputs and 64 row driver outputs enabling it to drive a 120-dot by 64-dot LCD. In addition, there are resistors to divide the bias voltage, a power supply op-amp, DC-DC converter (+5 V →−5 V) and contrast control circuit, enabling the LCD to be driven by a single power supply. The device can be connected to another T6A04A to drive a 240-dot by 64-dot LCD.

Unit: mm

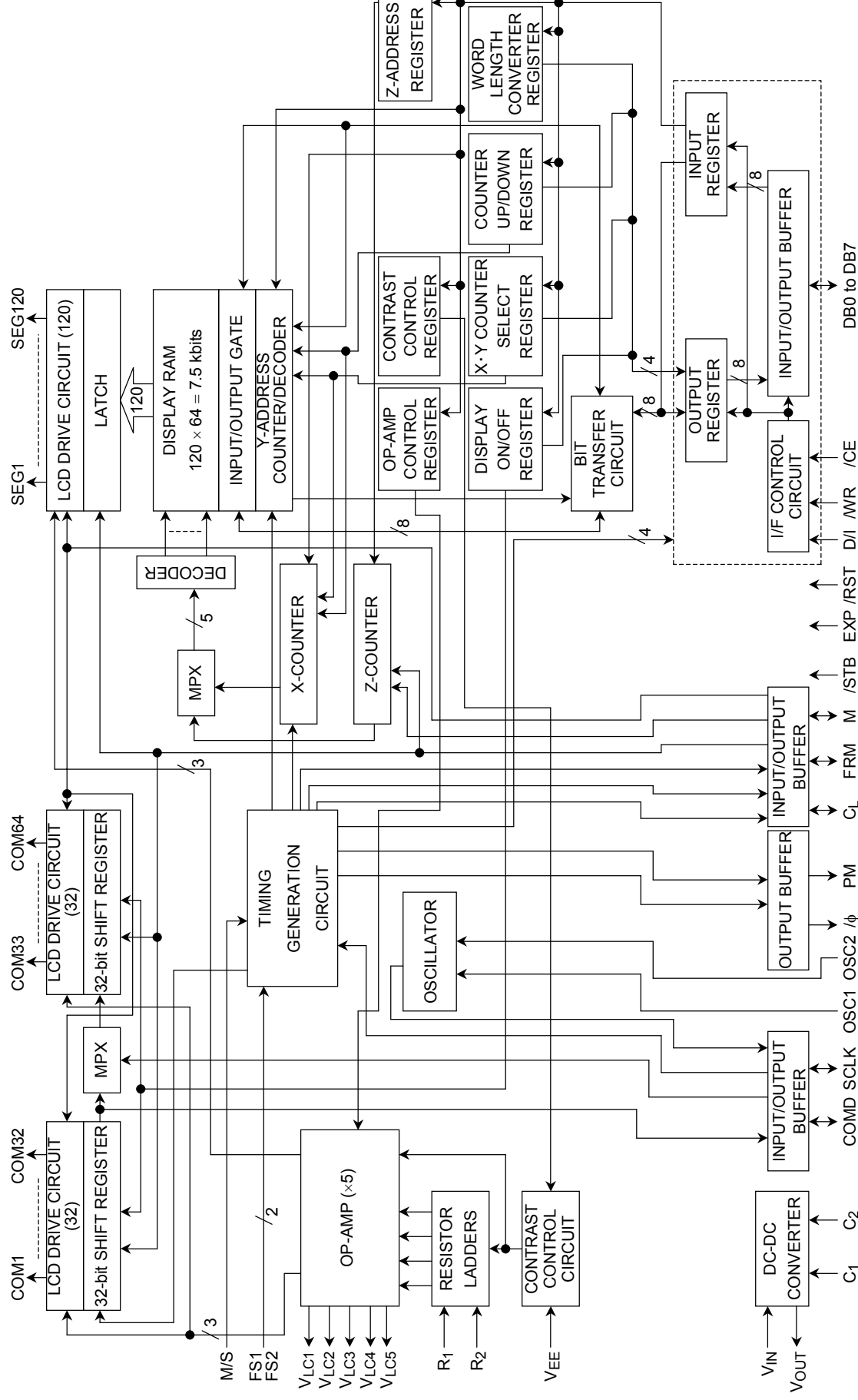| T6A04A	Lead Pitch	
	IN	OUT
(UAW, 6NS)	1.0	0.28
(UEM, 7NS)	0.4	0.4

Please contact Toshiba or an authorized Toshiba dealer for information on package dimensions.
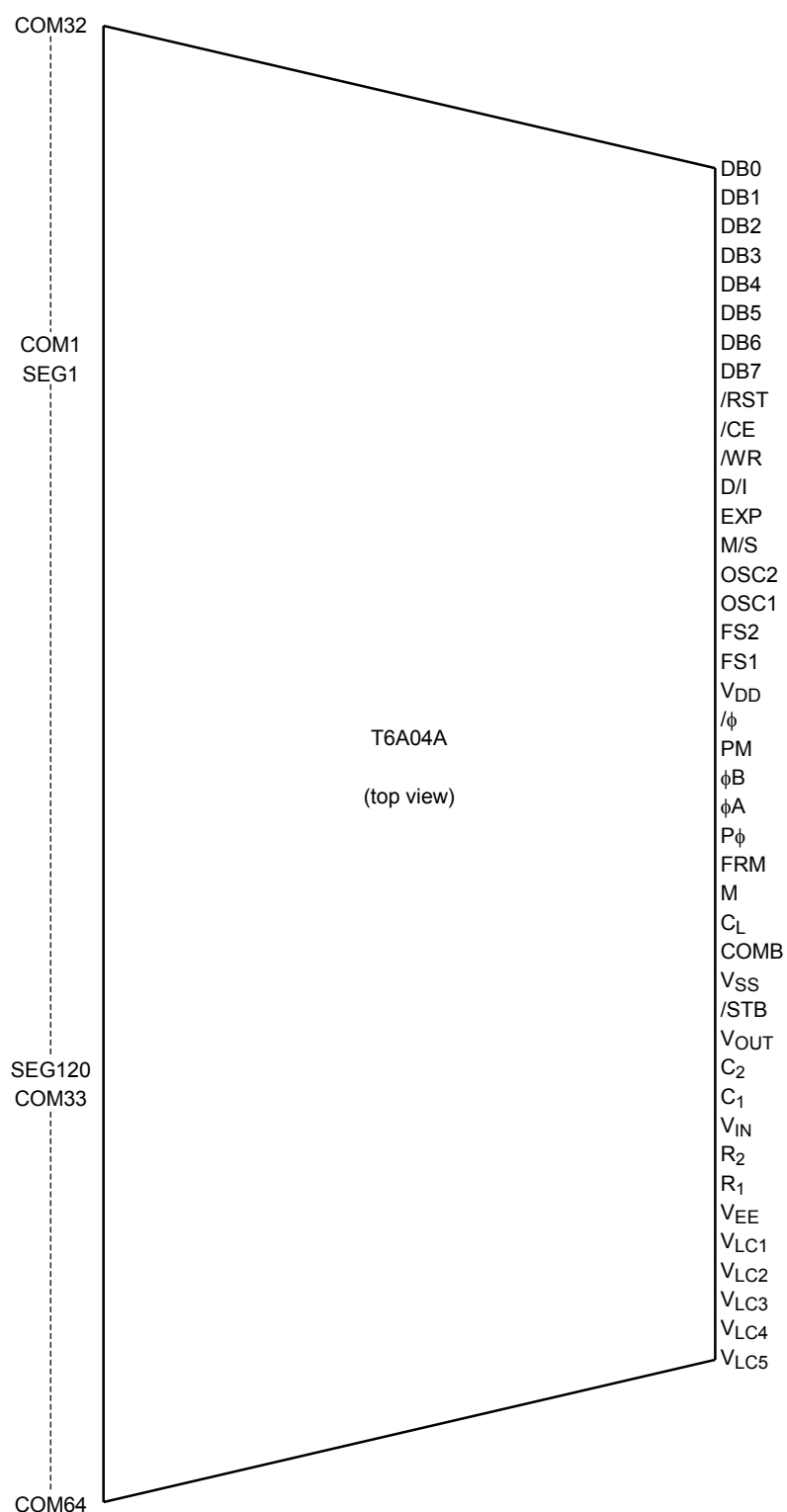
TCP (Tape Carrier Package)

Features

- On-chip display RAM capacity : $120 \times 64 = 7.5$ kbits
- Display RAM data
  (1) Display data = 1.................. LCD turns on.
  (2) Display data = 0.................. LCD turns off.
- 1/64 duty cycle
- Word length of display data can be switched between eight bits and six bits according to the character font.
- LCD driver outputs : 120 column driver outputs and 64 row driver outputs
- Interface with 80-series MPU
- On-chip oscillator with one external resistor
- Low power consumption
- On-chip resistors to divide bias voltage, on-chip operational amplifier for LCD supply, on-chip DC-DC converter, on-chip contrast control circuit
- CMOS process
- Operating voltage : 4.5 to 5.5 V
- Operating voltage for LCD drive signal : $V_{DD} - V_{EE} = 16.0$ V (max)
- Package : TCP (tape carrier package)

2002-03-06

Block Diagram

Pin Assignment

Pin assignment diagram, T6A04A (top view).

Left side pins (top to bottom): COM32, COM1, SEG1, SEG120, COM33, COM64

Right side pins (top to bottom): DB0, DB1, DB2, DB3, DB4, DB5, DB6, DB7, /RST, /CE, /WR, D/I, EXP, M/S, OSC2, OSC1, FS2, FS1, V_{DD}, /ϕ, PM, ϕB, ϕA, Pϕ, FRM, M, C_L, COMB, V_{SS}, /STB, V_{OUT}, C_2, C_1, V_{IN}, R_2, R_1, V_{EE}, V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4}, V_{LC5}

Note 1: The above diagram shows the pin configuration of the LSI chip; it does not show the configuration of the tape carrier package.

Pin Functions

Pin Name	I/O	Functions
SEG1 to SEG120	Output	Column driver output
COM1 to COM64	Output	Row driver output • Disable expansion mode (EXP = L, M/S = H) → COM1 to COM64 are enabled. • Enable expansion mode/master mode (EXP = H, M/S = H) → COM1 to COM32 are enabled and COM33 to COM64 are disabled. • Enable expansion mode/slave mode (EXP = H, M/S = L) → COM1 to COM32 are disabled and COM33 to COM64 are enabled.
C_L	I/O	Input/output for shift clock pulse • Master mode (M/S = H) → Output • Slave mode (M/S = L) → Input
M	I/O	Input/output for frame signal • Master mode (M/S = H) → Output • Slave mode (M/S = L) → Input
FRM	I/O	Input/output for display synchronous signal • Master mode (M/S = H) → Output • Slave mode (M/S = L) → Input
$P\phi$, ϕA, ϕB	I/O	Input/output system clock signal • Master mode (M/S = H) → Output • Slave mode (M/S = L) → Input
COMD	I/O	Input/output row signal data • Master mode (M/S = H) → Output • Slave mode (M/S = L) → Input
DB0 to DB7	I/O	Data bus
D/I	Input	Input for data/instruction select signal • D/I = H → indicates that the data on DB0 to DB7 is display data. • D/I = L → indicates that the data on DB0 to DB7 is control data.
/WR	Input	Input for write select signal • /WR = H → Read selected • /WR = L → Write selected
/CE	Input	Input for chip enable signal • /WR = L → Data on DB0 to DB7 is latched on the rising edge of /CE. • /WR = H → Data appears at DB0 to DB7 while /CE is Low.
/RST	Input	Input for reset signal • /RST = L → Reset state
/STB	Input	Input for standby signal • Usually connected to V_{DD} • /STB = L → T6A04A is in standby state and cannot accept any commands or data. Column driver signal and row driver signal are at the V_{DD} level
FS1, FS2	Input	Input for frequency selection
EXP	Input	Input for expansion mode selection • M/S = H → enables expansion mode. Two chips can be used together. • M/S = L → disables expansion mode.

Pin Name	I/O	Functions
M/S	Input	Input for master/slave selection ● M/S = H → T6A04A is master chip. ● M/S = L → T6A04A is slave chip.
OSC1, OSC2	—	When using the internal clock oscillator, connect a resistor between OSC1 and OSC2. When using an external clock, connect the clock as input to OSC1 and leave OSC2 open.
R_1, R_2	—	Input for LCD drive bias selection ● LCD drive bias selection is shown in the following table $\begin{array}{\|c\|c\|c\|} \hline R_2 & R_1 & \text{Bias} \\ \hline 0 & 0 & 1/6 \\ \hline 0 & 1 & 1/7 \\ \hline 1 & 0 & 1/8 \\ \hline 1 & 1 & 1/9 \\ \hline \end{array}$
C_1, C_2	—	Connected by a capacitor for DC-DC converter
V_{IN}	—	Input for DC-DC converter. Connect to V_{DD}.
V_{OUT}	—	DC-DC converter output
V_{EE}	—	Power supply for LCD driver circuit ● When using on-chip DC-DC converter, connect V_{EE} to V_{OUT}
V_{LC1} to V_{LC5}	—	Power supply for LCD driver circuit ● M/S = H → bias voltage output ● M/S = L → bias voltage input
V_{DD}	—	Power supply for logic circuit
V_{SS}	—	Ground: Reference
PM	—	Pre-frame signal for Toshiba T9841B
/ϕ	—	Output system clock for Toshiba T9841B

2002-03-06

Function of Each Block

- Interface logic

    The T6A04A can be operated with an 80-Series MPU.
    Figure 1 shows an example of the interface.

```
        A0  ─────────────────────►  D/1
     /IORQ  ─────────────────────►  /CE
      /WR   ─────────────────────►  /WR
    <MPU>                           <T6A04A>
  D0 to D7  ◄────────────────────►  DB0 to DB7
   /RESET   ─────────────────────►  /RST
```
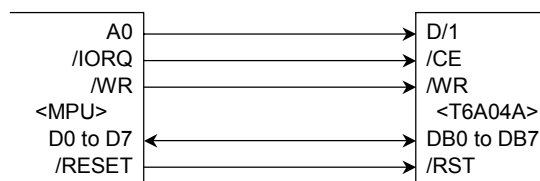
Figure 1

- Input register

    This register stores 8-bit data from the MPU. The D/I signal distinguishes between command data and display data.

- Output register

    This register stores 8-bit data from the display RAM. When display data is read, the display data specified by the address in the address counter is stored in this register. After that, the address is automatically incremented or decremented. Therefore, when an address is set, the correct data does not appear as the first data item that is read. The data in the specified address location appears as the second data item that is read.

- X-address counter

    The X-address counter is a 64-up/down counter. It holds the row address of a location in the display RAM. Writing data to or reading data from the display RAM causes the X-address to be automatically incremented or decremented.

- Y-(page) address counter

    The Y-(page) address counter is either a 15-up/down counter, when the word length is eight bits, or a 20-up/down counter, when the word length is six bits. It holds the column address of a location in the display RAM. Writing data to or reading data from the display RAM causes the Y-address to be automatically incremented or decremented.

- Z-address counter

    The Z-address counter is a 64-up counter that provides the display RAM data for the LCD drive circuit. The data stored in the Z-address register is sent to the Z-address counter as the Z start address.
    For instance, when the Z start address is 32, the counter increments as follows: 32, 33, 34 ..., 62, 63, 0, 1, 2 ... 30, 31, 32. Therefore, the display start line is line 32 of the display RAM.

- Up/down register

    The 1-bit datum stored in this register selects either Up or Down mode for the X-and Y-(page) address counters.

- Counter select register

    The 1-bit datum stored in this register selects the X-address counter or Y-(page) address counter.

- Display ON/OFF register

    This 1-bit register holds the display ON/OFF state. In the OFF state, the output data from the display RAM is cleared. In the ON state, the display RAM data is displayed. The display ON/OFF state does not affect the data in the display RAM.

- Z-address register

    This 6-bit register holds the data which specifies the display start line. The data is loaded into the Z-address counter on the FRM signal. Using the Z-address register, vertical scrolling is possible.

- Word length register

    The 1-bit datum stored in this register selects the word length: eight bits per word or six bits per word.

- Word length change circuit

    This circuit is controlled by the word length register. when the word length is eight bits, data is transferred eight bits at a time. When the word length is six bits, the data transfer method is shown in Figure 2 as follows:
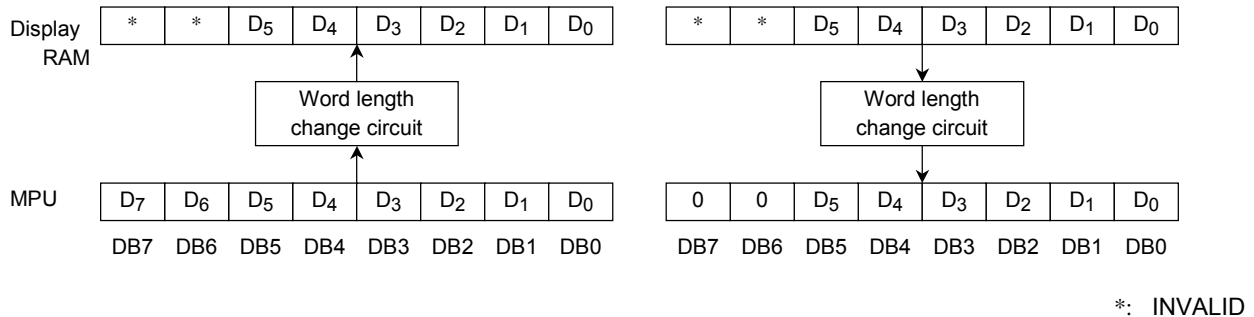
Display RAM	*	*	D_5	D_4	D_3	D_2	D_1	D_0

Word length change circuit

MPU	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

	*	*	D_5	D_4	D_3	D_2	D_1	D_0

Word length change circuit

	0	0	D_5	D_4	D_3	D_2	D_1	D_0

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

*: INVALID

Figure 2

- Oscillator

    The T6A04A includes an on-chip oscillator. When using this oscillator, connect an external resistor between OSC1 and OSC2, as shown in Figure 3. When using an external clock, connect the clock input to OSC1 and leave OSC2 open.
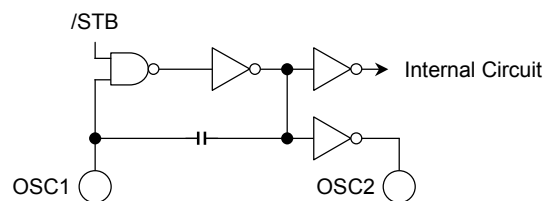
/STB

OSC1   OSC2   Internal Circuit

Figure 3

- Timing generation circuit

    This circuit divides the signals from the oscillator and generates the display timing signals and the operating clock signal.

- Shift register

    The T6A04A has two 32-bit shift registers. In disable expansion mode, both the shift registers are enabled. These two 32-bit shift registers can be combined to form a 64-bit shift register. In enable expansion mode the 32-bit shift register for COM1 to COM32 is enabled in master chip mode, and the 32-bit shift register for COM33 to COM64 is enabled in slave chip mode.

- Latch circuit

    The latch circuit latches data from the display RAM on the rising edge of the C_L signal.

- Column driver circuit

    The column driver circuit consists of 120 driver circuits. One of the four LCD driving levels is selected by the combination of the M signal and the display data transferred from the latch circuit. Details of the column driver circuit are shown in Figure 4.
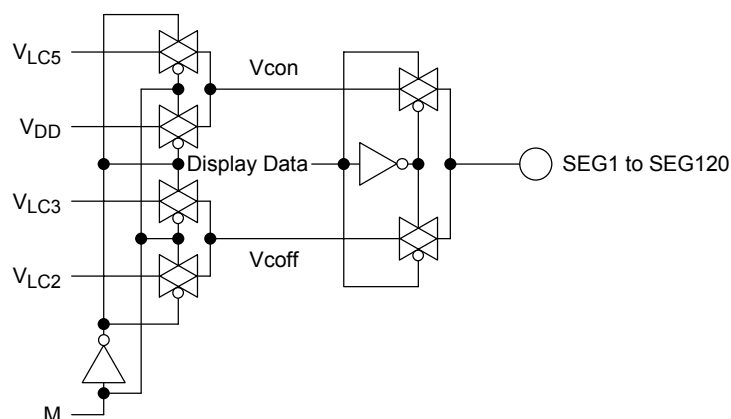

Figure 4

- Row driver circuit

    The row driver circuit consists of 64 driver circuits. One of the four LCD driving levels is selected by the combination of the M signal and the data from the shift-register. Details of the row driver circuit are shown in Figure 5.
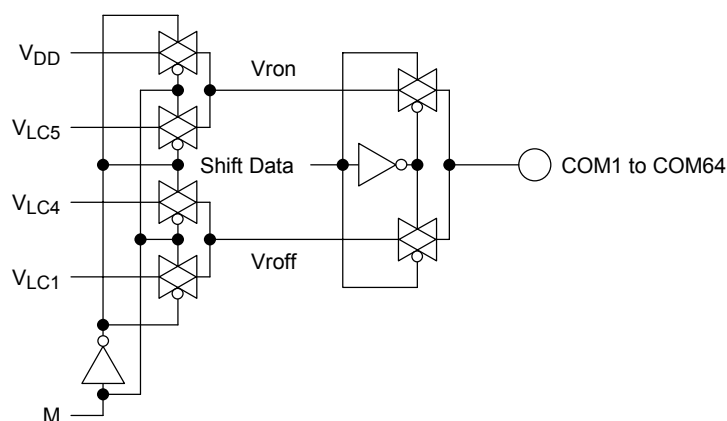

Figure 5

- DC-DC converter

   The T6A04A has an on-chip DC-DC converter. When +5 V is applied to V_{IN}, the DC-DC converter generates −5 V at V_{OUT}. The voltage from V_{OUT} will drop due to the load current for V_{EE}.

   This characteristic is defined in "Electrical Characteristics".

   Normally the value of external capacitors is 1.0 μF; this value may need some adjustment according to the application. When the T6A04A is in standby state, $V_{OUT} = 0$ V. See Figure 6.
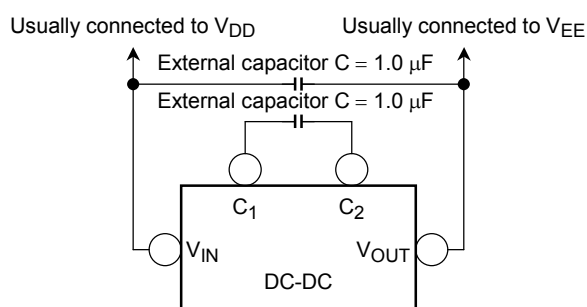

Figure 6

When using an external power supply, input the voltage to V_{EE} and leave the C_1, C_2 V_{OUT} pins open.

- Voltage divider resistors, contrast control circuit

The T6A04A has on-chip resistors which include op-amps, that divide the bias voltage, and a contrast control circuit. The voltage bias is modified by the values of R_1 and R_2. One of four biases can be selected. These resistors and the contrast control circuit are shown in Figure 7 below.
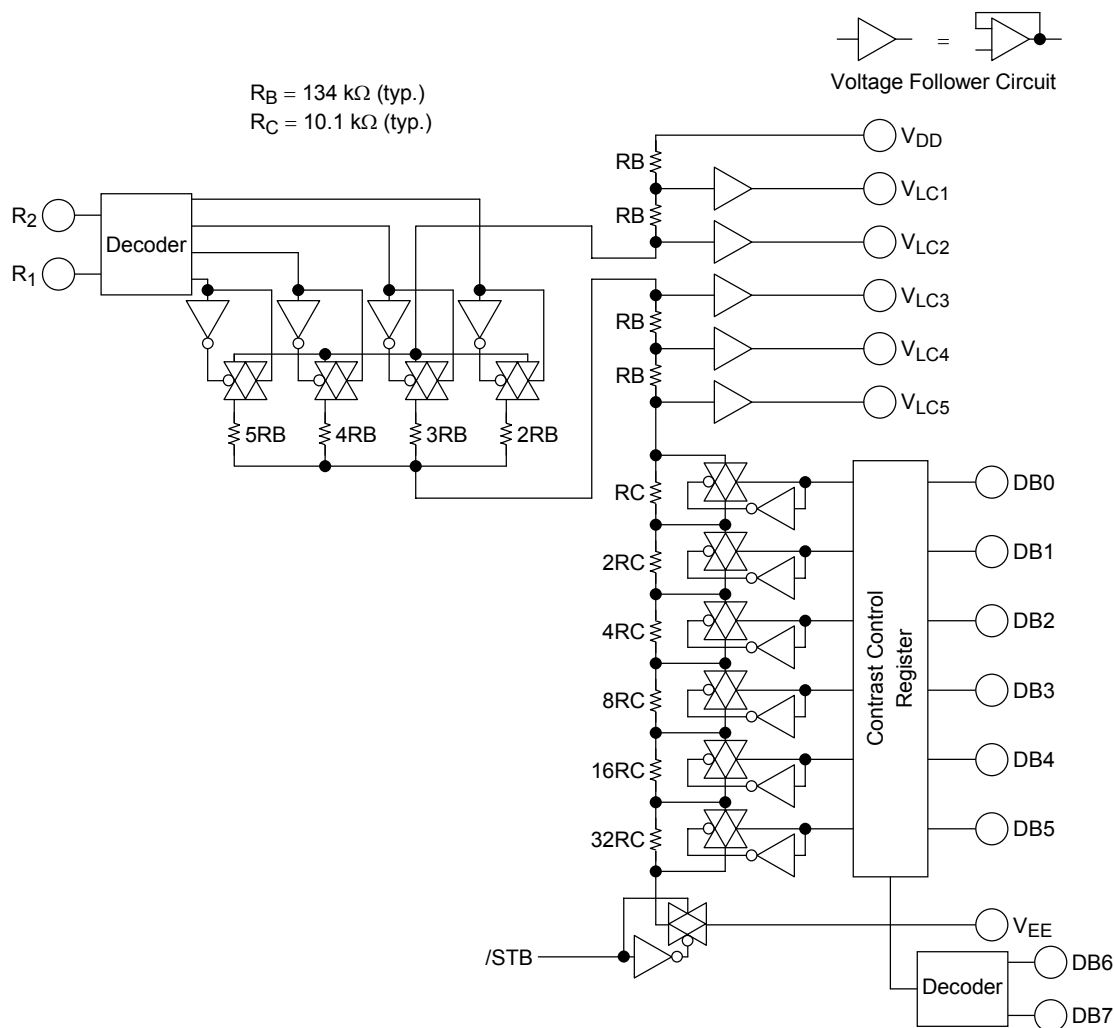

Figure 7

- Op-amp, op-amp control register

The T6A04A has five operational amplifiers which determine the LCD driving level. The power supplied by these op-amps is modified by the contents of the op-amp control register to match the LCD panel. The op-amp can also be controlled in such a way that it supplies full current on the rising edge of C_L and a reduced current otherwise.

To maintain good LCD contrast, connect a capacitor between the op-amp output and V_{DD}. The value of the capacitor should normally be in the range 0.1 to 1.0 μF.

- Display RAM

    The display RAM consists of 64 rows × 120 columns for a total of 7680 cells. It is directly bit-mapped to the LCD. The relation between the display RAM and LCD is shown in Figure 8.

    When the word length is set to eight bits, the display RAM is arranged in 15 pages and each page contains 64 words. When the word length is set to six bits, the display RAM is arranged in 20 pages and each page contains 64 words. See Figure 8.
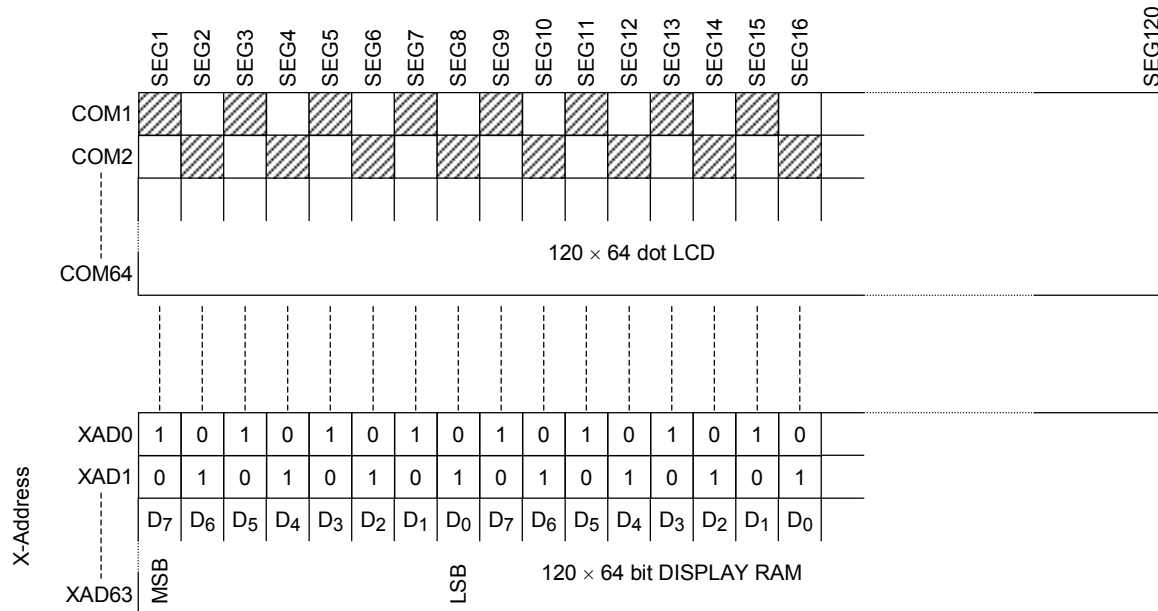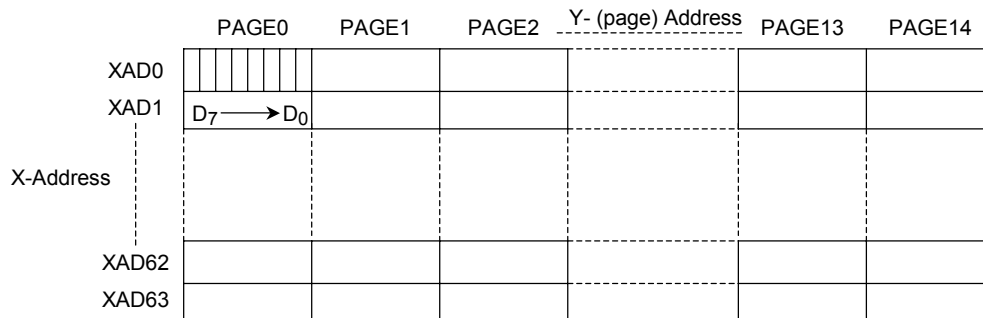

Figure 8

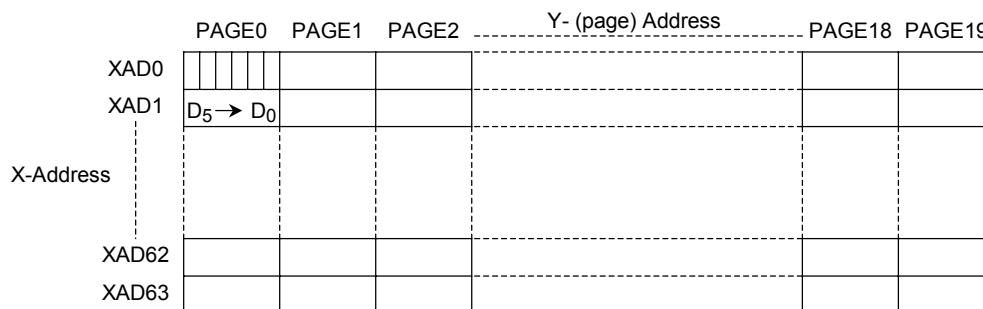(1)   8-bits-per-word mode

(2)   6-bits-per-word mode

Figure 9

Command Definitions

Command Name	D/I	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
DPE	0	0	0	0	0	0	0	0	1	1/0	Display ON (1)/OFF (0)
86E	0	0	0	0	0	0	0	0	0	1/0	Word Length: 8 bits (1)/6 bits (0)
UDE	0	0	0	0	0	0	0	1	1/0	1/0	Counter Select : DB1 Y (1)/X (0) Mode Select : DB0 UP (1)/DOWN (0)
CHE	0	0	0	0	0	1	1	*	*	*	Test Mode Select
OPA1	0	0	0	0	0	1	0	*	1/0	1/0	Op-amp Power Control 1
OPA2	0	0	0	0	0	0	1	*	1/0	1/0	Op-amp Power Control 2
SYE	0	0	0	0	1	Y-(page) Address (0 to 19)					Y-(page) Address Set
SZE	0	0	0	1	Z-Address (0 to 63)						Z-Address Set
SXE	0	0	1	0	X-Address (0 to 63)						X-Address Set
SCE	0	0	1	1	CONTRAST CONTROL (0 to 63)						Contrast Set
STRD	0	1	B	8/6	D	R	0	0	Y/X	U/D	Status Read
DAWR	1	0	Write Data								Display Data Write
DARD	1	1	Read Data								Display Data Read

∗: INVALID

- Display ON/OFF select (DPE)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	0	1	1	Display ON (03H)
0	0	0	0	0	0	0	0	1	0	Display OFF (02H)

This command turns display ON/OFF. It does not affect the data in the display RAM.

Note 2: An L input on /RST turns display OFF.

- Word length 8 bits/6 bits select (86E)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	0	0	1	8 Bits/Word Mode (01H)
0	0	0	0	0	0	0	0	0	0	6 Bits/Word Mode (00H)

This command sets the word length for display RAM data to eithers six bits or eight bits.

Note 3: An L input on /RST sets the word length to eight bits per word.

- X/Y (page) counter, up/down mode select (UDE)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	1	0	0	X-Counter/Down Mode (04H)
0	0	0	0	0	0	0	1	0	1	X-Counter/Up Mode (05H)
0	0	0	0	0	0	0	1	1	0	Y-Counter/Down Mode (06H)
0	0	0	0	0	0	0	1	1	1	Y-Counter/Up Mode (07H)

This command selects the counter and the up/down mode. For instance, when X-counter/up mode is selected, the X-address is incremented in response to every data read and write. However, when X-counter/up mode is selected, the address in the Y-(page) counter will not change. Hence the Y-address must be set (with the SYE command) before it can be changed.

Note 4: An L input to /RST sets the Y-counter to up mode.

- Test mode select (CHE)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	1	1	*	*	*	*: INVALID

This command selects the test mode. Do not use this command.

- Set Y-(page) address (SYE)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	A	A	A	A	A

Range: 8-bit/Word: 20H to 2EH (page 0 to page 14)
        6-bit/Word: 20H to 33H (page 0 to page 19)
When operating in 8-bits-per-word mode, this command selects one of the 15 pages from the display RAM. (Do not try to select a page outside this range.) When operating in 6-bits-per-word mode, this command selects one of the 20 pages from the display RAM.

Note 5: An L input to /RST sets the Y-address to page 0.

- Set Z-address (SZE)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	A	A	A	A	A	A

Range: 40H to 7FH (ZAD0 to ZAD63)
This command sets the top row of the LCD screen, irrespective of the current X-address. For instance, when the Z-address is 32, the top row of the LCD screen is address 32 of the display RAM, and the bottom row of the LCD screen is address 31 of the display RAM.

Note 6: An L input to /RST sets the Z-address to 0.

- Set X-address (SXE)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	A	A	A	A	A	A

Range: 80H to BFH (XAD0 to XAD63)
   This command sets the X-address (in the range 0 to 63). An L input to /RST sets the X-address to 0.

- Set contrast (SCE)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	A	A	A	A	A	A

Range: C0H to FFH
   This command sets the contrast for the LCD. The LCD contrast can be set in 64 steps. The command C0H selects the brightest level; the command FFH selects the darkest.

- Op-amp control 1 (OPA1)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	*	A	A

∗: INVALID

Range: 10H to 13H (when DB2 = 0)
   This command sets the power supply strength for the operational amplifier. This command selects one of four levels. The command 10H selects the lowest power supply strength and the command 13H selects the maximum strength.

Note 7:   An L input to /RST sets the op-amp power supply strength to the lowest level.
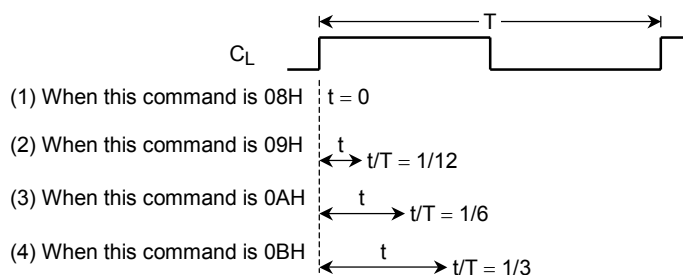
- Op-amp control 2 (OPA2)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	*	A	A

∗: INVALID

Range: 08H to 0BH (when DB2 = 0)
   This command enhances the power supply strength of the operational amplifier over a short period from the rising edge of C_L. This command selects one of four levels of strength.

Note 8:   An L input to /RST sets t to 0 for op-amp. See Figure 10.

The amplifier's strength is enhanced over the period denoted by ↔, starting on the rising edge of C_L.

Figure 10

- Status read (STRD)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	B	8/6	D	R	0	0	Y/X	U/D

B (busy) : When B is 1, the T6A04A is executing an internal operation and no instruction can be accepted except STRD.
When B is 0, the T6A04A can accept an instruction.

8/6 (word length) : When 8/6 is 1, the word length of the display data is eight bits per word.
When 8/6 is 0, the word length of the display data is six bits per word.

D (display) : When D is 1, display is ON.
When D is 0, display is OFF.

R (reset) : When R is 1, the T6A04A is in reset state.
When R is 0, the T6A04A is in operating state.

Y/X (counter) : When Y/X is 1, the Y counter is selected.
When Y/X is 0, the X counter is selected.

U/D (up/down) : When U/D is 1, the X and Y counters are in up mode.
When U/D is 0, the X and Y counters are in down mode.

- Write/read display data (DAWR/DARD)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	1	D	D	D	D	D	D	D	D	DAWR: Display Data Write
1	1	D	D	D	D	D	D	D	D	DARD: Display Data Read

The command DAWR writes the display data to the display RAM. The command DARD outputs the display data from the display RAM. However, when a data read is executed, the correct data does not appear on the first data reading. Therefore, ensure that the T6A04A performs a dummy data read before reading the actual data.

Function Description

- X-address counter and Y-(page) address counter

    Figure 11-1 shows a sample operation involving the X-address counter.

    After Reset is executed, the X-address (XAD) becomes 0, then X-counter/up mode is selected. Next, the X-address is set to 62 using the SXE command.

    After data has been written or read, the X-address is automatically incremented by 1.

    After X-counter/down mode has been selected and data has been written or read, the X-address is automatically decremented by 1.

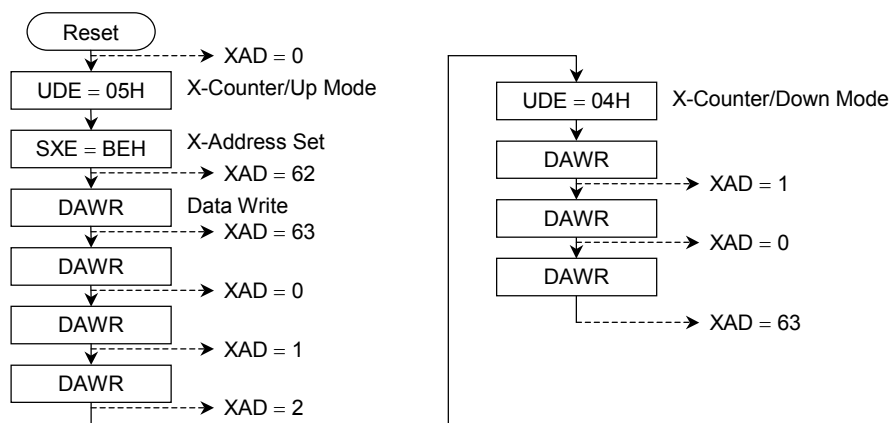   When the X-counter is selected, the Y-counter is not incremented or decremented.

Figure 11-1

    Figure 11-2 shows a sample operation involving the Y-address counter in 8-bit word length mode.

    After Reset is executed, the Y-(page) address (page) becomes 0, then Y-(page) counter/up mode and 8-bit word length mode are selected. After data has been written or read, the Y-(page) address counter is automatically incremented by 1.

    After Y-(page) counter/down mode has been selected and data has been written or read, the Y-(page) address is automatically decremented by 1.

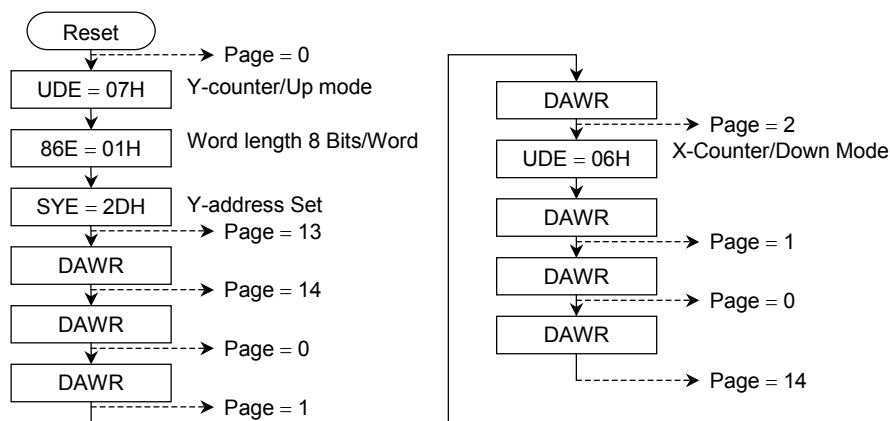   When the Y-(page) counter is selected, the X-counter is not incremented or decremented.

Figure 11-2

    When operating in 6-bit word length mode, the Y-(page) address counter can court up to 19.
    If Page = 18 in up mode, after data has been written or read, the Y-(page) address (page) becomes 0.
    If Page = 0 in down mode, after data has been written or read, the Y-(page) address (page) becomes 18.

- Data read

  When reading data, there are some cases when dummy data must be read. This is because when the data read command invoked, the data pointed to by the address counter is transferred to the output register; the contents of the output register are then transferred by the next data read command.

  Therefore when reading data straight after power-on or straight after an address-setting command, such as SYE or SXE, a dummy data read must be performed. See Figure 12.
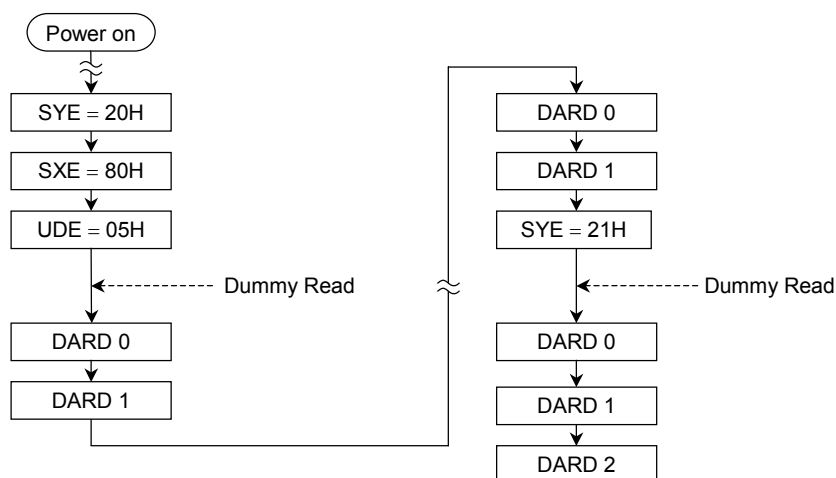

Figure 12

- Reset function

  When /RST = L, the reset function is executed and the following settings are mode.
  - (3) Display ....OFF
  - (4) Word length.............................8 bits/word
  - (5) Counter mode..........................Y-counter/up mode
  - (6) Y-(page) address......................Page = 0
  - (7) X-address ....XAD = 0
  - (8) Z-address................................ZAD = 0
  - (9) Op-amp1 (OPA1).....................min
  - (10) Op-amp2 (OPA2).....................min

- Standby function

  When /STB = L, the T6A04A is in standby state. The internal oscillator is stopped, power consumption is reduced, and the power supply level for the LCD (V_{LC1} to V_{LC5}) becomes V_{DD}.

- Busy flag

  When the T6A04A is executing an internal operation (other than the STRD command), the busy flag is set to logical H. The state of the busy flag is output in response to the STRD command. While the busy flag is H, no instruction can be accepted (except the STRD command). The busy state period (T) is as follows.

  $2/fosc \leqq T \leqq 4/fosc$ [seconds]   fosc: Frequency of OSC1

- Oscillation frequency

    The frequency select pins (FS1 and FS2), are used to set the relation between the oscillation frequency (f_{OSC}) and frame frequency (f_M), as shown in the table below.

R_f (kΩ)	f_{OSC} (kHz)	f/φ (kHz)	f_{FRM} (Hz)	f_M (Hz)	FS1	FS2
1000	26.88	13.44	70	35	0	0
480	53.76	26.88	70	35	1	0
105	215.00	107.50	70	35	0	1
50	430.10	215.00	70	35	1	1

Note 9: The resistance values are typical values.
The oscillation frequency depends on how the device is mounted. It is necessary to adjust the oscillation frequency to a target value.

- Expansion function

    The T6A04A's expansion function, allows two, T6A04As to drive an LCD panel of up to 240 by 64 dots.
    The table below shows the functions which can be selected with the M/S and EXP pins.

		M/S	
		H	L
EXP	H	• Two-chip mode (enable expansion mode) • Master chip COM1 to COM32 are available.	• Two-chip mode (enable expansion mode) • Slave chip • COM33 to COM64 are available. • Timing signals and power voltage are supplied from master chip.
	L	• Single-chip mode (disable expansion mode) • COM1 to COM32 are available.	• Do not select.

    Figures 13-1 and -2 illustrate application examples of disable expansion mode and enable expansion mode.
    Enable Expansion Mode (two-chip mode)
    As shown in Figure 13-2, and Figure 14 the master chip supplies the LCD drive signals and power voltage to the slave chip (the oscillator, the timing circuits, op-amp and contrast control circuit are disabled).
    COM1 to COM32 of the master chip and COM33 to COM64 of the slave chip are available (COM33 to COM64 of the master chip and COM1 to COM32 of the slave chip are disabled).
    The T9841B is available as an expansion driver for the T6A04A (a T6A04A and T9841B can drive a 200 × 64-dot LCD panel).
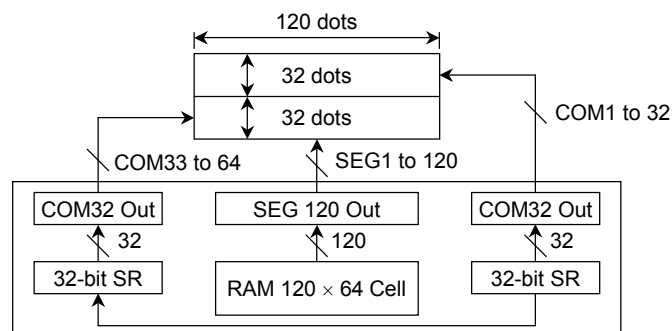
    (1)   Disable expansion mode

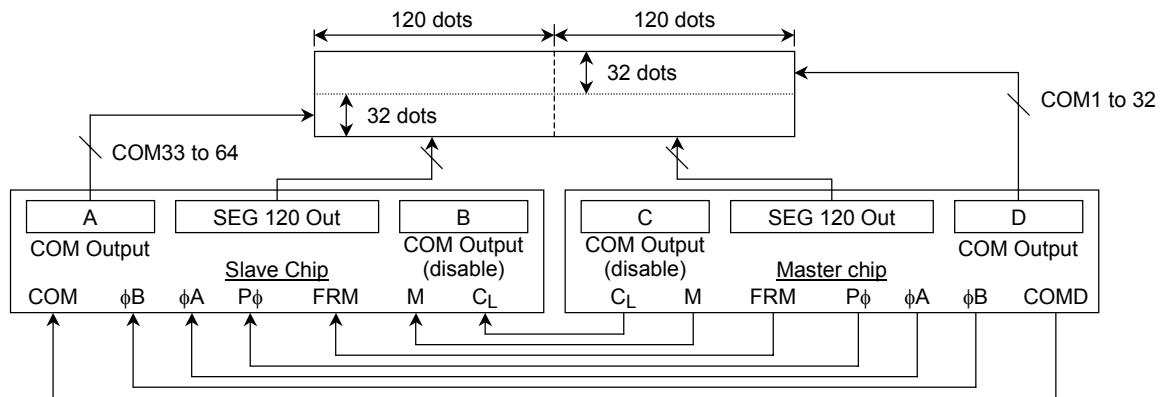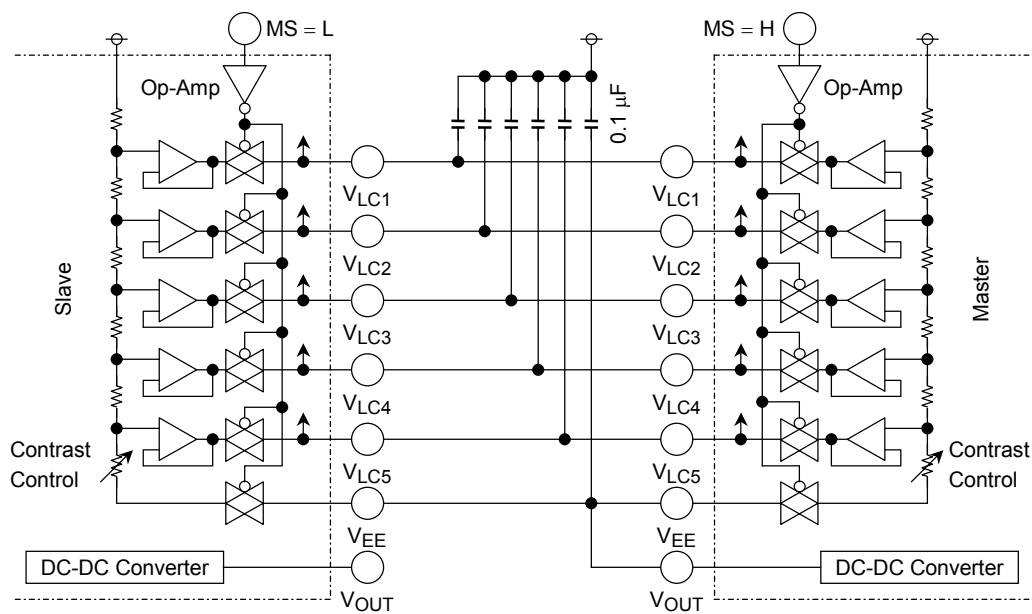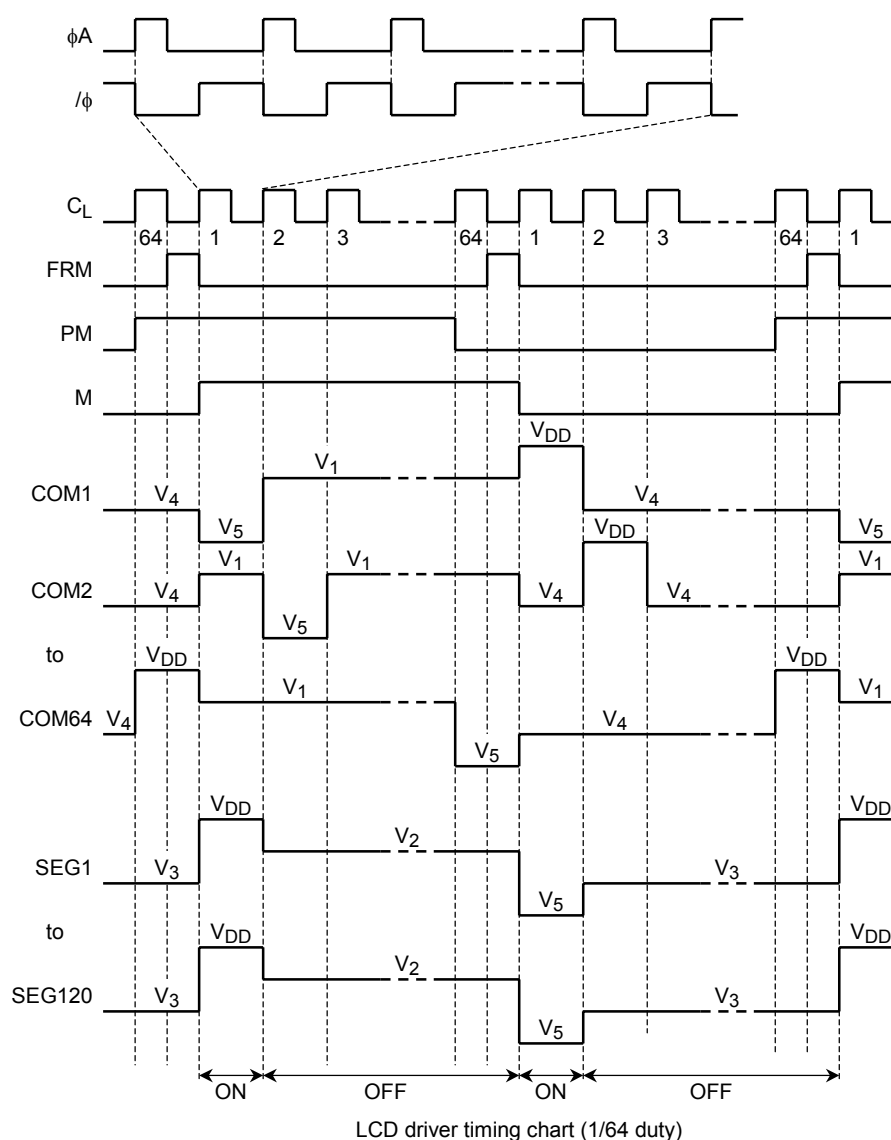**Figure 13-1**

(2) Expansion mode

Figure 13-2

Figure 14

LCD Driver Waveform

LCD driver timing chart (1/64 duty)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage (1)	V_{DD} (Note 10)	−0.3 to 7.0	V
Supply voltage (2)	$V_{LC1, 2, 3, 4, 5}$ V_{EE} (Note 12)	V_{DD} − 18.0 to V_{DD} + 0.3	V
Input voltage	V_{IN} (Note 10, 11)	−0.3 to V_{DD} + 0.3	V
Operating temperature	T_{opr}	−20 to 75	°C
Storage temperature	T_{stg}	−55 to 25	°C

Note 10: Referenced to V_{SS} = 0 V

Note 11: Applies to all data bus pins and input pins except V_{EE}, V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4} and V_{LC5}.

Note 12: Ensure that the following condition is always maintained.

$V_{DD} \geqq V_{LC1} \geqq V_{LC2} \geqq V_{LC3} \geqq V_{LC4} \geqq V_{LC5} \geqq V_{EE}$

Electrical Characteristics

DC Characteristics

Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, V_{LC5} = 0 V, Ta = –20 to 75°C)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	PIN Name
Operating supply (1)		V_{DD}	—	—	4.5	—	5.5	V	V_{DD}, V_{IN}
Operating supply (2)		V_{LC5} V_{EE}	—	—	V_{DD} – 16.0	—	V_{DD} – 4.0	V	V_{EE}, V_{LC5}
Input voltage (1)	H level	V_{IH1}	—	—	0.7 V_{DD}	—	V_{DD}	V	M/S, EXP, R_1, R_2, C_L, M, FRM, ϕA, ϕB, COMD, FS1, FS2, Pϕ
	L level	V_{IL1}	—	—	0	—	0.3 V_{DD}		
Input voltage (2)	H level	V_{IH2}	—	—	2.2	—	V_{DD}	V	DB0 to DB7, D/I, /WR, /CE, /RST, /STB
	L level	V_{IL2}	—	—	0	—	0.8		
Output voltage (1)	H level	V_{OH1}	—	I_{OH} = –400 μA	V_{DD} – 0.4	—	V_{DD}	V	C_L, M, FRM, Pϕ, COMD, ϕA, ϕB
	L level	V_{OL1}	—	I_{OL} = 400 μA	0	—	0.4		
Output voltage (2)	H level	V_{OH2}	—	I_{OH} = –205 μA	2.4	—	V_{DD}	V	D/I, /WR, /CE, DB0 to DB7, /RST, /STB
	L level	V_{OL2}	—	I_{OL} = 1.6 mA	0	—	0.4		
Column output resistance		Rcol	—	V_{DD} – V_{LC5} = 11.0 V Load current = ±100 μA	—	—	7.5	kΩ	SEG1 to SEG120
Row output resistance		Rrow	—	V_{DD} – V_{LC5} = 11.0 V Load current = ±100 μA	—	—	1.5	kΩ	COM1 to COM64
Input leakage		I_{IL}	—	V_{IN} = V_{DD} to GND	–1	—	1	μA	M/S, EXP, R_1, R_2, C_L, M, FRM, D/I, /WR, COMD, /CE, DB0 to DB7, /STB, /RST, FS1, FS2, Pϕ, ϕA, ϕB
Operating freq.		fϕ	—	—	10	—	250	kHz	/ϕ
External clock freq.		f_{ex}	—	—	20	—	500	kHz	OSC1
External clock duty		f_{duty}	—	—	45	50	55	%	OSC1
External clock rise/fall time		t_r/t_f	—	—	—	—	50	ns	V_{DD}
Current consumption (1)		I_{DD1}	—	(Note 13)	—	850	1400	μA	V_{DD}
Current consumption (2)		I_{DD2}	—	(Note 14)	—	950	1600	μA	V_{DD}
Current consumption (3)		I_{DDSTB}	—	(Note 15)	–1	—	1	μA	V_{DD}
Output voltage		Vo	1	(Note 16)	–4.0	–4.2	—	V	V_{OUT}

Note 13: V_{DD} = 5.0 V ± 10%, V_{EE} = V_{OUT} (from DC-DC converter)
Master mode, no data access
R_f = 47 kΩ, no load
1/9 bias, FS1, 2 = H, op-amp strength at minimum level

Note 14: V_{DD} = 5.0 V ± 10%, V_{EE} = V_{OUT} (from DC-DC Converter)
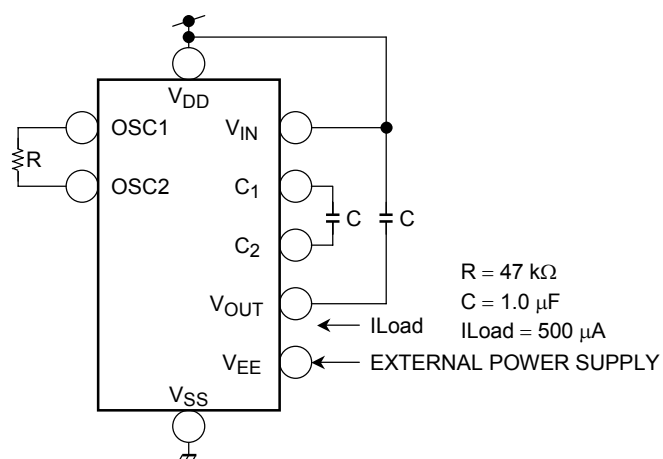Master mode, data access cycle $f_{/CE}$ = 1 MHz
R_f = 47 kΩ, No load
1/9 bias, FS1, 2 = H, op-amp strength at minimum level

Note 15: V_{DD} = 5.0 V ± 10%, V_{DD} – V_{EE} = 16 V
Master mode, /STB = L

Note 16: V_{IN} = 5.0 V, ILoad = 500 μA, V_{EE} = –5.0 V (external power supply)
C_1 – C_2 = 1.0 μF, V_{IN} – V_{OUT} = 1.0 μF, R = 47 kΩ, Ta = 25°C

Test Circuit

1.

$R = 47\ k\Omega$
$C = 1.0\ \mu F$
$ILoad = 500\ \mu A$

AC Characteristics

Test Conditions (Unless Otherwise Noted, $V_{SS} = 0$ V, $V_{DD} = 5.0$ V ± 10%, Ta = −20 to 75°C)

Characteristics	Symbol	Min	Max	Unit
Enable cycle time	t_{cycE}	500	—	ns
Enable pulse width	PWEL	220	—	ns
Enable rise/fall time	t_{Er}, t_{Ef}	—	20	ns
Address set-up time	t_{AS}	40	—	ns
Address hold time	t_{AH}	0	—	ns
Data set-up time	t_{DS}	60	—	ns
Data hold time	t_{DHW}	10	—	ns
Data delay time	t_{DD} (Note 17)	—	200	ns
Data hold time	t_{DHR} (Note 17)	10	—	ns

Load Circuit

$R_L = 2.4\ k\Omega$
$R = 11\ k\Omega$
$C = 130$ pF (including wiring capacitance)
$D = 1S1588$

Note 17: With load circuit connected

Application Circuit

(1) T6A04A single-chip mode

- Oscillation frequency is at a minimum.
- LCD drive bias is 1/9.
- DC-DC converter is used.

Application Circuit

(2) T6A04A two-chip mode

- Oscillation frequency is at a minimum.
- LCD drive bias is 1/9.
- DC-DC converter is used.
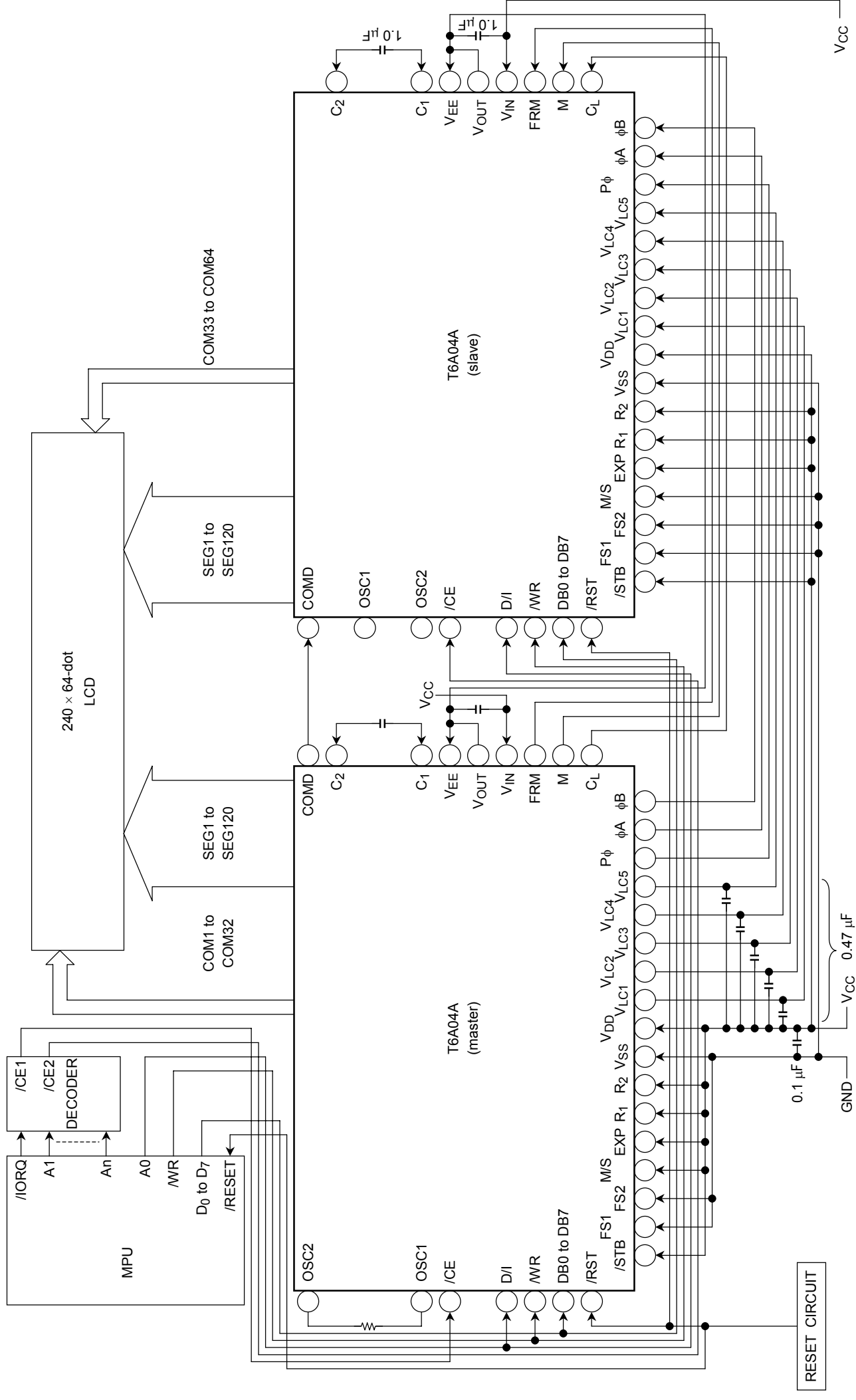
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