1 Tentative 128-bit address translation specification

1.1 Overview of the translation schemes

We propose two new translation schemes for 128-bit addresses, Sv44 and Sv54, which differ in the amount of virtual memory a process sees. We artificially limit physical address size to 2^{64}, by arbitrarily limiting the size of the PPN to 50.

Minimal Page Size Page size is increased to 16 KiB from the 4 KiB of RV32 and RV64. This is because for current workloads, and especially those requiring a large address space, we expect 4 KiB pages to cause a lot more TLB misses, and 16 KiB strikes a better balance between memory usage and TLB misses.

Page Table Entry Size The page table entries (PTEs) are widened to 128-bit, thus following `MXLEN`, even though the upper double-word isn't used as of now. This allows for further flexibility to define future schemes, and eases development, since it follows the natural integer size of RV128. This leads to a 1K entries per page.

1.2 Sv44

1.2.1 Additional Properties

Page Table Depth The page table's depth is kept at 3 (analogous to Sv39 in RV64), to limit latency in cases of TLB misses.

1.2.2 Implementation

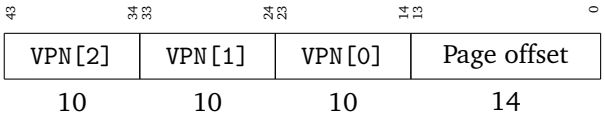

FIGURE 1 – Sv44 Virtual Address

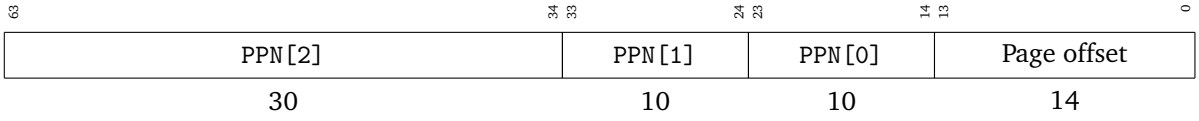

FIGURE 2 – Sv44 Physical Address

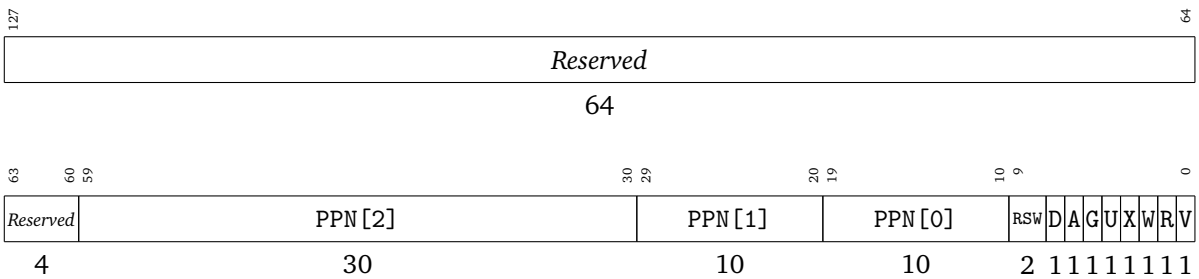

FIGURE 3 – Sv44 Page Table Entry

1.2.3 Larger Page Size

Using the approach used for RV32 and RV64, we can define pages of 16 MiB and 16 GiB.

1.2.4 Limitations

Maximum size of a virtual address space : 44 bits $\implies 2^{44} = 16$ TiB.
Maximal addressable physical memory : 64 bits $\implies 2^{64} = 16$ EiB.

1.3 Sv54

1.3.1 Additional Properties

Page Table Depth The page table's depth is now 4.

1.3.2 Implementation

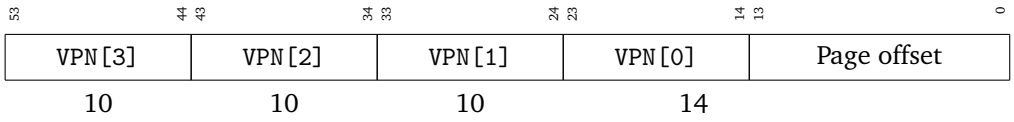

FIGURE 4 – Sv54 Virtual Address

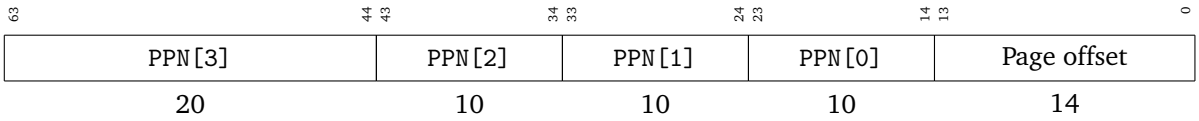

FIGURE 5 – Sv54 Physical Address

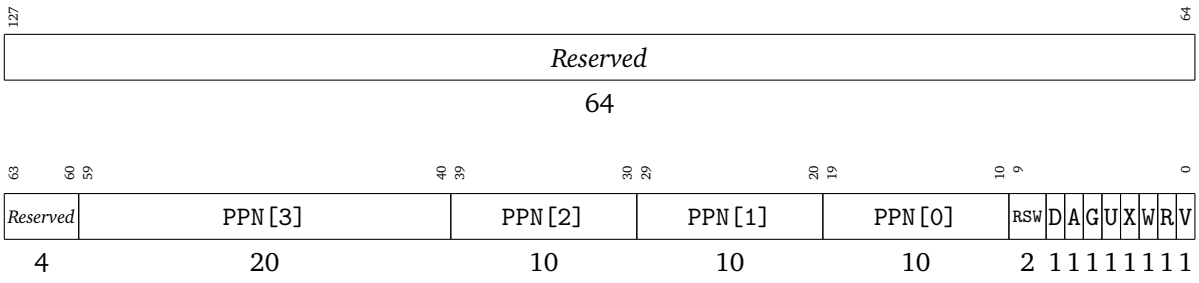

FIGURE 6 – Sv44 Page Table Entry

1.3.3 Limitations

Maximum size of a virtual address space : 54 bits $\implies 2^{54} = 16$ PiB.
Maximal addressable physical memory : 64 bits $\implies 2^{64} = 16$ EiB.

1.3.4 Larger Page Size

Using the approach used for RV32 and RV64, we can define pages of 16 MiB, 16 GiB and 16 TiB.

1.4 `satp` Register

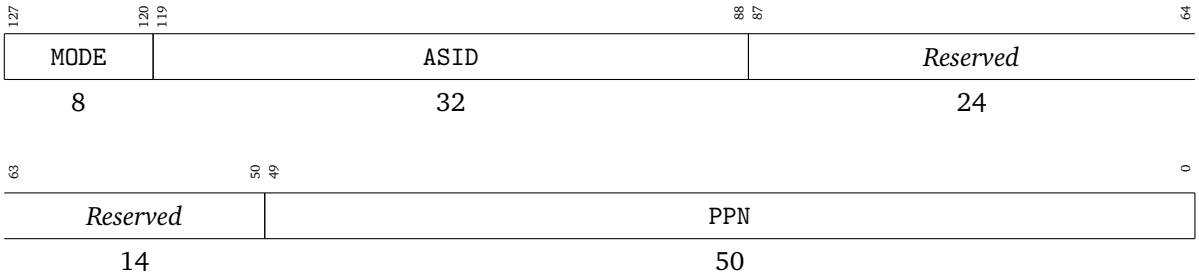

FIGURE 7 – Structure of the `satp` register

1.4.1 `MODE` values

`MODE` field value	Adressing mode
0	Bare
1-11	*Reserved*
12	Sv44
13	Sv54
$14 \rightarrow 255$	*Reserved*

Additional values can be used for new addressing schemes, and some bits could be used as flags for address translation features, too.

18 bits are left reserved for now above the `PPN` field, to facilitate possible future physical memory range extensions, or to be used to denote virtual memory capabilities (in the sense of Cambridge' CHERI for instance).

1.5 Translation process

The translation process remains unchanged from the one described in the base specification (as of writing, it is located in section 4.3.2 of the privileged spec), with the following constants :

— `PAGESIZE` = 2^{14}
— `LEVELS` = 3 for Sv44, or 4 for Sv54
— `PTESIZE` = 16