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PAPER

# Wafer-scale uniformity of Dolan-bridge and bridgeless Manhattan-style Josephson junctions for superconducting quantum processors

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Supplementary material for this article is available online

## Abstract

We investigate die-level and wafer-scale uniformity of Dolan-bridge and bridgeless Manhattan-style Josephson junctions, using multiple substrates with and without through-silicon vias (TSVs). Dolan junctions fabricated on planar substrates have the highest yield and lowest room-temperature conductance spread, equivalent to ∼100 MHz in transmon frequency. In TSV-integrated substrates, Dolan junctions suffer most in both yield and disorder, making Manhattan junctions preferable. Manhattan junctions show pronounced conductance decrease from wafer center to edge, which we qualitatively capture using a geometric model of spatially-dependent resist shadowing during junction electrode evaporation. Analysis of actual junction overlap areas using scanning electron micrographs supports the model, and further points to a remnant spatial dependence possibly due to contact resistance.

## 1. Introduction

Monolithic superconducting quantum processors (SQPs) have scaled to enable key demonstrations of quantum-computational advantage [1] and milestone demonstrations of quantum error correction [2–4] on the road to fault-tolerant quantum computing. Sustaining this scaling requires a multi-faceted fabrication approach simultaneously meeting yield, frequency, coherence, and coupling requirements of circuit elements, as well as the routing of control lines needed for gate and measurement operations. The latter motivates the active development of 3D integration strategies such as flip-chip [5–7] to avoid overcrowding of circuit elements and vertical routing [8–10] of input and output lines to circumvent the scaling limitations associated with lateral wirebonding. Through-silicon visas (TSVs) are needed in some vertical routing approaches [11–14], and especially for suppression of resonance modes arising from the increased size of SQPs and their packaging.

TSVs further aggravate the targeting of superconducting qubit frequencies, which already bottlenecks the yield of operable devices even on planar substrates [15]. Poor qubit frequency targeting is a primary cause of crosstalk induced by microwave drives [2] and can limit gate speeds. It also increases residual *ZZ* coupling in processors with always-on qubit-qubit coupling [2, 3, 16], making gate fidelity and leakage dependent on the state of spectator qubits [17]. Laser annealing of qubit Josephson junctions (JJs) [15, 18–21] is an established method for selective qubit frequency trimming without intrinsic effect on qubit coherence. Currently, laser annealing allows a monotonic decrease with ∼300 MHz range and ∼15 MHz imprecision (defined as the

standard deviation of frequency targeting error post-annealing) [21]. To safely rely on laser annealing for post-fabrication trimming, fabrication itself must achieve an imprecision several times lower than the tuning range, e.g. ∼50 MHz.

The main limit to qubit frequency targeting is variability in the fabrication of Al-$AlO_x$-Al JJs, which most commonly relies on double-angle shadow evaporation with intermediate *in-situ* oxidation. Two main variables affecting the Josephson coupling energy ($E_J$) are the overlap area between the two Al electrodes and the tunnel barrier thickness. The two most popular JJ fabrication variants differ only in the shadowing mechanism: Dolan-bridge [22] junctions use a suspended resist bridge whereas Manhattan-style [23] junctions do not. Since Dolan JJs are more sensitive to resist-height variation by design, Manhattan JJs may be preferable particularly on substrates with TSVs that compromise the uniformity of spin-coated resist. Previous works have shown a reduction in wafer-scale variation of Manhattan JJs [24, 25]. On the other hand, recent reports [26–28] indicate that geometric effects cause pronounced center-to-edge variation in Manhattan JJs, affecting their uniformity at wafer scale.

In this work, we present an experimental investigation comparing the uniformity of Dolan versus Manhattan JJs at both die- and wafer-scale on planar substrates with and without TSVs. We benchmark uniformity using room-temperature (RT) conductance ($G$) measurements, extracting the conductance coefficient of variation (CV) and residual standard deviation (RSD) of predicted transmon frequency. A wafer-center-to-edge variation is again observed particularly in Manhattan junctions, which we attribute to a geometric shadowing effect during electrode evaporation. Scanning electron microscopy (SEM) of many junctions supports the model, and further points to remnant spatial dependence possibly due to contact resistance. Our findings indicate that for our current fabrication processes, Dolan JJs perform best for planar substrates, while the opposite holds for TSV-integrated substrates. We identify several paths for further required improvement.

## 2. Design of experiments

We investigate uniformity of Dolan and Manhattan JJs using six 100 mm diameter Si wafers. (Sections S1 and S2 of the Supplementary Information provide detailed descriptions of the fabrication processes used.) Three of these wafers, labeled Planar 17Q (quantity one) and TSV 17Q (quantity two), are used to obtain and compare metrics for both junction variants in fully planar substrates and TSV-integrated ones. Each wafer contains thousands of test structures, each consisting of two nominally identical JJs connecting in parallel to pre-fabricated NbTiN probing pads (200 nm thick, defined by sputtering and etching). These test structures mimic the two-junction transmon with NbTiN capacitor plates used in our standard SQPs (figure 1(a)).

In the Planar 17Q wafer, a 13 × 13 mm die-level layout mimicking our planar 17-qubit SQP (Surface-17 [11, 21, 29]) is copy-pasted into two 2 × 4 arrays. The top half of the wafer has test-structure arrays for Dolan-bridge JJs, while the bottom half has test-structure arrays for Manhattan-style JJs. At the location of each transmon of the SQP, we place a sub-array of 4 × 4 test structures. Within each sub-array (figure 1(b)), the designed single-junction overlap area ($A_{\text{overlap}}$) is finely stepped within one of three ranges, labeled low (l), mid (m) and high (h), mimicking the choice of three qubit-frequency groups in our SQPs [11, 16, 21, 29]. For Dolan-bridge JJs, we change $A_{\text{overlap}}$ by varying the width $W_t$ of the top electrode and keeping the width of the bottom electrode $W_b = 3W_t$. For Manhattan-style JJs, we instead vary $W_b$ and fix $W_t = 160$ nm. In total, the wafer contains 2176 test structures of each JJ variant. We first fabricate only the Manhattan JJs on the bottom half of the wafer and perform all conductance measurements on them. We subsequently fabricate and measure all Dolan JJs on the top half of the wafer. Each TSV 17Q wafer contains test structures of only one JJ variant. In each wafer, the die-level layout (copy-pasted into one 2 × 4 array) has TSVs placed at the same locations as a variant of Surface-17 with TSVs (figure 1(b)). The density (∼1.7% area coverage) and position of TSVs is chosen to push the lowest-frequency spurious modes of the SQP in its sample holder to $\gtrsim 15$ GHz (as per finite-element simulation). At the location of each transmon in the SQP, we place a 5 × 5 sub-array of test structures. In this case, all sub-arrays are identical. Importantly, test structures overlapping with TSVs, although fabricated, are ignored and not included in conductance measurements. This yields at most 378 viable test structures per die and thus 3024 per wafer.

Three additional wafers, labeled Planar 35 × 35, are used to test the geometric resist-shadowing model and to investigate further sources of spatial non-uniformity in Manhattan JJs. Each wafer (figure 5) has a 35 × 35 array of nominally identical test structures ($W_b = W_t = 200$ nm). In the first wafer, like in the 17Q wafers, the test structures have symmetric JJ pairs with NbTiN probing pads. In the second, they have symmetric JJ pairs with TiN probing pads (160 nm thick, pre-defined by atomic layer deposition (ALD) and etching). In the third, they have single JJs with Al probing pads evaporated simultaneously with the JJ electrodes.

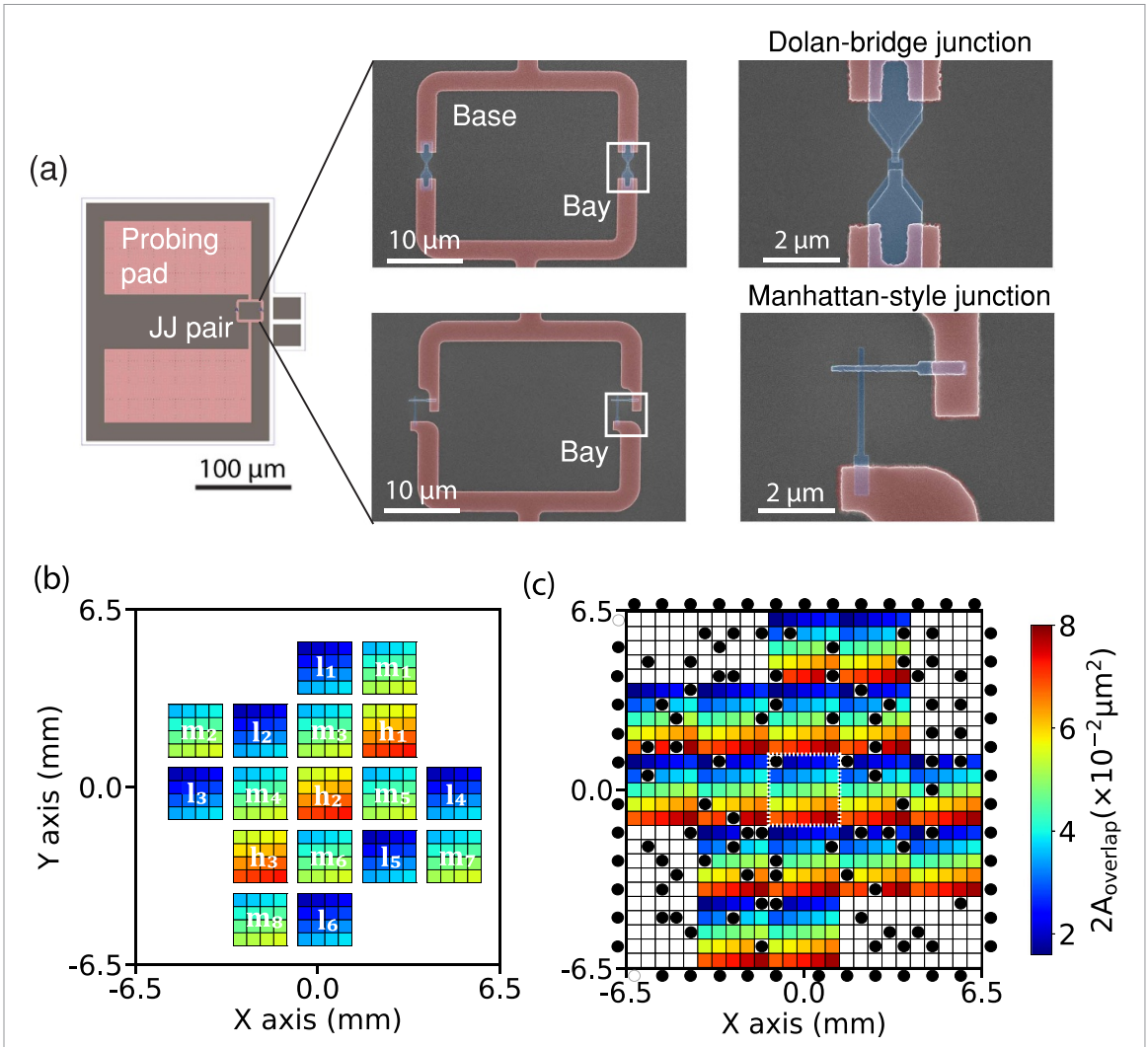


**Figure 1.** (a) Schematic and SEM images at two length scales of the test structures used to investigate uniformity of Dolan versus Manhattan JJ pairs on planar and TSV-integrated wafers. Two junctions in each structure complete a loop with a pre-fabricated NbTiN base. Probing pads in the base allow measuring the parallel conductance of the junction pair. (b) Die-level planar layout with 17, $4 \times 4$ sub-arrays of junction test structures. Each array is centered at the location of one transmon in our planar Surface-17 SQP. Each array has a sweep of junction overlap area $A_{overlap}$ in one of three ranges (labeled l, m and h). (c) Die-level TSV layout arranged as 17, $5 \times 5$ sub-arrays of junction test structures. Each array is centered at the location of one transmon in our TSV-integrated Surface-17. One such array is highlighted by the white dotted line. Each array has an identical sweep of $A_{overlap}$. Test structures that overlap with vias (black circles) are ignored and not included in measurements, yielding at most 378 test structures per die. Heatmaps in (b) and (c) indicate the chosen $A_{overlap}$ for each test structure.

## 3. Measurements and analysis

All $G$ measurements are acquired by the 2-point method using a home-built transimpedance amplifier with gain $10^5\,\Omega$. A low input voltage (10 mV) is applied across the junctions to minimize the possibility of causing failure to open or short circuit. With one exception noted below, measurements on all planar wafers are performed using a manual probe station located inside our cleanroom, which is temperature controlled to $20 \pm 1\,^{\circ}$C. During manual measurements, the intensity from a light-emitting diode source is set to the lowest possible visibility (<500 lx), limiting the contribution from substrate conductance to $<1\,\mu$S, as determined from $G$ measurements on test structures both without JJs and with JJs known to have failed to open circuit. Measurements on the TSV 17Q wafers as well as on the Planar $35 \times 35$ TiN wafer are performed using a home-built automated probe station, also located inside the cleanroom, whose measurements are performed fully in the dark. To quantify series resistance from the probe contact and external cabling, we compared 2- and 4-point $G$ measurements taken with the automated probe station, finding a best-fit value of $\sim 18\,\Omega$. The series resistance of NbTiN probing pads is found to vary from $200\,\Omega$ at wafer center to $330\,\Omega$ at wafer edge by fabricating test structures with bays short-circuited directly in the base layer. This variation is attributed to the radial dependence of the thickness of the sputtered NbTiN films (resistivity

$\rho = 100\,\mu\Omega$-cm). Reported $G$ values are raw, i.e. as obtained from 2-point measurement without correction for series resistance, substrate conductance, nor a $4\,\mu$S offset from the transimpedance amplifier.

The range of $G$ is $40 - 350\,\mu$S. Values $< 20\,\mu$S and $>500\,\mu$S are filtered out as they mostly correspond to open and shorted junctions, respectively. To systematically detect and filter out data containing an open junction in a pair, a two-part linear regression analysis of conductance versus $A_{\text{overlap}}$ is implemented within each die in the Planar and TSV 17Q wafers. Values below 70% of the initial best fit are filtered out (figures S3 and S4). For the Planar $35 \times 35$ wafers containing nominally identical test structures throughout, conductance values below 70% of the mean are filtered out.

To quantify non-uniformity at both die and wafer scale, we use the conductance CV as a function of $A_{\text{overlap}}$ and the RSD of predicted qubit frequency. Die-(wafer-) level conductance CV is calculated using all the test structures with identical $A_{\text{overlap}}$ across the die (wafer) when calculating the mean $\mu_G$ and standard deviation $\sigma_G$. The spatial variation of junction conductance is visualized using heatmaps of conductance normalized by $\mu_G$ of all test structures with identical $A_{\text{overlap}}$. The predicted transmon qubit transition frequency ($f_{01}$) is calculated from $G$ using

$$f_{01} = \sqrt{8 f_c f_J} - f_c,$$

where $f_c = E_c/h = 270\,$MHz with $E_c$ the designed transmon charging energy, $f_J = E_J/h$, and $f_J = MG$ [30–32]. Here, $M = 134\,$GHz/mS is an experimentally determined constant obtained by comparing $G$ measured immediately prior to cooldown to the $E_J$ extracted for transmons across many of our SQPs. ($E_J$ is extracted from spectroscopy data obtained during cryogenic characterization.) Die-level frequency RSD is calculated from the residuals of the second fit. Wafer-level RSD is calculated similarly, but the residuals are obtained by performing a single fit on the combined filtered $G$ data from all dies.

To test the geometric resist-shadowing model, SEM images of JJs from different coordinates on all Planar $35 \times 35$ wafers are acquired at $10^5\times$ magnification. A total of 34 (35) JJ pairs are imaged for the NbTiN (TiN) wafer, and 36 single JJs for the Al wafer. Imaging is performed only after conductance measurements are completed. The actual deposited junction widths ($W'_b$, $W'_t$) and overlap area ($A'_{\text{overlap}}$) are extracted using home-made image analysis software (based on the OpenCV package) with the work flow presented in figure S8. The presence of other sources of spatial non-uniformity is evidenced from the spatial dependence of effective JJ conductivity calculated as $G/\Sigma A'_{\text{overlap}}$.

## 4. Results

A total of 2176 (3024) test structures are fabricated per JJ variant for the Planar and TSV 17Q datasets. A zoomed-out view (figure 2) of the planar dataset shows that the spatial variation of normalized conductance for Dolan JJs is significantly lower than for Manhattan JJs. For the latter, there is a clear systematic decrease from center to edge, making it unsurprising that the wafer-scale conductance CV is higher for Manhattan over all $A_{\text{overlap}}$. The general decrease observed in the conductance CV with increasing $A_{\text{overlap}}$ is in line with previous works [33, 34]. At die level, the spread of Dolan JJs is also lowest, with $\sim$100 MHz frequency RSD uniform across the wafer. For Manhattan JJs, the frequency RSD increases away from wafer center, indicating that the spatial variation is relevant even at die level.

Turning over to the TSV dataset (figure 3), we can again discern an underlying center-to-edge dependence for Manhattan JJs. However, this trend is masked by a significant increase in disorder. The disorder is much stronger for Dolan JJs, evident both at wafer scale and die level. Interestingly, the CV for Dolan does not display any clear dependence on $A_{\text{overlap}}$, suggesting that resist-height variations dominate the spread. Measurements of resist-height variations caused by TSVs and evidence of the impact of such variations on junction electrode and overlap geometries are shown in figure S2.

Note that the CV and RSD for Dolan are calculated both with and without applying regression filters. This is necessary because the high disorder makes the regression filter unable to reject only defective junctions. Even with the artificial improvement of Dolan CV and RSD that may arise from removing non-defective junctions, a strong conclusion holds: with TSVs, Manhattan JJs systematically outperform Dolan JJs. Nonetheless, with >300 MHz RSD at die level, even Manhattan JJs fall very short of frequency targeting objectives in the presence of TSVs. However, there is room for optimism as this investigation is best interpreted as a worst-case scenario for actual TSV-integrated SQPs. In our test, we place many junction pairs per transmon location of Surface-17. Therefore, in a real Surface-17, transmon JJ pairs would on average be $500\,\mu$m away from TSVs. Furthermore, the footprint of TSVs could be further optimized following [12].

### 4.1. Geometric resist-shadowing model

The essence of the geometric model is a spatial dependence of junction electrode widths arising from oblique incidence of the Al flux during evaporation. Specifically, the width of vertical electrodes (both electrodes for

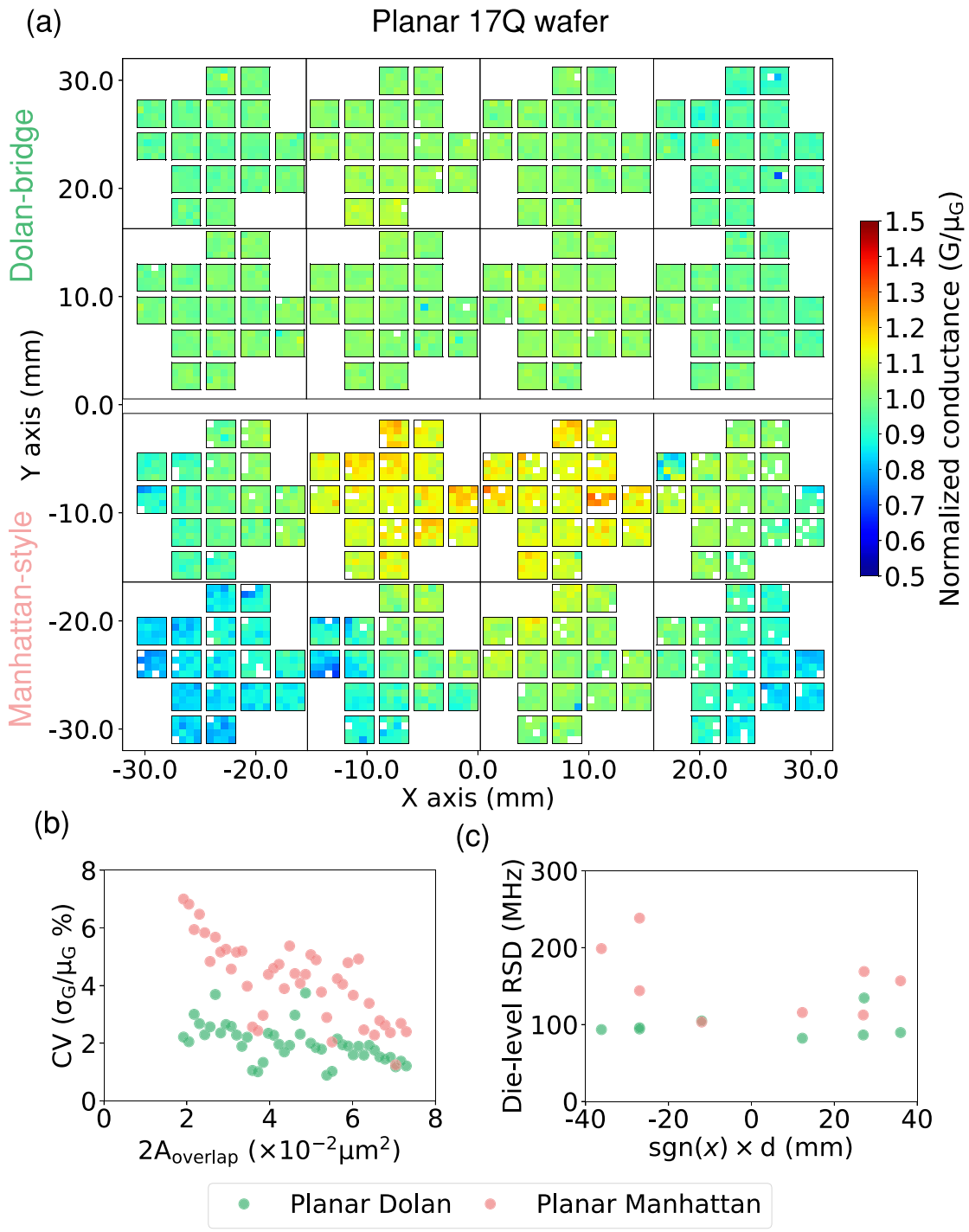


**Figure 2.** (a) Wafer-scale mean-normalized conductance heatmap of Dolan (top) and Manhattan (bottom) JJ test structures on the Planar 17Q wafer. The origin $(0, 0)$ indicates wafer center. Blank cells correspond to test structures identified as defective by the filtering. For this dataset, both JJ types are fabricated on a single wafer. (b) Wafer-scale conductance CV for both junction types as a function of $A_{\text{overlap}}$. (c) Die-level RSD of predicted qubit frequency as a function of distance (d) between die and wafer centers.

Dolan JJs, bottom electrode for Manhattan JJs) depends on the $x$ coordinate, while that of horizontal electrodes (top electrode for Manhattan) depends on the $y$ coordinate. Key parameters of the model are the thickness of the top resist $H = 600\,\text{nm}$ (which acts as the shadow mask), the wafer tilt $\alpha = 35°$ during Al evaporations, and the physical configuration of the electron-beam (e-beam) evaporator (Plassys MEB550S). These last parameters include the distance $D' = 650\,\text{mm}$ between the crucible at $\vec{C}$ and the pivot point $\vec{O}'$ of the sample holder, and the distance $R = 62.5\,\text{mm}$ between $\vec{O}'$ and center $\vec{O}$ of the exposed wafer surface (see schematic in figure 4(a)). This results in a distance $D = D'\cos(\alpha) - R$ between $\vec{C}$ and the plane defined by

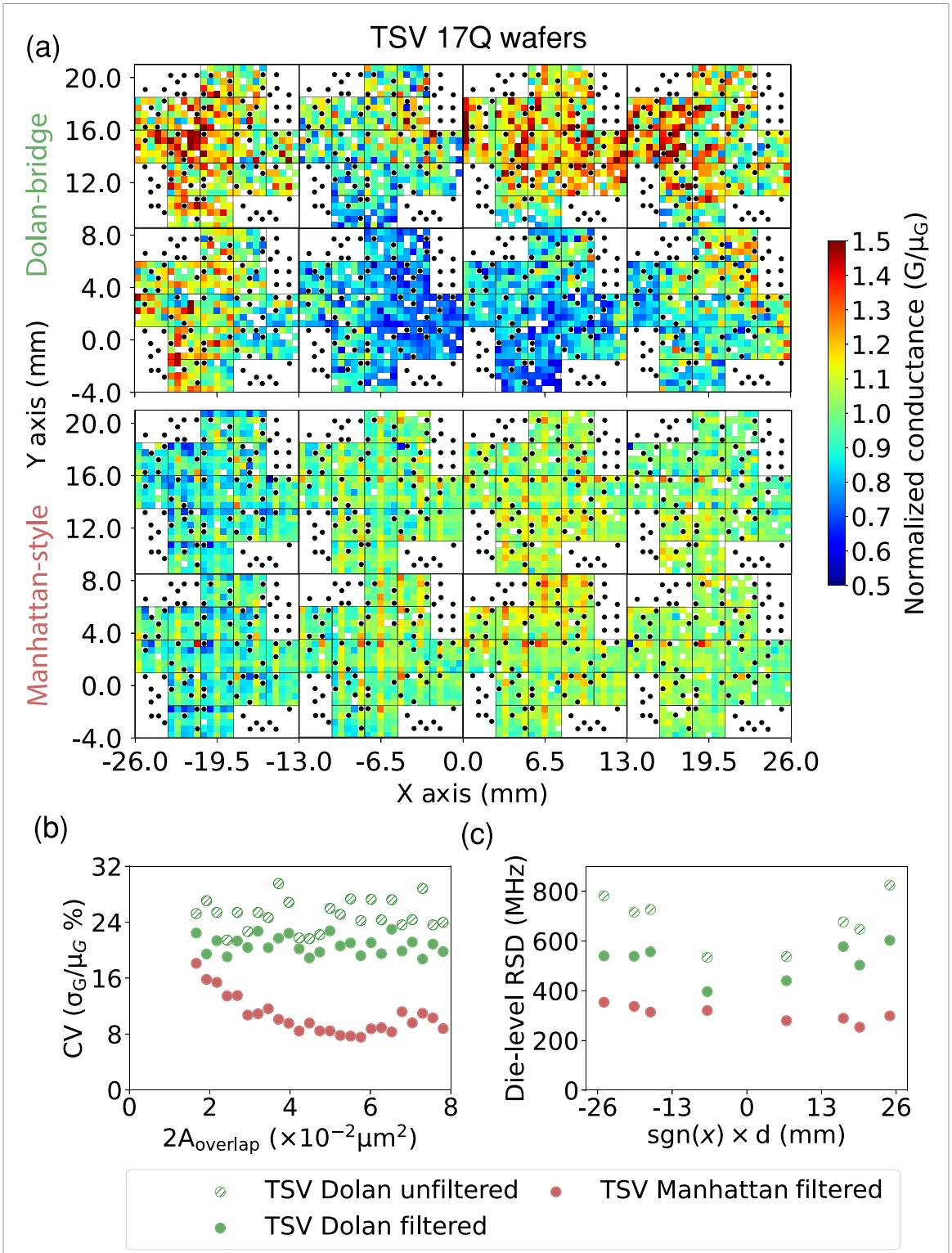


**Figure 3.** (a) Wafer-scale mean-normalized conductance heatmap of Dolan (top) and Manhattan (bottom) JJ test structures on TSV-integrated 17Q wafers. For this dataset, two separate wafers are fabricated, one for each JJ type. The origin $(0,0)$ indicates wafer center. Blank cells correspond to defective junctions removed by filtering outliers at die level. Cells marked with black circles indicate TSV locations. (b) Wafer-scale conductance CV for unfiltered (nf) and regression-filtered (f) Dolan JJ pairs and for filtered Manhattan JJ pairs as a function of $A_{\text{overlap}}$. (c) Die-level RSD of predicted qubit frequency as a function of distance (d) between die and wafer centers.

this surface [35]. In a cartesian coordinate system with origin at $\vec{O}$ and $\vec{r} = (x, y, 0)$ lying on this plane, $\vec{C} = (0, D' \sin(\alpha), D)$. Evaporation under these conditions deposits electrodes extending along the $y$ axis. An electrode of this orientation with $x$ coordinate has actual width

$$W'(x) \approx W + \delta W_{\text{offset}} - |x| \frac{H}{D}, \tag{1}$$

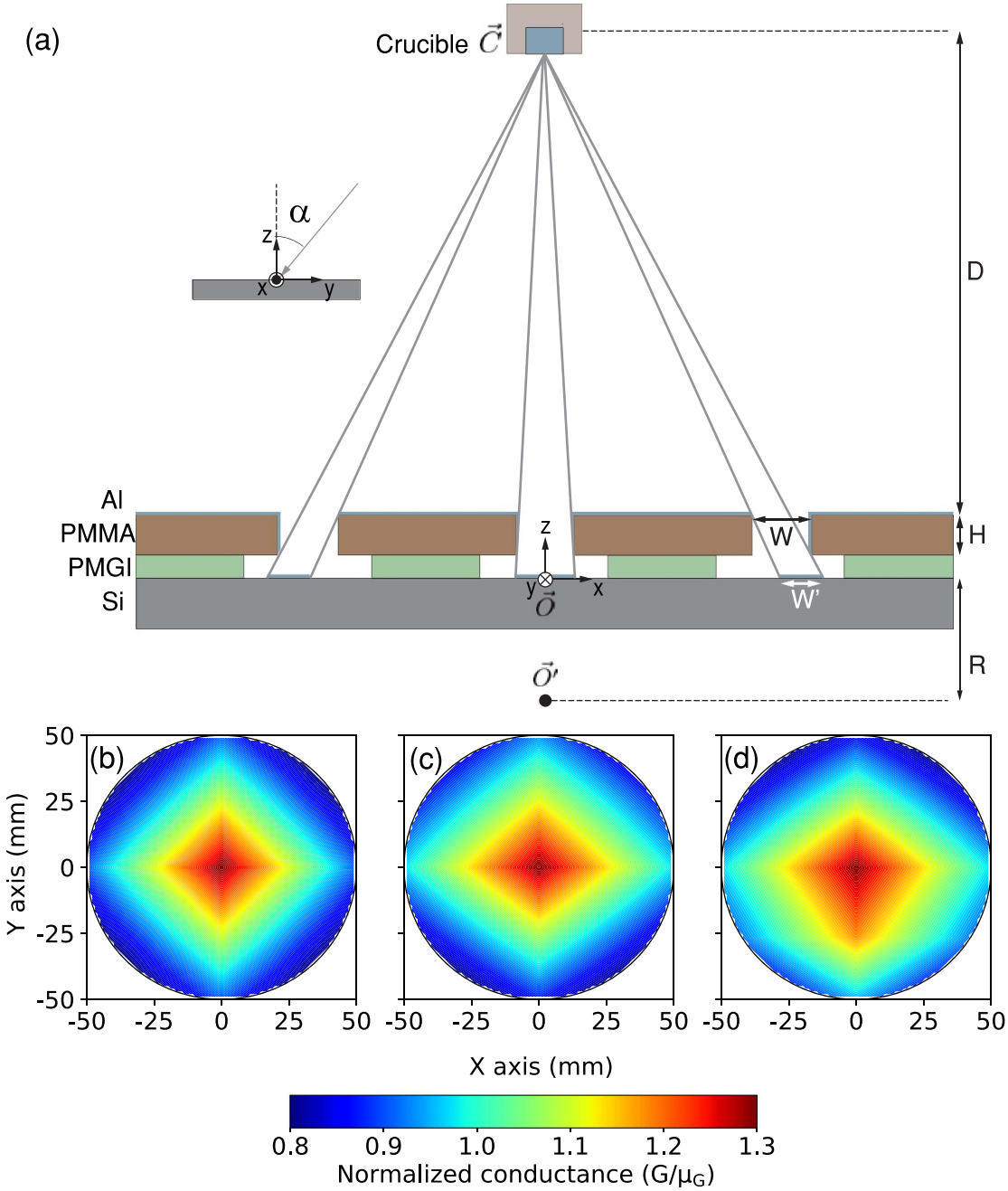


**Figure 4.** (a) Schematic of e-beam Al evaporation setup (not drawn to scale). Please see text for further details and parameter values. The illustration shows the decrease in junction electrode width from center to edge of wafer arising from the spatially-dependent shadowing effect. (b) Wafer-scale mean-normalized conductance computed from actual junction overlap area $A'_{\text{overlap}}$ as per equation (2), for Manhattan JJs with $W_{\text{t}} = W_{\text{b}} = 200\,\text{nm}$ and $\delta W_{\text{offset}} = 25\,\text{nm}$. (c) Same as (b) but adding the overlap contribution from sidewalls as per equation (4). (d) Same as (c) but adding effects of the first evaporation (of the bottom electrode) on the second evaporation (of the top electrode) (equations (5)–(7)).

where $\delta W_{\text{offset}}$ is a constant widening from over-exposure and development of the e-beam resist. Including these modifications to the width of both electrodes, the actual overlap area becomes

$$A'_{\text{overlap}}(\vec{r}) = W'_{\text{b}}(x)\, W'_{\text{t}}(y)\,. \tag{2}$$

Figure 4(b) shows the spatial dependence of $A'_{\text{overlap}}$ for Manhattan JJs with $W_{\text{b}} = W_{\text{t}} = 200\,\text{nm}$ and $\delta W_{\text{offset}} = 25\,\text{nm}$ on a 100-mm diameter wafer.

We can further expand the model by approximating the contribution of sidewalls to $A'_{\text{overlap}}$. The spatially-dependent actual bottom electrode thickness is

$$T'_{\text{b}}(\vec{r}) = T_{\text{b}} \frac{(D' - R)^2 D}{|\vec{r} - \vec{C}|^3}, \tag{3}$$

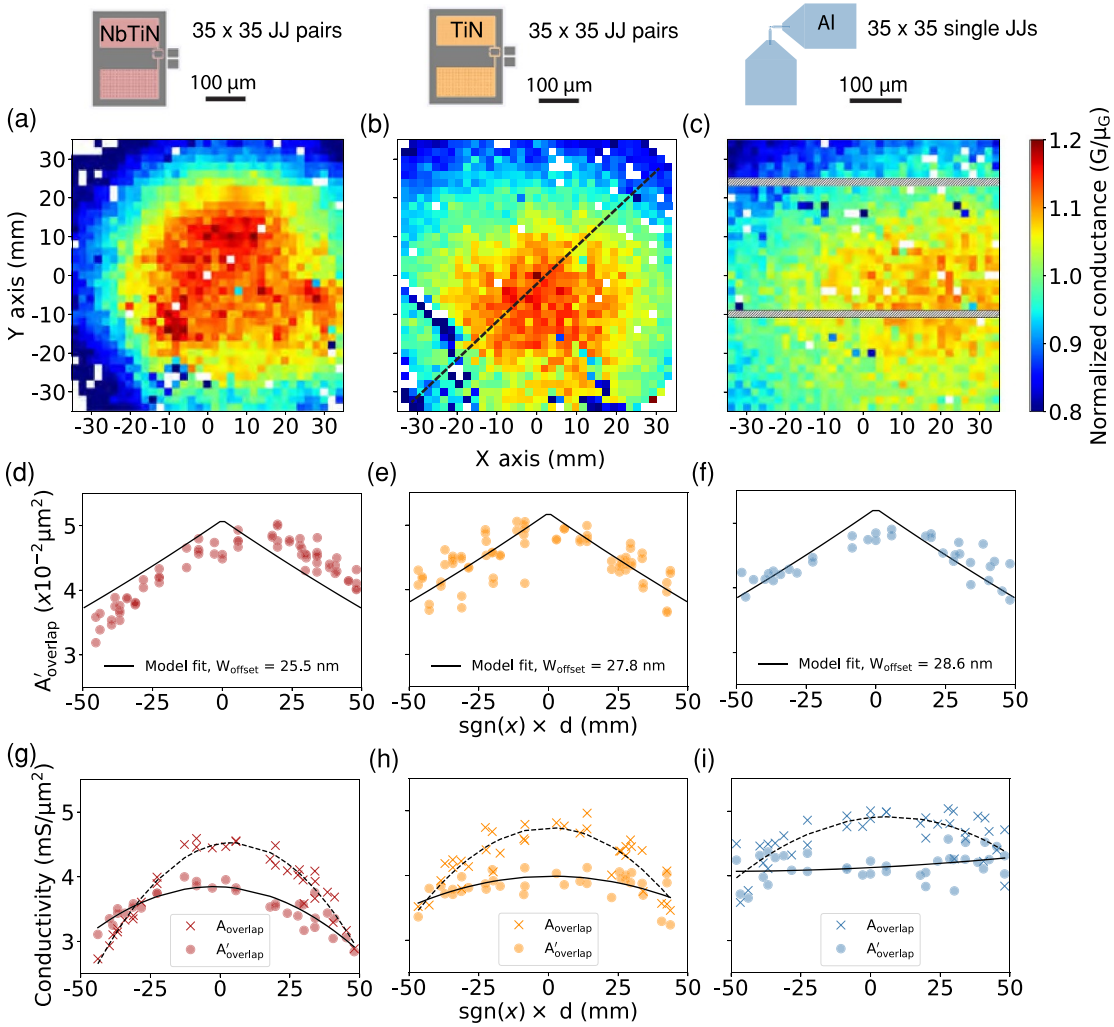


**Figure 5.** Wafer-scale mean-normalized conductance heatmap of 35 × 35 array of Manhattan JJ test structures fabricated on three planar wafers with the variants indicated by the top schematics. (a), (b) Symmetric junction pairs with (a) NbTiN probing pads deposited by sputtering and (b) TiN probing pads deposited by ALD. The black dotted line indicates the diagonal along which the JJ pairs are imaged for figure S9. (c) Single junctions with simultaneously fabricated Al probing pads. The hatched rows indicate accidentally omitted junctions during data acquisition. (d)–(f) Distribution of actual JJ overlap area $A'_{\mathrm{overlap}}$ as a function of junction radial position ($d$). Here, $A'_{\mathrm{overlap}}$ is extracted from top-view SEM images. Note that $A'_{\mathrm{overlap}}$ does not include the sidewall overlap as this contribution cannot be extracted from these images. The black curves are the best fits of the simplest geometric model (equation (2) with single free parameter $\delta W_{\mathrm{offset}}$). (g)–(i) Effective junction conductivity (computed from designed and actual overlap areas) as a function of $d$. The dashed (solid) curves are quadratic fits of $A_{\mathrm{overlap}}$ ($A'_{\mathrm{overlap}}$).

where $T_{\mathrm{b}} = 35\,\mathrm{nm}$ is the calibrated thickness at $\vec{O}$ under normal incidence ($\alpha = 0$). Approximating the sidewalls as vertical,

$$A'_{\mathrm{overlap}}(\vec{r}) = \left(W'_{\mathrm{b}}(x) + 2T'_{\mathrm{b}}(\vec{r})\right) W'_{\mathrm{t}}(y), \tag{4}$$

The modified spatial dependence is shown in figure 4(c). Note that we do not model the effect of shadowing by the bottom electrode during evaporation of the top electrode, which most likely reduces the overlap at the eastern sidewall (evident in figure S9).

Finally, we can model some predictable effects of the first evaporation (for the bottom electrode) on the top electrode. The first evaporation deposits an Al layer above the top resist, effectively increasing its height by $\delta H(\vec{r})$ (also given by the right-hand side of equation (3)). More importantly, it also deposits a lip on the southern resist edge for the top electrode (see figure S1), with width $W_{\mathrm{lip}}$ and height $H_{\mathrm{lip}}$:

$$W_{\mathrm{lip}}(\vec{r}) = -T_{\mathrm{b}} \frac{(D' - R)^2 (D' \sin(\alpha) - y)}{|\vec{r} - \vec{C}|^3}, \tag{5}$$

$$H_{\mathrm{lip}}(\vec{r}) = \frac{DW_{\mathrm{t}}}{D' \sin(\alpha) - y}. \tag{6}$$

**Table 1.** Summary of metrics obtained for Dolan and Manhattan JJ test structures on all wafers used throughout this study. The 17Q yield reported is that calculated for a Surface-17 SQP using the per-junction-pair yield of the Planar and TSV 17Q wafers. We note that the yield of actual planar Surface-17 SQPs with Manhattan-style JJs is roughly 50%, higher than that calculated from the Planar 17Q wafer. The die-level frequency RSD is the average across the eight dies in the 17Q wafers. For the 35 × 35 Planar wafers, the die-level frequency RSD is calculated from the average of sixteen 6 × 6 arrays of test structures within the inner 50 × 50 mm$^2$ area of the wafers.

| Summary of results | | | | | |
|---|---|---|---|---|---|
| Junction type | Substrate | Yield (%) | Conductance CV wafer scale (%) | Frequency RSD wafer scale (MHz) | Frequency RSD die level (MHz) |
| Dolan-bridge | Planar 17Q NbTiN | 2160/2176 = 99.2<br>17Q yield = 87.2 | 0.8–3.7 | 140 | 98 |
| | TSV 17Q NbTiN | 2958/3024 = 97.8<br>17Q yield = 68.5[a] | 21.6-29.5 | 800 | 681[a] |
| | | 2770/3024 = 91.6<br>17Q yield = 22.5[b] | 18.5-22.5 | 666 | 520[b] |
| Manhattan-style | Planar 17Q NbTiN | 2006/2176 = 92.2<br>17Q yield = 25.1 | 1.2–7 | 317 | 155 |
| | TSV 17Q NbTiN | 2867/3024 = 94.8<br>17Q yield = 40.3 | 7.5–18 | 342 | 306 |
| | Planar 35 × 35 NbTiN | 1176/1225 = 96.0 | 11.3 | 549 | 182 |
| | Planar 35 × 35 TiN | 1161/1225 = 94.8 | 8.9 | 446 | 172 |
| | Planar 35 × 35 Al | 1121/1155 = 97.0[c] | 6.8 | 251 | 119 |

[a] Without regression filtering.

[b] With regression filtering.

[c] Two rows were accidentally omitted during data acquisition.

The shadowing effect of these features makes

$$W'_{\mathrm{t}}(\vec{r}) \approx W_{\mathrm{t}} + \delta W_{\mathrm{offset}} - \begin{cases} W_{\mathrm{lip}}(\vec{r}) + H'(\vec{r})\,\frac{|y|}{D}, & \text{for } y \geqslant 0, \\ \max\left(H'(\vec{r})\,\frac{|y|}{D}, W_{\mathrm{lip}}(\vec{r}) + H'_{\mathrm{lip}}(\vec{r})\,\frac{|y|}{D}\right), & \text{for } y < 0, \end{cases} \tag{7}$$

where $H'(\vec{r}) = H + \delta H(\vec{r})$ and $H'_{\mathrm{lip}}(\vec{r}) = H_{\mathrm{lip}}(\vec{r}) + \delta H(\vec{r})$. Including all modeled effects leads to $A'_{\mathrm{overlap}}(\vec{r})$ as shown in figure 4(d).

The geometric model predicts that junction conductivity erroneously computed as $G/\Sigma A_{\mathrm{overlap}}$ will show a center-to-edge decrease. Experimental results for the three Planar 35 × 35 wafers clearly show this trend (figures 5(g)–(i)). In turn, the model predicts that conductivity computed as $G/\Sigma A'_{\mathrm{overlap}}$ will be flat. Due to the inaccuracy of approximating $A'_{\mathrm{overlap}}$ using top-view SEM images, a slight center-to-edge increase could even be observed. Conductivity computed as $G/\Sigma A'_{\mathrm{overlap}}$ is very uniform for the all-Al wafer, but not for the wafers with NbTiN and TiN probing pads. In these, the conductivity is very similar ($\sim$4 mS $\mu$m$^{-2}$) at wafer center, but decreases noticeably away from it. These observations suggest that series resistance from the contact region (nominally $32.4 \times 10^{-2}$ $\mu$m$^2$) between Al electrodes and the NbTiN or TiN bays is small at wafer center but increases significantly away from center. While the contact region area is also impacted by the geometric shadowing effect, fractionally the effect is much less significant than for the JJ overlap areas, and cannot explain the observation. Using circuit analysis, we can calculate the net contact series resistance per junction required to match the observed reduction in conductivity computed from $A'_{\mathrm{overlap}}$ at wafer edge. We find $\sim$2.3 kΩ for NbTiN pads and $\sim$900 Ω for TiN pads.

It remains important for future research to directly measure the magnitude and spatial dependence of this contact resistance, and to reduce both using bandaging layers [33, 36].

## 5. Conclusions

Table 1 summarizes the findings of our investigation of Dolan and Manhattan JJs on planar and TSV-integrated substrates, spanning yield, conductance CV and frequency RSD at wafer level, as well as average die-level RSD. For planar substrates, Dolan JJs perform best in all categories. In TSV-integrated substrates, Dolan JJs show a marked increase in disorder and decrease in yield, most likely due to their higher susceptibility to resist-height variation. Manhattan JJs are thus the preferred choice for TSV-integrated substrates, but their uniformity must be further improved. First, we must pre-compensate the spatial variation of junction overlap area that arises from the shadowing effect captured by the geometric model. For

the Manhattan-JJ resist stack used, the model predicts a narrowing of electrode widths by ∼60 nm from wafer center to edge (see figure S7). The resolution of our e-beam lithography system in 100 kV write mode is 5 nm, and thus it is possible in principle to pre-compensate the spatial variation in $A'_{\mathrm{overlap}}$. Next, the magnitude and strong spatial dependence of contact resistance between the Al electrodes and the NbTiN bays, only inferred from our data, should be quantified, understood, and hopefully diminished using bandaging layers. These improvements will allow to quantify the intrinsic disorder of Manhattan JJs and approach the ∼50 MHz target that will secure SQP yield by post-fabrication trimming using laser annealing.

## Data availability statement

The data that support the findings of this study are openly available at the following URL/DOI: http://github.com/DiCarloLab-Delft/Wafer_Scale_Fab_Data.

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## Additional information

The data shown in all figures of the main text and Supplementary Information are available at http://github.com/DiCarloLab-Delft/Wafer_Scale_Fab_Data. Correspondence and requests for additional materials should be addressed to L.D.C. (l.dicarlo@tudelft.nl).

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