EEL 3705L, Digital Logic Design Lab, Spring 2011

Lab Assignment #7:
LCD Display Controller & Clock

Version history:
v1.0, 3/17/11: Created the initial version of the assignment. –M. Frank
v1.1, 3/17/11: Corrected numbering of last 2 guiding questions. -MPF

1. Document description:

This document describes the 7th full lab assignment (& 3nd lab assignment after the midterm) for the Spring 2011 semester of EEL 3705L, Digital Logic Design Laboratory; this assignment's lab periods will take place the week of Mon. Mar. 21-Thu. Mar. 25.

2. Assignment Synopsis:

In this assignment, students will create a modular sequential logic design using VHDL finite-state machines to design & implement a controller for a real-world peripheral device of non-trivial complexity (a 2-line by 16-character liquid crystal display, Crystalfontz CFAH1602B-TMC-JP). The controller implementation must respect all of the signal timing constraints that are specified in the device datasheet (if it does not, then points will be deducted even if the design happens to work anyway). Once the controller is implemented, it must be used to display the team members' names and the current real time (from lab #6) on the LCD. This assignment is to be carried out as a structured design process. Students should design and test their circuits at home in the simulator, and then test their designs in lab on the DE2 boards.

3. Educational Objectives:

This assignment is intended to:

1. Give students practice at design & coding of substantial modular sequential designs using finite-state machines (FSMs) written in behavioral VHDL.
2. Give students experience interfacing with a real-world sequential peripheral device (LCD panel) with a serial/parallel control interface.
3. Give students practice at programming, simulating, and debugging substantial-sized modular sequential HDL-based designs using the Quartus tool.
4. Continue exercising students' ability to go through a structured design process with all appropriate documentation.

4. Design Objective:

In this assignment, your task is to design and prototype a sequential digital system in VHDL which uses the DE2 board's 2x16 LCD display to display your full name on the first line of the display, and the current time (from your digital clock you did for lab #6) on the second line. As part of this assignment, you must implement (from scratch!) a suitable LCD controller which respects all of the LCD panel's timing constraints, as specified in its datasheet, which can be found in the ZIP file of the DE2 system CD on Blackboard.

Note that your design ***MUST*** include an LCD controller that is created from scratch, and that respects all of the LCD module's documented timing constraints – if it is not, then you will not receive full credit, even if your design still appears to work perfectly. (Because, if you violate specifications, you cannot assume your design will always work reliably!) Thus, you must show your TA the code in your design that guarantees that all the LCD timing constraints will be met. The time should be displayed like "12:59:59 AM" and must be updated in real time, at least once per second. You must include the colons and the AM/PM indicator. For extra credit, also include the hundredths of seconds, like "12:59:59.99 AM." (Your LCD driver will have to be very efficient for that to work well!)

The design should be coded in a modular style, with emphasis on VHDL. Most of your modules should be written in sequential VHDL, in a behavioral style using process statements, with statements to update state variables.

5. Pre-Lab Preparation:

Note: For your final lab report for this assignment, you must follow the more detailed lab report format that you were required to use in Lab #1. This is practice for the more detailed series of design reports you will be required to do for your final project, which is in turn practice for senior design. However, to save you time, your pre-lab version of the report can be more abbreviated.

Reminder: You MUST complete the pre-lab assignment BEFORE coming to lab, and turn in your pre-lab report printout at the start of lab.

5.1. Guiding Questions

The following questions are intended to help guide and stimulate your thought process as you work through this assignment. As you gain experience, eventually you will be able to go through this type of thought process on your own, without being prompted.

Question #1. Think about (and sketch a high-level block diagram of) your overall system architecture. Decompose it into a set of interacting sequential modules (FSMs). Do not try to design the entire application as a single monolithic FSM (a single VHDL process) – that approach is unacceptable; it would be more difficult to design/debug, and it would not scale well to higher levels of design complexity.

For example, your high-level design could include the following major modules:

- A clock module that continuously outputs signals representing the different parts of the current time (hour, minute, second). This can include appropriate modules from lab 6, slightly modified to include AM/PM information.
- An LCD controller module that accepts LCD commands to be executed, sends those commands to the LCD in a way that respects the LCD's timing constraints, and outputs a "done" pulse or clock-edge when it is ready to process the next command.
- A system control module, which waits for different components of the time to change, & sends the LCD controller the sequence of commands needed to update the display accordingly.

Question #2. What will you use as your time reference(s) in the design? You do not necessarily have to use the same clock in all parts of your design. But in your LCD controller, to achieve maximum performance, you will probably want to use the fastest clock signal available. (You may even want it to be dual edge-triggered.)

Question #3. Design a simple finite-state machine for your LCD controller. I advise that it should accept the following input: An LCD command word (how many bits wide is it, including the control signals RS, RW, EN as well as the data?), a trigger pulse signal (where an active edge on that signal means, "send this command now"). And it should have a least one output bit, a "done" signal which tells the client (the module using this module) that the command has been sent & enough time has passed, and it is now ready to accept & send the next command. Make sure that your FSM respects all of the timing constraints from the LCD datasheet, including all setup & hold times, & all pulse width constraints!

Question #4. Design a top-level FSM for your overall application. It may help to first write out the algorithm as a flowchart or as pseudocode. Basically, it will need to have four parts: (1) initialize the LCD, via the sequence of commands & delays from sec. 14 of the datasheet; (2) send the sequence of characters representing your name. These can come from a ROM, or you can hard-code them into your FSM. (3) Write the colon (":") characters between the parts of the time, (4) Go into a state loop where you check for different components of the time to change, and if they have changed (since the last time through the loop), then write out the appropriate ASCII digits to the LCD at the appropriate locations. You could re-write all digits of the time to the display every time through the loop (that would be a little simpler), but that might slow down your display and cause unnecessary flickering of the LCD.

Question #5. By this point, you should have sketched out the basic structure and/or function of all your modules in block diagrams, flowcharts and/or pseudocode in your lab notebook. Now it's time to actually implement them in VHDL and/or schematics – although you should emphasize VHDL, as the problem statement specified.

Question #6. Think about design-for-test considerations, and plan ahead for prototype testing. Like in earlier labs, you may want to tap out some extra signals for testing purposes, signals which will help you diagnose any problems in the design. For example, if you also still display the current time on the 7-segment display like you did in lab 6, this will help you isolate problems with the time display on the LCD. Or, you may want to display values of state variables on the 7-segment display or on LEDs. To debug any timing problems in your LCD controller, you may find it helpful to use an oscilloscope – there are a few in the lab you can use, and you can tap out any desired signals to the GPIO headers for testing.

5.2. Pre-Lab Report Format

For the pre-lab version of the report for this assignment, you may follow the generic pre-lab report format that is given in the *General Lab Requirements* document. This format

is a little bit simpler than the one you had to use for lab #1. However, your final lab report will need to be more detailed – see section 7 below.

6. In-Lab Procedure:

In lab this week, you should load and test your design, according to the experimental testing procedure that you already came up with in your pre-lab report. As you go along (at home and in lab), take detailed notes in your lab notebook (in accordance with the Lab Report Requirements section of the *General Lab Requirements* document) that you will base your final report on. Be sure to take note of anything that happens during prototype testing that is different from what you expected, and take detailed notes that you will use for analysis and interpretation of your experimental results in your final lab report. If any design modifications turn out to be needed, go ahead and make them, and re-test the design until it is working. Before leaving the lab, demonstrate to the TA that your full name appears on the 1st line of the LCD display, that the real time appears on the 2nd line, and that you can set it. Also show the TA your code that guarantees that the LCD timing constraints are met. Remember to turn in your final lab report the following week.

7. Post-Lab Procedure:

For this assignment, for your final lab report, you should try follow the more detailed lab report format that you were required to use way back in Lab #1. This is to gear you up for the more detailed sequence of design reports that you will be required to do for your final project.