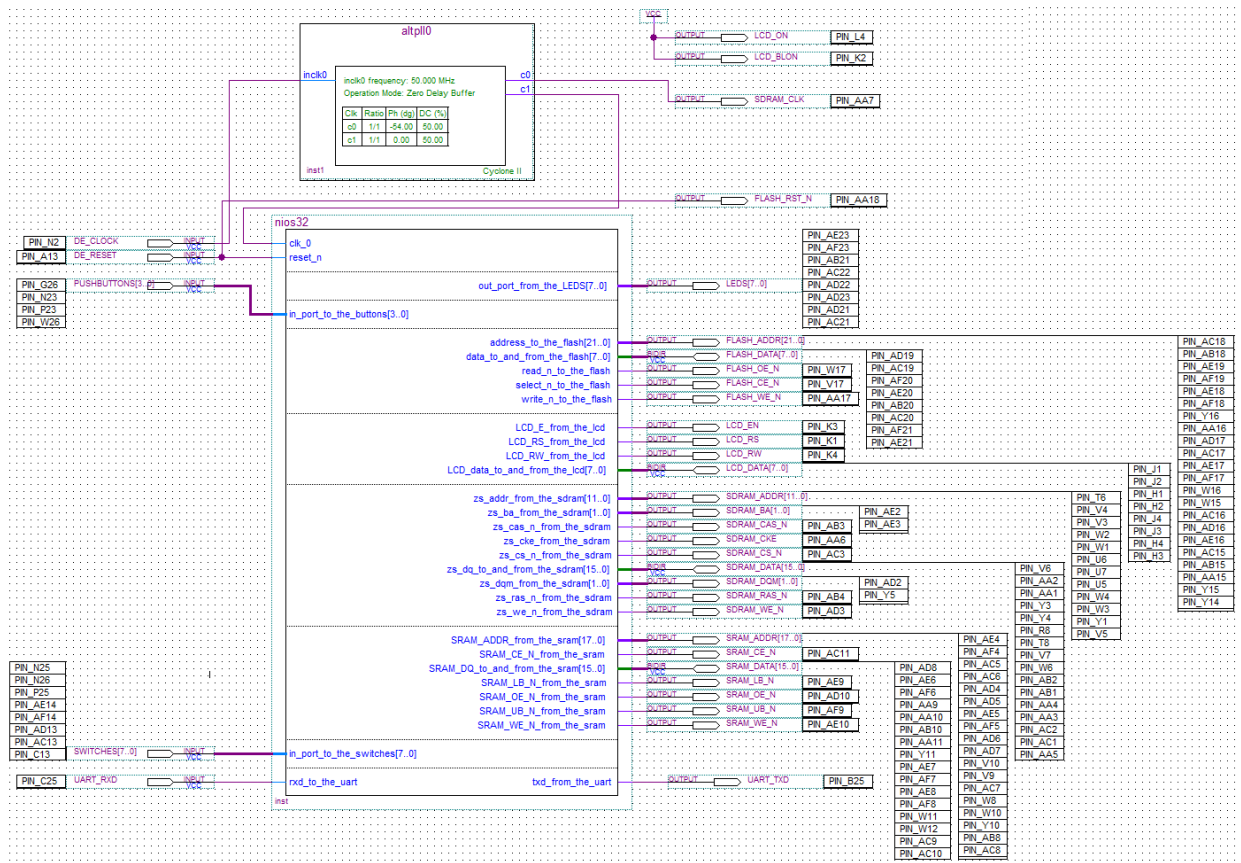


**Homework 6****Top Level BDF Graphic**

## SPOC Snapshot

Target

Device Family: Cyclone II

Clock Settings

Name	Source	MHz
clk_0	External	50.0

Use	Connecti...	Module Name	Description	Clock	Base	End	Tags	IRQ
<input checked="" type="checkbox"/>		<b>cpu</b>	Nios II Processor	clk_0				
		instruction_master	Avalon Memory Mapped Master					
		data_master	Avalon Memory Mapped Master					
		jtag_debug_module	Avalon Memory Mapped Slave		0x01900800	0x01900fff	IRQ 0	IRQ 31
<input checked="" type="checkbox"/>		<b>jtag_uart</b>	JTAG UART	clk_0				
		avalon_jtag_slave	Avalon Memory Mapped Slave	clk_0	0x01901080	0x01901087		
<input checked="" type="checkbox"/>		<b>uart</b>	UART (RS-232 Serial Port)	clk_0	0x01901000	0x0190101f		
<input checked="" type="checkbox"/>		<b>timer</b>	Interval Timer					
		s1	Avalon Memory Mapped Slave	clk_0	0x01901020	0x0190103f		
<input checked="" type="checkbox"/>		<b>buttons</b>	PIO (Parallel IO)					
		s1	Avalon Memory Mapped Slave	clk_0	0x01901040	0x0190104f		
<input checked="" type="checkbox"/>		<b>switches</b>	PIO (Parallel IO)					
		s1	Avalon Memory Mapped Slave	clk_0	0x01901050	0x0190105f		
<input checked="" type="checkbox"/>		<b>LEDs</b>	PIO (Parallel IO)					
		s1	Avalon Memory Mapped Slave	clk_0	0x01901060	0x0190106f		
<input checked="" type="checkbox"/>	<b>sram</b>	SRAM/SSRAM Controller						
	avalon_sram_slave	Avalon Memory Mapped Slave	clk_0	0x01880000	0x018fffff			
<input checked="" type="checkbox"/>	<b>sdram</b>	SDRAM Controller						
	s1	Avalon Memory Mapped Slave	clk_0	0x00800000	0x00ffffff			
<input checked="" type="checkbox"/>	<b>lcd</b>	Character LCD						
	control_slave	Avalon Memory Mapped Slave	clk_0	0x01901070	0x0190107f			
<input checked="" type="checkbox"/>	<b>ext_bus</b>	Avalon-MM Tristate Bridge						
	avalon_slave	Avalon Memory Mapped Slave	clk_0					
	tristate_master	Avalon Memory Mapped Tristate Master						
<input checked="" type="checkbox"/>	<b>flash</b>	Flash Memory Interface (CFI)						
	s1	Avalon Memory Mapped Tristate Slave	clk_0	0x01400000	0x017fffff			

## Resource Data

Flow Status	Successful - Wed Oct 23 11:22:57 2013
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Full Version
Revision Name	rpds17
Top-level Entity Name	rpds17
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	3,535 / 33,216 ( 11 % )
Total combinational functions	3,287 / 33,216 ( 10 % )
Dedicated logic registers	2,044 / 33,216 ( 6 % )
Total registers	2145
Total pins	148 / 475 ( 31 % )
Total virtual pins	0
Total memory bits	46,720 / 483,840 ( 10 % )
Embedded Multiplier 9-bit elements	4 / 70 ( 6 % )
Total PLLs	1 / 4 ( 25 % )