EEL 4710 Intro to FPLDs
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Spring 2012
Assignment #2 40 points
Due February 7

1. Write VHDL code to implement an arithmetic logic unit that implements the following functions on the 8-bit inputs *x* and *y* to generate an 8-bit output *z,* and a 1-bit output *cout.* Three select lines *s0, s1,* and *s2* are used to determine the function chosen. Use std_logic_vector for *x, y, s,* and *z.* Use std_logic for *cout.*

s2	*s1*	*s0*	*function*
0	0	0	Bit-wise AND
0	0	1	Bit-wise OR
0	1	0	Bit-wise XOR
0	1	1	Bit-wise NAND
1	0	0	Addition (x+y)
1	0	1	Subtraction (x-y)
1	1	0	Increment x (x+1)
1	1	1	Increment y (y+1)

2. Simulate the VHDL code you designed for part 1. Use Quartus or modelsim to generate a timing diagram. Show correct operation for each combination of select lines for several interesting inputs. Use your simulator's capability to group lines together and to show the input and output values using hexadecimal representation.

You must turn in a hardcopy and an electronic copy. The electronic copy should include a document that includes the timing diagram, and a zipped copy of your code.