

Async Parallel Processor Demonstrator

- Author: Paul Schulz
- Description: Asynchronous Parallel Processor Model
- Language: Verilog

How it works

This circuit is an investigation into an asynchronous parallel processor.

A processing node follows the following state flow: - Wait for valid data; - Process the data to produce an output value, and let neighbors know that processing is being done; - Make the result available; and wait for more data to process.

In this example, the processing node is doing a calculation on four(4) inputs of 4 bits, based on the "Arctic Circle Theorem" model. (video)

How to test

TBD

Experiment by changing the input values.

IO

#	Input	Output	Bidirectional
0	input bit 0	segment a	second counter bit 0
1	input bit 1	segment b	second counter bit 1
2	input bit 2	segment c	second counter bit 2
3	input bit 3	segment d	second counter bit 3
4	load input 0	segment e	second counter bit 4
5	load input 1	segment f	second counter bit 5
6	load input 2	segment g	second counter bit 6
7	load input 3	dot	second counter bit 7

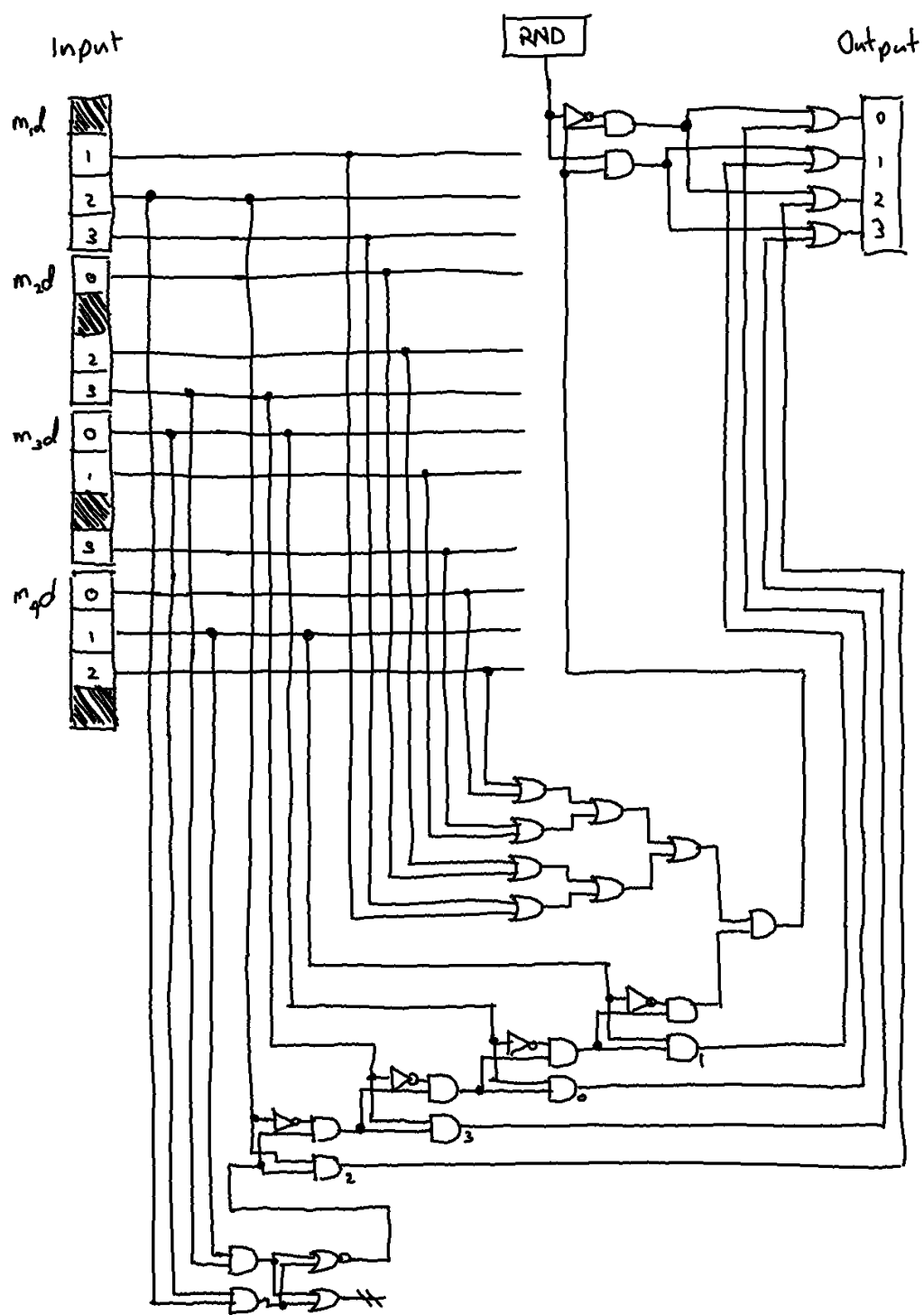


Figure 1: picture