Brac University

CSE 350: Digital Electronics and Pulse techniques

Exp-04: Analysis of the binary weighted D/A converter

Name:	Section:
ID:	Group:

Objectives

1. To construct binary weighted D/A converter
2. Verifying that the digital signal is converted to a proportional analog signal

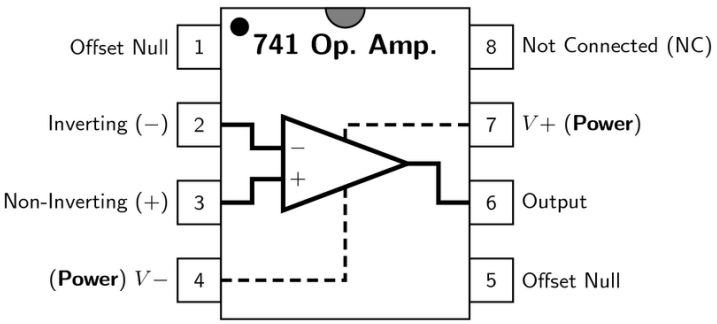
Equipment and component list

Equipment

1. Digital Multimeter
2. DC power supply

Component

- Operational amplifier - UA741 - x1 piece
- Resistors -
  - 10 KΩ - x1 piece
  - 5 KΩ - x1 piece
  - 2.5 KΩ - x1 piece
  - 1.25 KΩ - x1 piece
  - 1 KΩ - x1 piece



741 IC pin diagram

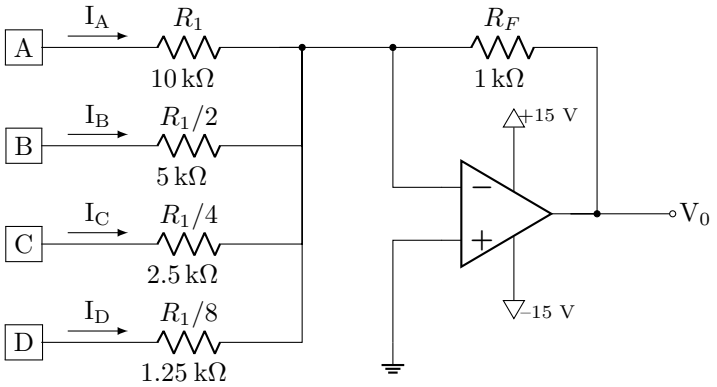


Figure 1: Binary weighted D/A converter

Task-01: Binary weighted D/A converter

THEORY

A four bit converter will have $2^4 = 16$ input combinations. Consequently, the converter will show 16 different output analog voltage levels for 16 different input combinations.

Case 1: (D, C, B, A) = (0, 0, 0, 1)

The voltage across R_1 is 5V. So, the current through R_1 is $I_A = 0.5$ mA. Since the current into the op-amp input terminals are negligible, this 0.5 mA current will flow through the R_F resistance. Hence, the voltage across the resistance R_F is, V_{R_F}= 0.5 mA × 1 KΩ = 0.5 V. Consequently, the output voltage is -0.5V.

Case 2: (D, C, B, A) = (0, 0, 1, 0)

The voltage across $R_1/2$ is 5V. So, the current through $R_1/2$ is $I_B = 1$ mA. Since the current into the op-amp input terminals are negligible, this 1 mA current will flow through the R_F resistance. Hence, the voltage across the resistance R_F is, V_{R_F}= 1 mA × 1 KΩ = 1V. Consequently, the output voltage is -1V.

Case 3: (D, C, B, A) = (0, 0, 1, 1)

The voltage across R_1 is 5V and the voltage across $R_1/2$ is 5V. The current through R_1 is $I_A = 0.5$ mA and the current through $R_1/2$ is $I_B = 1$ mA. So, the total current through the resistance is 1.5 mA. Hence, the voltage across the resistance R_F is, V_{R_F}= 1.5 mA × 1 KΩ = 1.5V. Consequently, the output voltage is -1.5V.

Similarly, we can calculate the output voltage for any other input combination. The relationship between the digital input values and the corresponding analog output levels is presented in the staircase plot in figure 2.

The output is a negative going staircase waveform with 15 steps of -0.5V each. In practice, due to the variations in the logic HIGH voltage levels, all the steps will not have the same size. The value of the feedback resistor R_F changes the size of the steps. Thus, a desired size for a step can be obtained by connecting appropriate feedback resistor. The only condition to look out for is that the maximum and minimum output voltages should not go beyond the saturation levels of the op-amp.

We can find that the output voltage is defined by the expression:

$$V_o = \left(\frac{V_A}{R_1} + \frac{V_B \times 2}{R_1} + \frac{V_C \times 4}{R_1} + \frac{V_D \times 8}{R_1}\right) \times (-R_F) \tag{1}$$

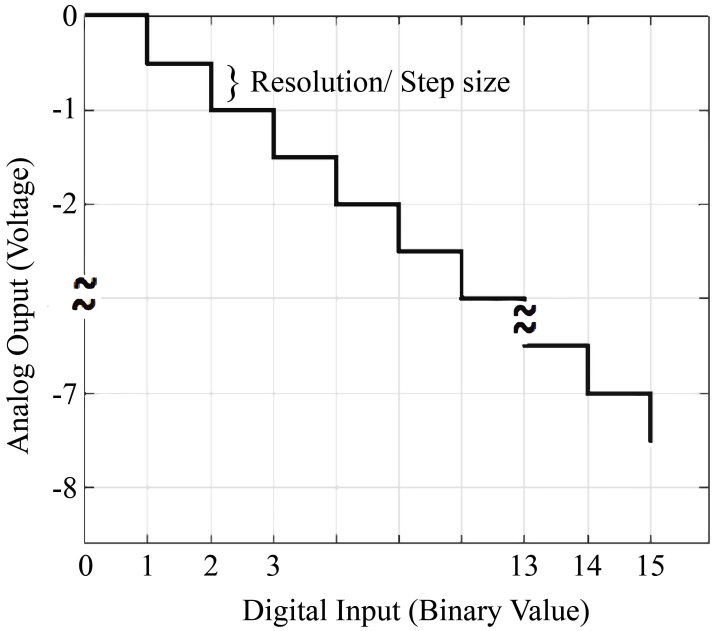


Figure 2: Staircase plot of output vs input in binary weighted D/A converter.

The x-axis of the plot represents the digital input values expressed in binary form. The y-axis represents the analog output voltage levels generated by the DAC in response to these digital inputs. The staircase appearance of the plot reflects the quantization process inherent in DAC operation. Each step corresponds to a specific digital input value, resulting in a discrete change in the analog output. This quantization means that the output can only take on certain values. The height of each step in the staircase plot indicates the resolution or step size of the DAC. A higher resolution DAC will have smaller steps, allowing for finer adjustments in the analog output. Conversely, a DAC with lower resolution will have larger steps, resulting in a more abrupt change in output for each increment in digital input. To find the resolution, one just needs to find the change in output analog voltage for one LSB change in digital input.

As this DAC circuit is fundamentally an inverting summing amplifier, the output is negative, and decreases as we increase the digital input. This is the result of the inverting nature of this configuration.

Procedure:

1. Construct the circuit on breadboard. Supply +15V and –15V to the op amp.
2. Consider the HIGH input to be 5V and the LOW input to be 0V.
3. Use multimeter to measure the output voltage for different input combinations. This output voltage is the 'analog' output signal. Fill up table 1.
4. Complete tasks 2 and 4 in the **Report** section

Precautions:

1. For the digital inputs, do not use the switches from the trainer board. The DAC might not work properly due to current limit of the switches. You can use the 5V source of the trainer board or use DC power supply. If you are using multiple power supplies (trainer board and DC power supply simultaneously), make sure to connect the grounds of each individual supply.
2. For the op amp supply voltage, use the +15V and -15V from the trainer board (top left). Make sure to adjust the knobs to get the desired voltages.
3. Use minimal number of wires. Unnecessary wiring increases the probability of errors.
4. Build the circuit similar to the layout of the given circuit diagram, such that debugging is easier if anything goes wrong.

Data Tables

In all the data tables, write the input combinations in ascending order.

SL	$V_D(V)$	$V_C(V)$	$V_B(V)$	$V_A(V)$	$V_Y(V)$
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

Table 1: Table for binary-weighted D/A converter

$\overline{Signature}$

Report

Please answer the following questions briefly in the given space.

1. Find the resolution of the D/A converter.

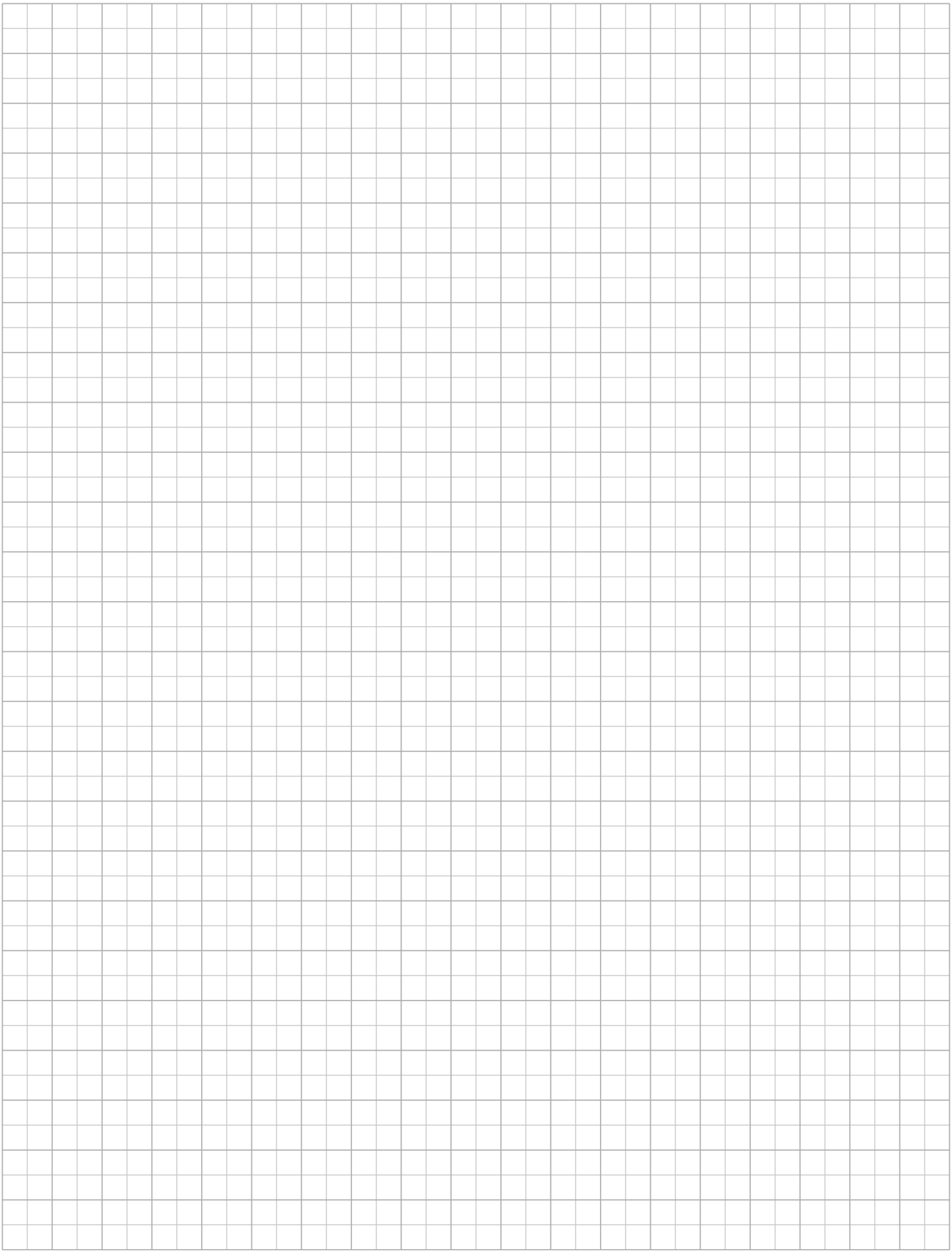
Ans.

2. For the D/A converter, change the value of R_F (feedback resistance) to $0.5\times R_F$ and then to $2\times R_F$. For each case, measure output voltage for any two consecutive input combinations and calculate the step sizes. Does the effect on step size match with the theory?

Ans.

3. How can you get output lower than -15 V in the above D/A converter?
Ans.

4. Plot the results obtained in table 1 in the given graph paper. Keep the serial no of inputs in the horizontal axis and the output voltages in the vertical axis.



Graph paper for table 1