library ieee;

use ieee.std\_logic\_1164.all;

entity led\_blink is

port (

i\_clk : in std\_logic;

i\_rst\_n : in std\_logic;

o\_led : out std\_logic

);

end entity led\_blink;

architecture rtl of led\_blink is

signal r\_led : std\_logic := '0';

begin

process(i\_clk, i\_rst\_n)

variable counter : natural range 0 to 5000000 := 0;

begin

if (i\_rst\_n = '0') then

counter := 0;

r\_led <= '0';

elsif (rising\_edge(i\_clk)) then

if (counter = 5000000) then

counter := 0;

r\_led <= not r\_led;

else

counter := counter + 1;

end if;

end if;

end process;

o\_led <= r\_led;

end architecture rtl;