ALINX FPGA BOARD

AX7102

User Manual

ALINX

Development Environment:
Vivado 2015.4 is from Xilinx website
https://www.xilinx.com

Official website:
Http://www.alinx.com.cn

E-mail:
avic@alinx.com.cn

Tel:
+86-021-67676997

WeChat public number：
ALINX-HEIJIN

Contents

一、 Overview 6
二、 FPGA Core Board 8
(一) Overview 8
(二) FPGA 9
(三) CLOCK 11
(四) DDR3 14
(五) QSPI Flash 17
(六) LEDs 19
(七) RESET Button 20
(八) JTAG Interface 21
(九) Power Input 22
(十) Board-to-Board Connector 23
(十一) POWER 31
(十二) Mechanical 34
三、 Expansion Board 35
(一) Overview 35
(二) Gigabit Ethernet 36
(三) SFP Interface 38
(四) VGA Port 40
(五) USB2.0 42
(六) SD Socket 45
(七) USB Serial Port 46
(八) RS232 接口 48
(九) EEPROM 24LC04 49
(十) RTC 50
(十一) GPIO Expansion Headers 51
(十二) JTAG Interface 55
(十三) Buttons 55

(十四) LED 56
(十五) POWER.....57

The AX7102 development Kit presents a robust hardware design platform built around the XILINX Artix-7 FPGA, which optimized for lowest cost and power with small form-factor packaging for the highest volume applications. The AX7102 development board is equipped with high-speed DDR3 memory, SFP networking, and USB2.0 capabilities, Ethernet networking, and much more other resource that promise many exciting applications.

This ARTIX-7 FPGA development platform includes core board and expansion board, so that users can reuse the core board in their own projects conveniently. The kit contains complete reference designs and source code for each part on board. it is a good choice for students or FPGA engineers to learn Artix-7 FPGA and do evaluation base on it. This document provides users key information about the kit. Figure1-1 shows a photograph of the whole board.

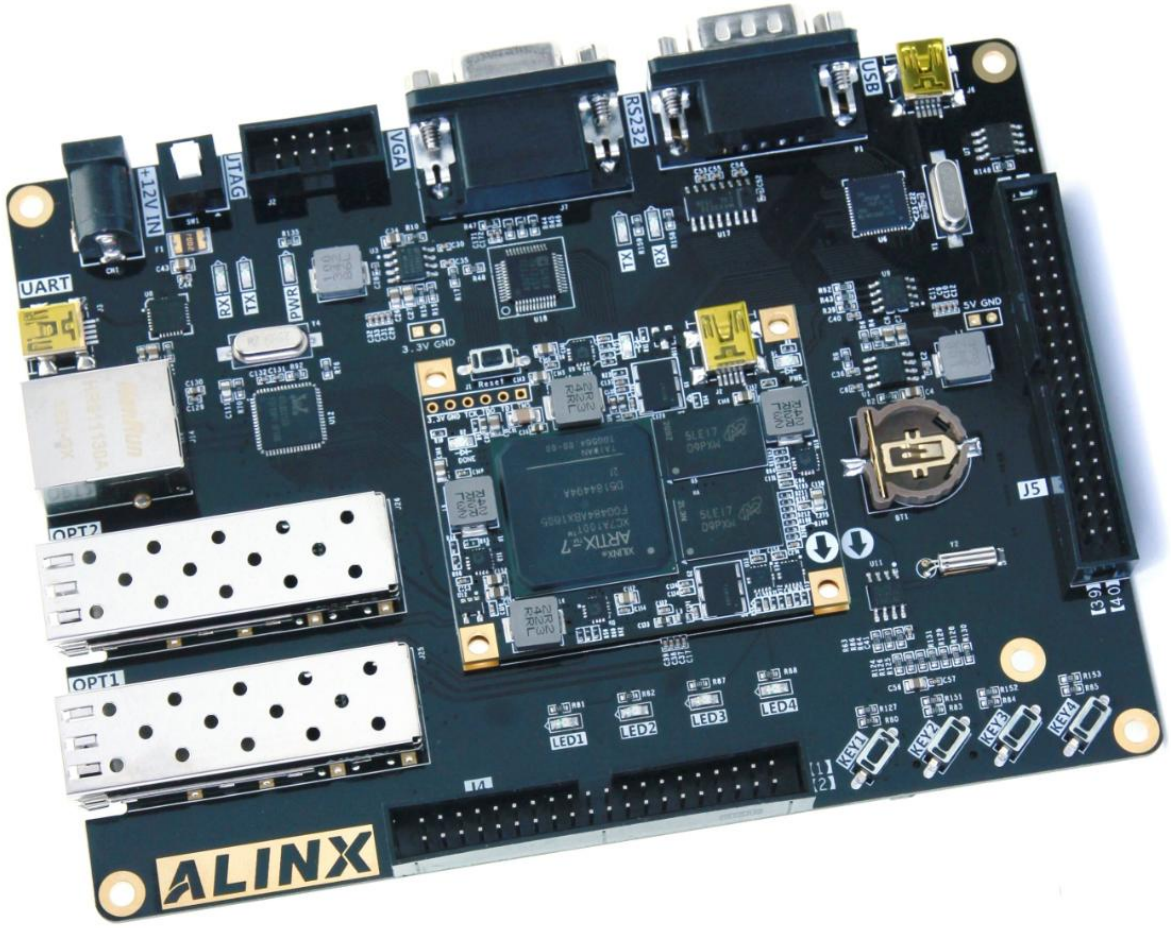


Figure1-1 AX7102 Overview

一、 Overview

The AX7102 board comprises FPGA core board and expansion board, four high-speed board-to-board connectors are used to connect between the core board and the expansion board.

The core board is a minimal systems which mainly consists of FPGA chipset, two DDR3 and QSPI FLASH. The expansion board extends the many peripheral interface for core board, which contains SFP fiber interface, gigabit Ethernet network port, USB2.0 port, VGA port and etc.

Figure 1-2 provides a quick overview of the block diagram of AX7102 board.

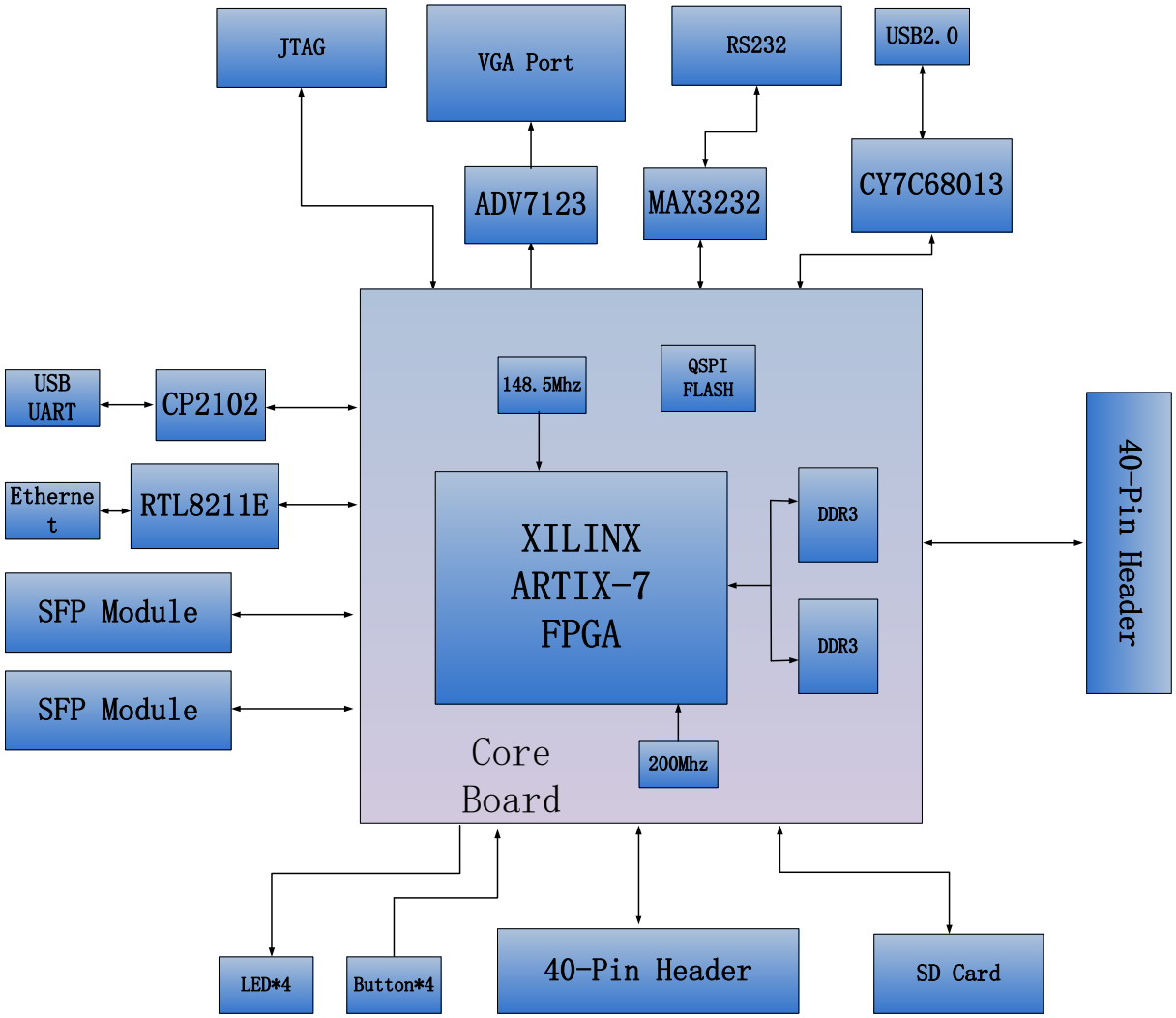


Figure 1-2 AX7102 Block Diagram

The following hardware resources are provided on the AX7102 board:

Features of FPGA Core Board:

- **FPGA Device**
  - XILINX ARTIX-7 FPGA XC7A100T ;
  - 101,440 Logic Cells;
  - 240 DSP48 Slices include 18 x 18 multiplier, an adder, and accumulator;
  - 4860Kb Block RAM Blocks;

- **Memory**
  - 2pcs 4Gbit(256M x 16bit) DDR3 memory make up to 8Gbit size in total.
  - 128 Mb QSPI FLASH.

- **CLOCK**
  - 200Mhz differential crystal oscillator for system clock.
  - 148.5MHz differential crystal oscillator for GTP transceiver.

Features of FPGA Expansion Board:

- **Communication**
  - 10/100/1000 Ethernet;
  - Two Port of SFP Interface.
  - USB2.0 Port;
  - USB-to-Serial port;
  - RS232 Serial Port;
  - Real-Time Clock;
  - EEPROM with I2C interface;
  - Micro SD Socket;

- **Connectors**
  - Two 40pin Expansion Headers(it can connect 4.3' LCD module, ADDA module, Audio module etc.);
  - 10pin 2.54mm JTAG connector;

- **Display**

- 24-bit DAC of VGA output ;

- **Buttons and Indicators**
  - 5 User LEDs and (one is on core board);
  - 5 user Buttons (one button acts as reset button on core board);

二、 FPGA Core Board

(一) Overview

AC7100 (P/N of Core Board) is a high performance core board using XILINX Artix-7 XC7A100T-2FGG484I chipset. Two DDR3 memory is connected to FPGA with 32bit data width and one 128Mbit QSPI FLASH is used for storage of FPGA bitstreams or application code.

About 180 IOs (include 86 pairs LVDS signals) and signals of GTP transceivers are extended to expansion board using board-on-board connector. The core board is very small of 45*55 (mm) size, it will be a good choice to use this core board in project which need a lot of IOs and space limitation.

Figure 2-1-1 and Figure 2-1-2 shows the top view and bottom view of the FPGA Core board.

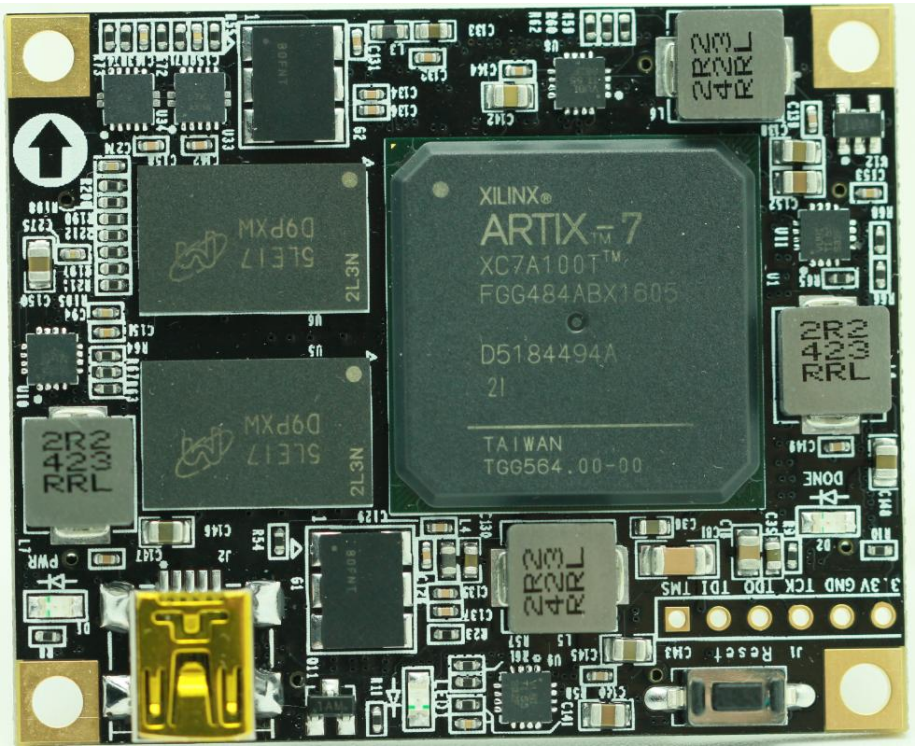


Figure2-1-1 AC7100 TOP View

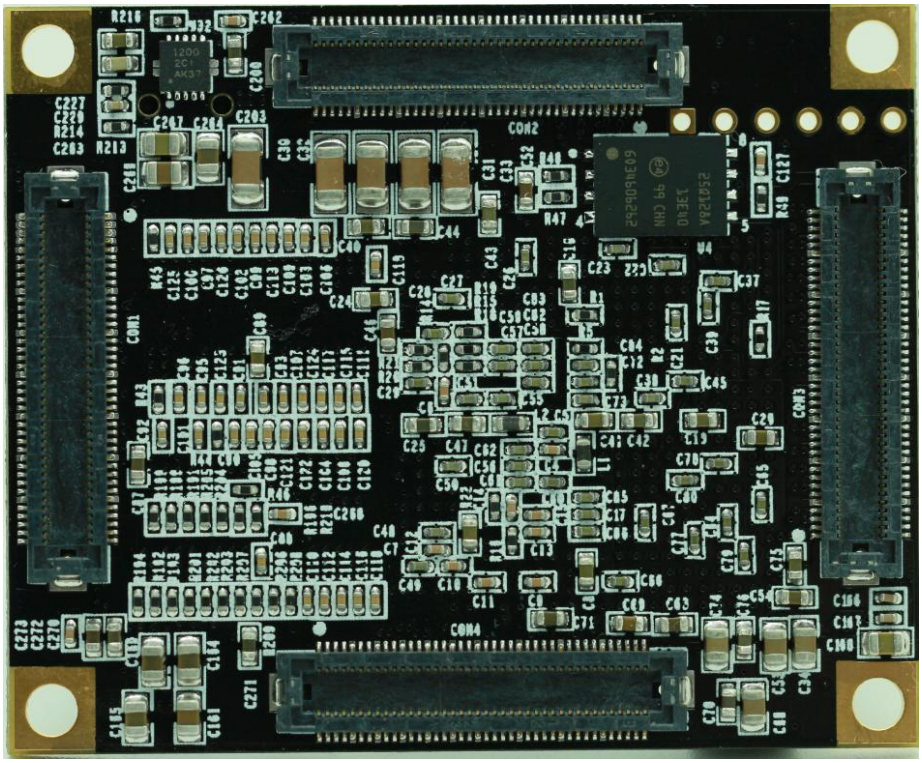


Figure 2-1-2 AC7100 Bottom View

(二) FPGA

AC7100 Core board uses Xilinx Artix-7 FPGA device, the detail part number is

XC7A100T-2FGG484I. The Xilinx Artix-7 FPGA ordering information is shown in Figure 2-2-1.

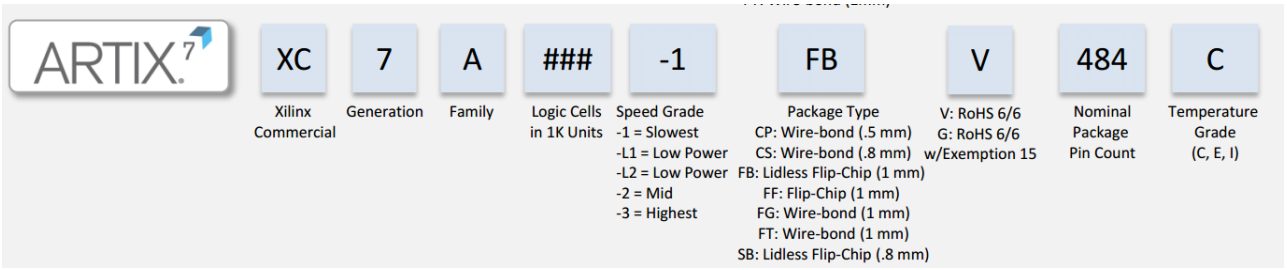


Figure 2-2-1 Artix-7 Ordering Information

Figure 2-2-2 shows the FPGA chipset on AC7100 core board.

Figure 2-2-2 FPGA Chipset

The feature summary of XC7A100T is listed as following:

Items	Parameters
Logic Cells	101440
Slices	15850
Max Distributed RAM(Kb)	1188
Block RAM (kb)	4860
DSP48E1 Slices	240

CMTs	6
PCIe Gen2	1
XADC	1 个 12bit, 1Mbps AD
GTP Transceiver	4 个 , 6.6Gb/s max
Speed	-2
Operation Temperate	-40 ~ 85degree

FPGA Power Supply

Artix-7 FPGA has six power supplies including V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCO}, $V_{MGTAVCC}$ and $V_{MGTAVTT}$. V_{CCINT} is the core power supply of FPGA and should be connected to +1.0V. V_{CCBRAM} is power supply of FPGA Block RAM and also should be connected to +1.0V. V_{CCAUX} is FPGA auxiliary power supply and should be connected to +1.8V. V_{CCO} is each BANK power supply, because the IOs of FPGA bank35 is connected to the DDR3, the V_{CCO} voltage of bank35 should be +1.5V. V_{CCO} of Bank15 and Bank16 is power from a LDO chipset, so the voltage of these two bank can be changed if we use different LDO chipset. $V_{MGTAVCC}$ is the power supply of GTP transceiver, it should be connected to +1.0V. $V_{MGTAVTT}$ is terminal power supply of the GTP transceiver, and should be connected to the +1.2V.

The Artix-7 FPGA has the Power-On/Off Power supply sequencing, the recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on.

(三) CLOCK

AC7100 core board is equipped with two Sitime differential crystal oscillators , one is 200Mhz differential crystal oscillator for FPGA system clock, another is 148.5Mhz differential crystal oscillator for GTP transceiver.

1). 200Mhz Differential Crystal Oscillator

The Figure 2-3-1 is the circuit of 200Mhz system clock, the output of differential crystal oscillator is connected to global clock pin MRCC (R4 and T4) of FPGA.

This 200Mhz system clock can produce different frequency clock to drive the user logic thought PLLs and DCMs inside FPGA.

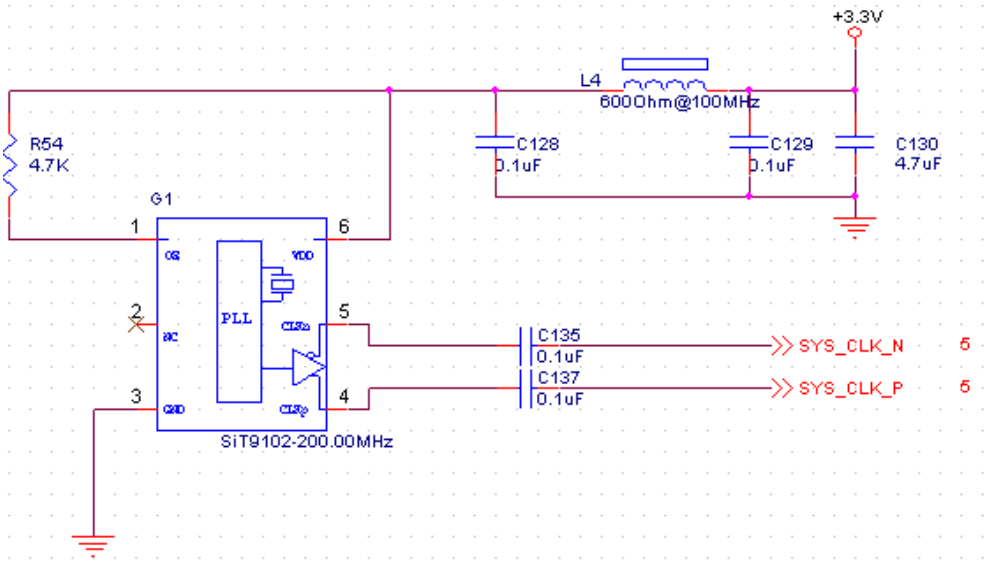


Figure 2-3-1 200Mhz System Clock

Figure 2-3-2 shows the onboard 200Mhz differential crystal oscillator

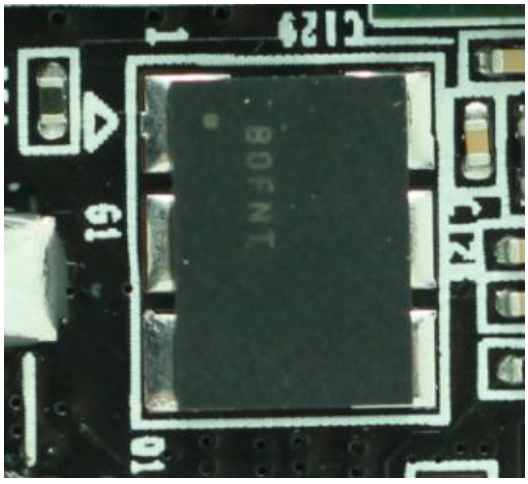


Figure 2-3-2 Onboard 200Mhz Crystal Oscillator

Clock Pin Assignment.

Net Name	FPGA PIN
SYS_CLK_P	R4
SYS_CLK_N	T4

2). 148.5Mhz Differential Crystal Oscillator

The Figure 2-3-3 is the circuit of 148.5Mhz clock for GPT transceiver. The output of differential crystal oscillator is connected to MGTREFCLK0P pin(F6) and MGTREFCLK0N pin(E6) of FPGA bank216.

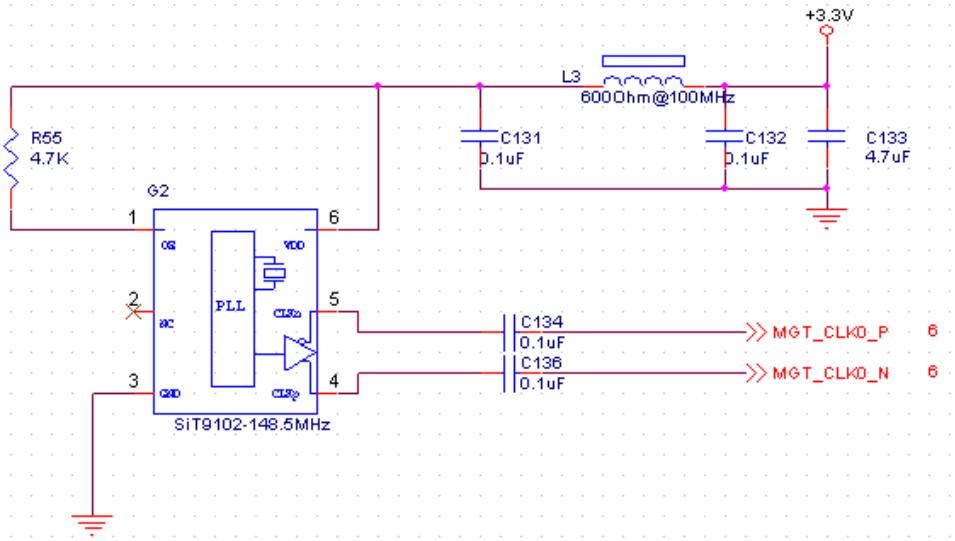


Figure 2-3-3 148.5Mhz Differential Crystal Oscillators

Figure 2-3-4 shows the onboard 148.5Mhz differential crystal oscillator.

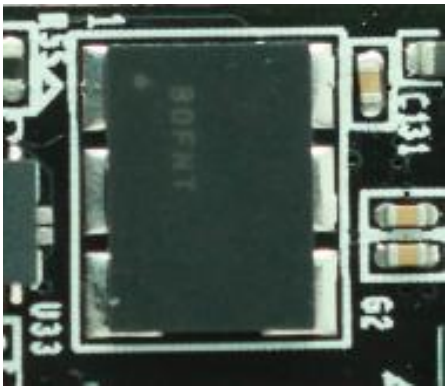


图 2-3-4 Onboard 148.5Mhz Crystal Oscillator

Clock Pin Assignment.

Net Name	FPGA PIN
MGT_CLK0_P	F6
MGT_CLK0_N	E6

(四) DDR3

The core board features 1GB of DDR3 memory, implemented using two 512MB DDR3 devices. The data bandwidth is in 32-bit, comprised of two x16 devices with a single address/command bus. the target clock speed for FPGA and DDR3 is 800 MHz(Data rate is 1600M). The part number of equipped two DDR3 devices is Micron MT41J256M16HA-125 which is compatible with MT41K256M16HA-125. Detail information of DDR3 SDRAM is shown in table 2-4-1 below.

Table 2-4-1 DDR3 SDRAM Information

Part	P/N	Capacity	Vender
U5,U6	MT41J256M16HA-125	256M x 16bit	Micron

Connections between FPGA and DDR3 are shown in Figure 2-4-1.

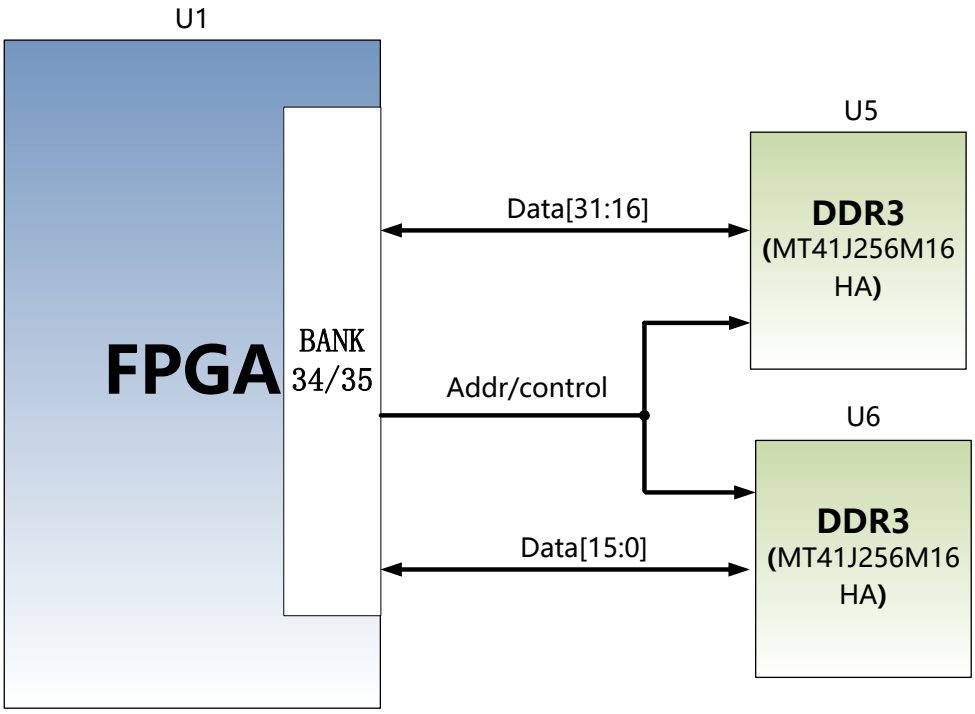


Figure 2-4-1 Connections between FPGA and DDR3

Figure 2-4-2 shows onboard two DDR3 SDRAM.

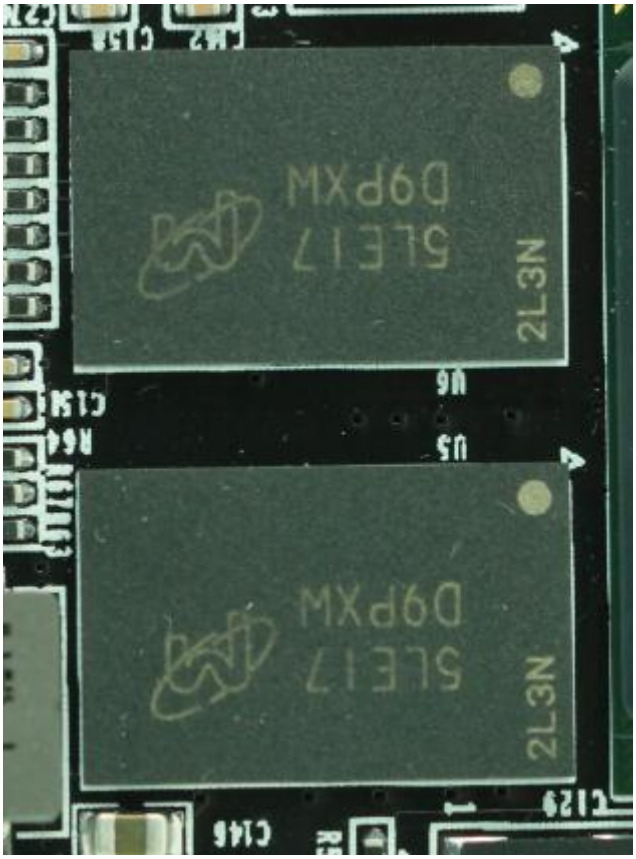


Figure 2-4-2 DDR3 SDRAM Onboard

DDR3 SDRAM PIN Assignment :

Net Name	FPGA PIN Name	FPGA P/N
DDR3_DQS0_P	IO_L3P_T0_DQS_AD5P_35	E1
DDR3_DQS0_N	IO_L3N_T0_DQS_AD5N_35	D1
DDR3_DQS1_P	IO_L9P_T1_DQS_AD7P_35	K2
DDR3_DQS1_N	IO_L9N_T1_DQS_AD7N_35	J2
DDR3_DQS2_P	IO_L15P_T2_DQS_35	M1
DDR3_DQS2_N	IO_L15N_T2_DQS_35	L1
DDR3_DQS3_P	IO_L21P_T3_DQS_35	P5
DDR3_DQS3_N	IO_L21N_T3_DQS_35	P4
DDR3_DQ[0]	IO_L2P_T0_AD12P_35	C2
DDR3_DQ [1]	IO_L5P_T0_AD13P_35	G1
DDR3_DQ [2]	IO_L1N_T0_AD4N_35	A1
DDR3_DQ [3]	IO_L6P_T0_35	F3

DDR3_DQ [4]	IO_L2N_T0_AD12N_35	B2
DDR3_DQ [5]	IO_L5N_T0_AD13N_35	F1
DDR3_DQ [6]	IO_L1P_T0_AD4P_35	B1
DDR3_DQ [7]	IO_L4P_T0_35	E2
DDR3_DQ [8]	IO_L11P_T1_SRCC_35	H3
DDR3_DQ [9]	IO_L11N_T1_SRCC_35	G3
DDR3_DQ [10]	IO_L8P_T1_AD14P_35	H2
DDR3_DQ [11]	IO_L10N_T1_AD15N_35	H5
DDR3_DQ [12]	IO_L7N_T1_AD6N_35	J1
DDR3_DQ [13]	IO_L10P_T1_AD15P_35	J5
DDR3_DQ [14]	IO_L7P_T1_AD6P_35	K1
DDR3_DQ [15]	IO_L12P_T1_MRCC_35	H4
DDR3_DQ [16]	IO_L18N_T2_35	L4
DDR3_DQ [17]	IO_L16P_T2_35	M3
DDR3_DQ [18]	IO_L14P_T2_SRCC_35	L3
DDR3_DQ [19]	IO_L17N_T2_35	J6
DDR3_DQ [20]	IO_L14N_T2_SRCC_35	K3
DDR3_DQ [21]	IO_L17P_T2_35	K6
DDR3_DQ [22]	IO_L13N_T2_MRCC_35	J4
DDR3_DQ [23]	IO_L18P_T2_35	L5
DDR3_DQ [24]	IO_L20N_T3_35	P1
DDR3_DQ [25]	IO_L19P_T3_35	N4
DDR3_DQ [26]	IO_L20P_T3_35	R1
DDR3_DQ [27]	IO_L22N_T3_35	N2
DDR3_DQ [28]	IO_L23P_T3_35	M6
DDR3_DQ [29]	IO_L24N_T3_35	N5
DDR3_DQ [30]	IO_L24P_T3_35	P6
DDR3_DQ [31]	IO_L22P_T3_35	P2
DDR3_DM0	IO_L4N_T0_35	D2
DDR3_DM1	IO_L8N_T1_AD14N_35	G2
DDR3_DM2	IO_L16N_T2_35	M2

DDR3_DM3	IO_L23N_T3_35	M5
DDR3_A[0]	IO_L11N_T1_SRCC_34	AA4
DDR3_A[1]	IO_L8N_T1_34	AB2
DDR3_A[2]	IO_L10P_T1_34	AA5
DDR3_A[3]	IO_L10N_T1_34	AB5
DDR3_A[4]	IO_L7N_T1_34	AB1
DDR3_A[5]	IO_L6P_T0_34	U3
DDR3_A[6]	IO_L5P_T0_34	W1
DDR3_A[7]	IO_L1P_T0_34	T1
DDR3_A[8]	IO_L2N_T0_34	V2
DDR3_A[9]	IO_L2P_T0_34	U2
DDR3_A[10]	IO_L5N_T0_34	Y1
DDR3_A[11]	IO_L4P_T0_34	W2
DDR3_A[12]	IO_L4N_T0_34	Y2
DDR3_A[13]	IO_L1N_T0_34	U1
DDR3_A[14]	IO_L6N_T0_VREF_34	V3
DDR3_BA[0]	IO_L9N_T1_DQS_34	AA3
DDR3_BA[1]	IO_L9P_T1_DQS_34	Y3
DDR3_BA[2]	IO_L11P_T1_SRCC_34	Y4
DDR3_S0	IO_L8P_T1_34	AB3
DDR3_RAS	IO_L12P_T1_MRCC_34	V4
DDR3_CAS	IO_L12N_T1_MRCC_34	W4
DDR3_WE	IO_L7P_T1_34	AA1
DDR3_ODT	IO_L14N_T2_SRCC_34	U5
DDR3_RESET	IO_L15P_T2_DQS_34	W6
DDR3_CLK_P	IO_L3P_T0_DQS_34	R3
DDR3_CLK_N	IO_L3N_T0_DQS_34	R2
DDR3_CKE	IO_L14P_T2_SRCC_34	T5

(五) QSPI Flash

The board is assembled with 128Mbit of QSPI flash memory using an 4-bit data

bus. The flash device is N25Q128 which uses 3.3V CMOS signaling standard. Because of its non-volatile property, it is usually used for storing software binaries, images, sounds or other media. Detail information of QSPI FLASH is shown in table 2-5-1 below.

Part	P/N	Capacity	Vender
U8	N25Q128	128M Bit	Numonyx

Table 2-5-1 QSPI Flash Information

Connections between FPGA and Flash are shown in Figure 2-5-1.

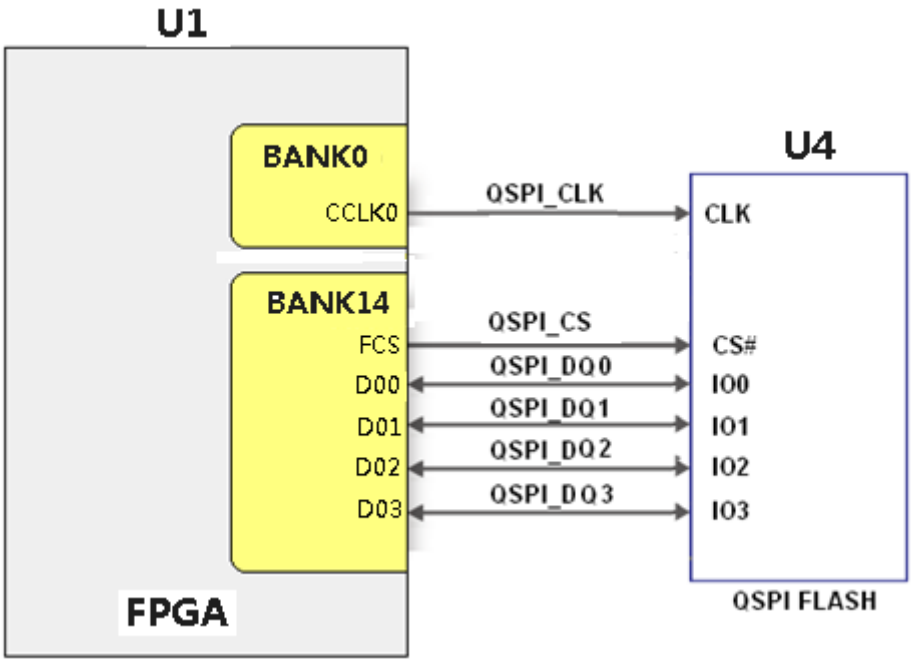


Figure 2-5-1 Connections between FPGA and Flash

Pin Assignment of FLASH：

Net Name	FPGA PIN Name	FPGA P/N
QSPI_CLK	CCLK_0	L12
QSPI_CS	IO_L6P_T0_FCS_B_14	T19
QSPI_DQ0	IO_L1P_T0_D00_MOSI_14	P22
QSPI_DQ1	IO_L1N_T0_D01_DIN_14	R22
QSPI_DQ2	IO_L2P_T0_D02_14	P21
QSPI_DQ3	IO_L2N_T0_D03_14	R21

Figure 2-5-2 shows onboard QSPI FLASH.

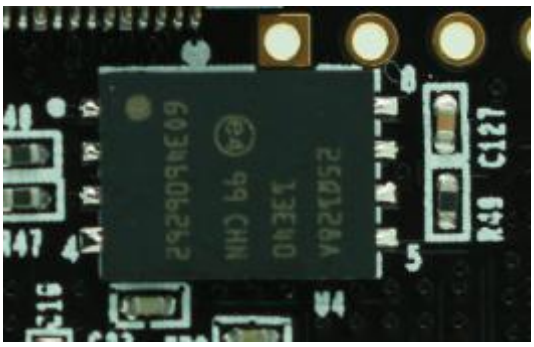


Figure 2-5-2 QSPI FLASH Onboard

(六) LEDs

There are three RED LEDs on the FPGA, it includes power indicator LED, done indicator LED and user LED. When the core board is power on, the power indicator LED turns on. when the FPGA configuration is configured, the done LED will be on. The user LED is driven directly by a pin of FPGA, driving its associated pin to a high logic level turns the LED on, and driving the pin low turns it off.

The schematic diagram of the hardware connection of the LED is shown in Figure 2-6-1:

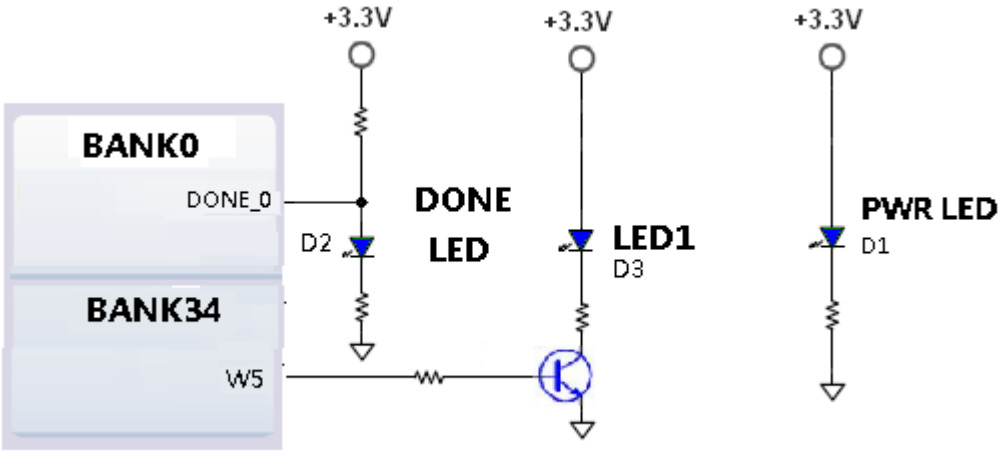


Figure 2-6-1 Connections between the LEDs and FPGA

Figure 2-6-2 is the LEDs on AC7100 board.

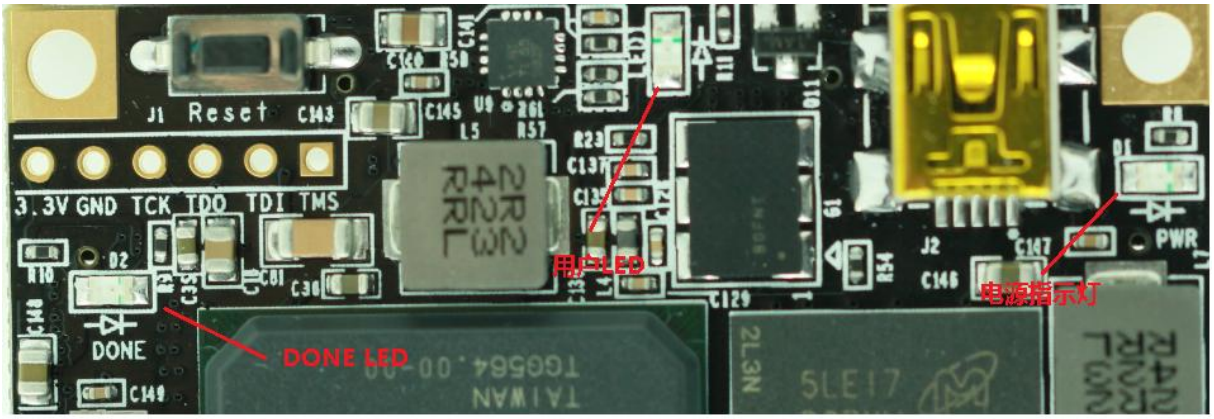


Figure 2-6-2 LEDs on AC7100 board

Pin Assignment of User LED

Net Name	FPGAPIN Name	FPGA P/N	Comment
LED1	IO_L15N_T2_DQS_34	W5	User LED

(七) RESET Button

AC7100 core board has a reset button, it is connected to the bank34 IO of FPGA. User can use this button to initialize the FPGA program. when reset button is pressed, the reset signal to FPGA is low and the reset is valid. When the button is not pressed, the reset signal is high.

The schematic diagram of the reset button connection is shown in Figure 2-7-1

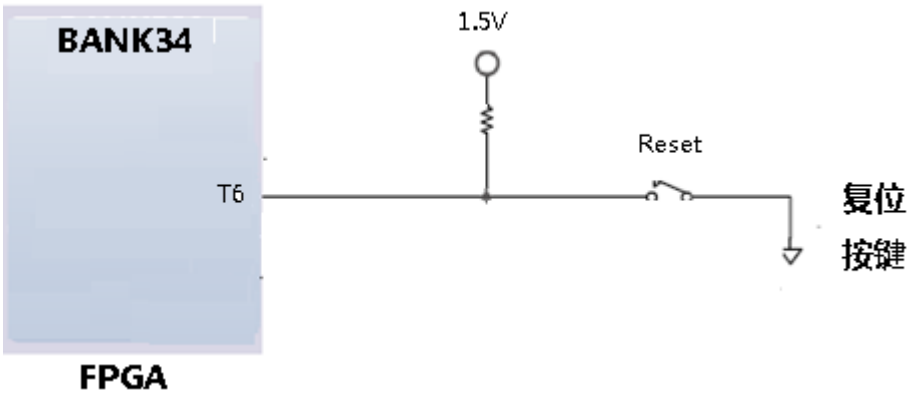


Figure 2-7-1 Connections between the button and FPGA

Figure 2-7-2 is the reset button on AC7100 board

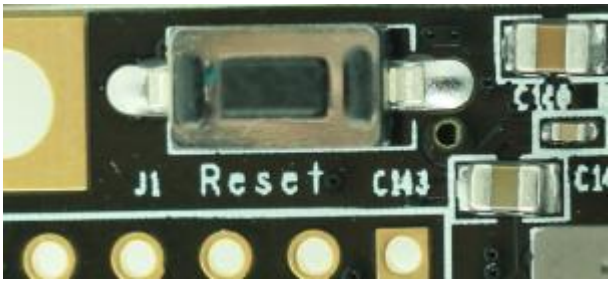


Figure 2-7-2 Reset Button on AC7100 Board

Pin Assignment of Reset Button

Net Name	FPGAPIN Name	FPGA P/N	Comment
RESET_N	IO_L17N_T2_34	T6	复位按键Reset

(八) JTAG Interface

In the AC7100 core board, it reserves a JTAG interface (J1), it is used to download or debug FPGA program without expansion board. Figure 2-8-1 is circuit part of the JTAG port, only four JTAG signals(TMS, TDI, TDO, TCK) are connected to J1 for JTAG access.

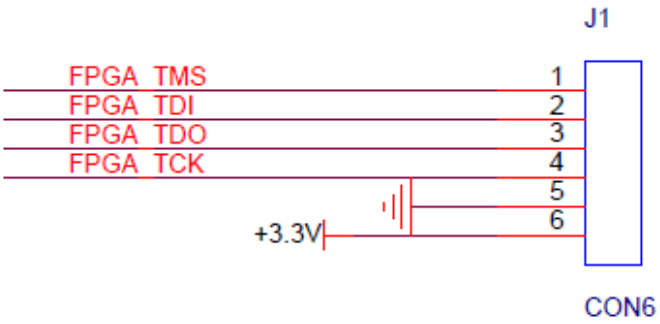


Figure 2-8-1 JTAG Interface

In AC7100 core board, the JTAG connector(J1) is not mounted, If user want to use it, please install the JTAG connector with single 6-pins 2.54mm pitch connector. Figure 2-8-2 shows the JTAG connector position on PCB board.

Figure 2-8-2 JTAG Interface On Board

(九) Power Input

In AC7100 core board, we reserved a mini USB port(J2) which can power on core board and work separately without expansion board. Using a USB cable connect to computer, the +5.0V power supply is coming from USB port to power on AC7100 board. Please do not connect other power supply which voltage is higher than +5.0V, it maybe damage the core board.

The schematic diagram of the mini USB connection is shown in Figure 2-9-1

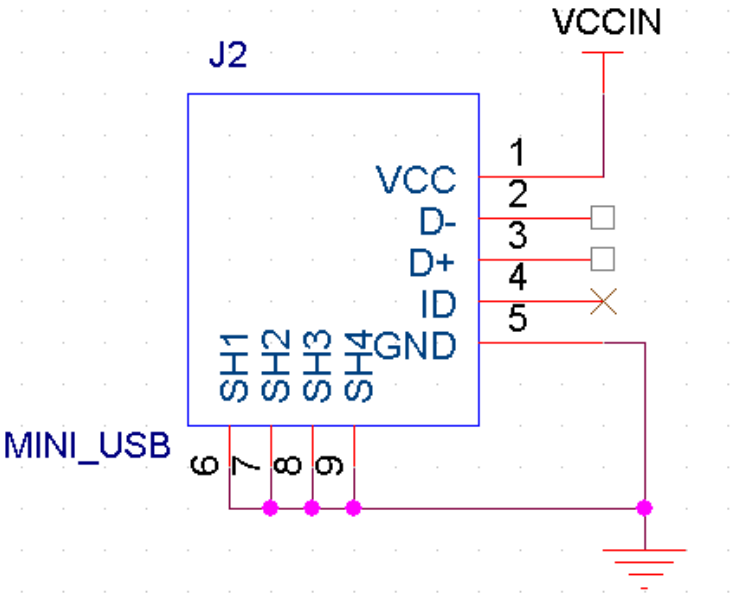


Figure 2-9-1MINI USB Port

Figure 2-9-2 is mini USB port on AC7100 board.

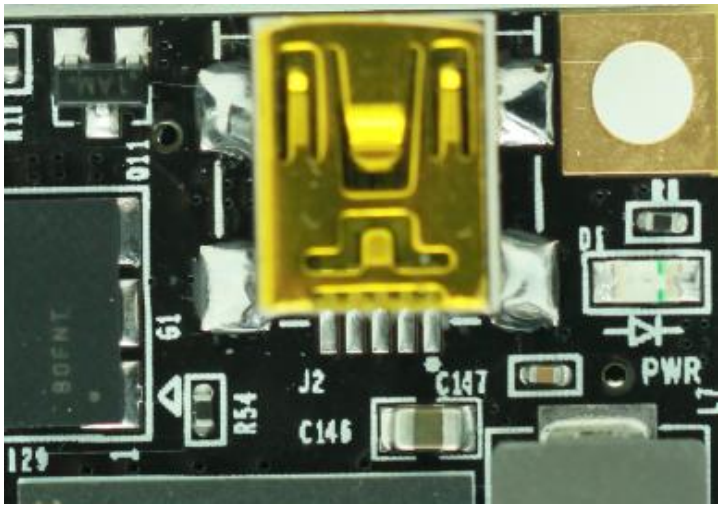


Figure 2-9-2 MINI USB port on AC7100 board

(十) Board-to-Board Connector

The core board has four high-speed board-to-board connectors on PCB bottom side. Each connector is 80-pins of 0.5mm pin pitch, which is suitable for high-speed signal transmission. 180 FPGA IOs (include 86 pairs LVDS signals) and all differential signals of GTP transceivers are connected to expansion board through these four connectors.

CON1 Connector

CON1 is one of 80-pins connector which is used to connect +5V power signals and FPGA IO signals between core board and expansion board. Please note that the voltage level of IO from FPGA bank34 is +1.5V standard. Table 2-10-1 list the pin assignment of CON1conector.

Table 2-10-1：Pin assignment of CN1

CON1 PIN	Net Name	FPGA PIN	Voltage Level	CON1 PIN	Net Name	FPGA PIN	Voltage Level
1	VCCIN	-	+5V	2	VCCIN	-	+5V
3	VCCIN	-	+5V	4	VCCIN	-	+5V
5	VCCIN	-	+5V	6	VCCIN	-	+5V
7	VCCIN	-	+5V	8	VCCIN	-	+5V
9	GND	-	Ground	10	GND	-	Ground

11	-	-	-	12	-	-	-
13	-	-	-	14	-	-	-
15	-	-	-	16	B13_L4_P	AA15	3.3V
17	-	-	-	18	B13_L4_N	AB15	3.3V
19	GND	-	Ground	20	GND	-	Ground
21	B13_L5_P	Y13	3.3V	22	B13_L1_P	Y16	3.3V
23	B13_L5_N	AA14	3.3V	24	B13_L1_N	AA16	3.3V
25	B13_L7_P	AB11	3.3V	26	B13_L2_P	AB16	3.3V
27	B13_L7_P	AB12	3.3V	28	B13_L2_N	AB17	3.3V
29	GND	-	Ground	30	GND	-	Ground
31	B13_L3_P	AA13	3.3V	32	B13_L6_P	W14	3.3V
33	B13_L3_N	AB13	3.3V	34	B13_L6_N	Y14	3.3V
35	B34_L23_P	Y8	1.5V	36	B34_L20_P	AB7	1.5V
37	B34_L23_N	Y7	1.5V	38	B34_L20_N	AB6	1.5V
39	GND	-	Ground	40	GND	-	Ground
41	B34_L18_N	AA6	1.5V	42	B34_L21_N	V8	1.5V
43	B34_L18_P	Y6	1.5V	44	B34_L21_P	V9	1.5V
45	B34_L19_P	V7	1.5V	46	B34_L22_P	AA8	1.5V
47	B34_L19_N	W7	1.5V	48	B34_L22_N	AB8	1.5V
49	GND	-	Ground	50	GND	-	Ground
51	XADC_VN	M9	ADC	52	NC		
53	XADC_VP	L10	ADC	54	B34_L25	U7	1.5V
55	-	-	-	56	B34_L24_P	W9	1.5V
57	-	-	-	58	B34_L24_N	Y9	1.5V
59	GND	-	Ground	60	GND	-	Ground
61	B16_L1_N	F14	3.3V	62	-	-	-
63	B16_L1_P	F13	3.3V	64	-	-	-
65	B16_L4_N	E14	3.3V	66	-	-	-
67	B16_L4_P	E13	3.3V	68	-	-	-
69	GND	-	Ground	70	GND	-	Ground
71	B16_L6_N	D15	3.3V	72	-	-	-

73	B16_L6_P	D14	3.3V	74	-	-	-
75	B16_L8_P	C13	3.3V	76	-	-	-
77	B16_L8_N	B13	3.3V	78	-	-	-
79	-	-	-	80	-	-	-

Figure 2-10-1 is the CON1 connector on core board, and the pin1 of connector is marked on the board.

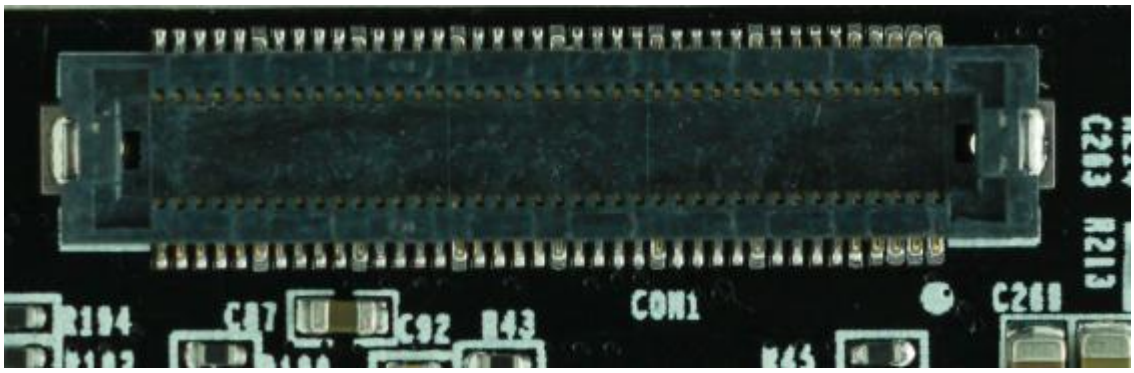


Figure 2-10-1 CON1 Connector Onboard

CON2 Connector

The 80-Pin connector CON2 is used to extend the IOs of FPGA bank13 and bank14, the voltage level of these IOs are +3.3V standard. The pin assignment of the CON2 connector is shown in table 2-10-2:

Table 2-10-2：Pin Assignment of CON2 Connector

CON2 PIN	Net Name	FPGA PIN	Voltage Level	CON2 PIN	Net Name	FPGA PIN	Voltage Level
1	B13_L16_P	W15	3.3V	2	B14_L16_P	V17	3.3V
3	B13_L16_N	W16	3.3V	4	B14_L16_N	W17	3.3V
5	B13_L15_P	T14	3.3V	6	B13_L14_P	U15	3.3V
7	B13_L15_N	T15	3.3V	8	B13_L14_N	V15	3.3V
9	GND	-	Ground	10	GND	-	Ground
11	B13_L13_P	V13	3.3V	12	B14_L10_P	AB21	3.3V
13	B13_L13_N	V14	3.3V	14	B14_L10_N	AB22	3.3V
15	B13_L12_P	W11	3.3V	16	B14_L8_N	AA21	3.3V
17	B13_L12_N	W12	3.3V	18	B14_L8_P	AA20	3.3V

19	GND	-	Ground	20	GND	-	Ground
21	B13_L11_P	Y11	3.3V	22	B14_L15_N	AB20	3.3V
23	B13_L11_N	Y12	3.3V	24	B14_L15_P	AA19	3.3V
25	B13_L10_P	V10	3.3V	26	B14_L17_P	AA18	3.3V
27	B13_L10_N	W10	3.3V	28	B14_L17_N	AB18	3.3V
29	GND	-	Ground	30	GND	-	Ground
31	B13_L9_N	AA11	3.3V	32	B14_L6_N	T20	3.3V
33	B13_L9_P	AA10	3.3V	34	B13_IO0	Y17	3.3V
35	B13_L8_N	AB10	3.3V	36	B14_L7_N	W22	3.3V
37	B13_L8_P	AA9	3.3V	38	B14_L7_P	W21	3.3V
39	GND	-	Ground	40	GND	-	Ground
41	B14_L11_N	V20	3.3V	42	B14_L4_P	T21	3.3V
43	B14_L11_P	U20	3.3V	44	B14_L4_N	U21	3.3V
45	B14_L14_N	V19	3.3V	46	B14_L9_P	Y21	3.3V
47	B14_L14_P	V18	3.3V	48	B14_L9_N	Y22	3.3V
49	GND	-	Ground	50	GND	-	Ground
51	B14_L5_N	R19	3.3V	52	B14_L12_N	W20	3.3V
53	B14_L5_P	P19	3.3V	54	B14_L12_P	W19	3.3V
55	B14_L18_N	U18	3.3V	56	B14_L13_N	Y19	3.3V
57	B14_L18_P	U17	3.3V	58	B14_L13_P	Y18	3.3V
59	GND	-	Ground	60	GND	-	Ground
61	B13_L17_P	T16	3.3V	62	B14_L3_N	V22	3.3V
63	B13_L17_N	U16	3.3V	64	B14_L3_P	U22	3.3V
65	B14_L21_N	P17	3.3V	66	B14_L20_N	T18	3.3V
67	B14_L21_P	N17	3.3V	68	B14_L20_P	R18	3.3V
69	GND	-	Ground	70	GND	-	Ground
71	B14_L22_P	P15	3.3V	72	B14_L19_N	R14	3.3V
73	B14_L22_N	R16	3.3V	74	B14_L19_P	P14	3.3V
75	B14_L24_N	R17	3.3V	76	B14_L23_P	N13	3.3V
77	B14_L24_P	P16	3.3V	78	B14_L23_N	N14	3.3V
79	B14_IO0	P20	3.3V	80	B14_IO25	N15	3.3V

Figure 2-10-2 is the CON2 connector on core board, and the pin1 of connector is marked on the board.

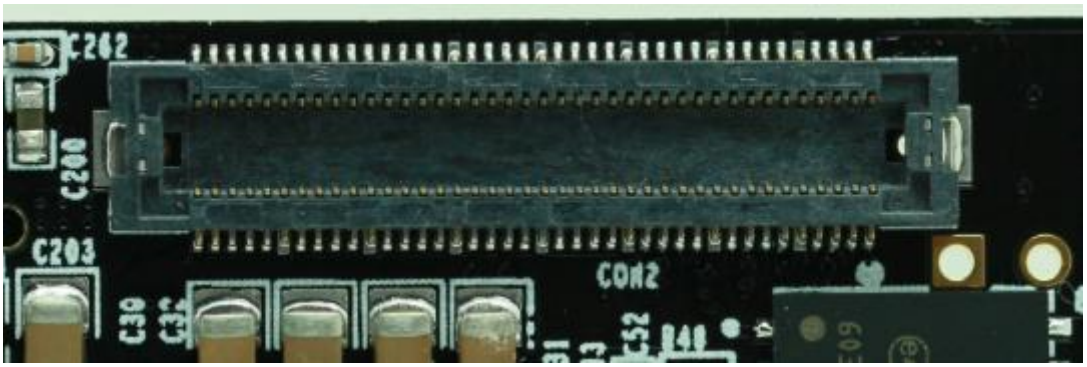


Figure 2-10-2 CON2 Connector Onboard

CON3 Connector

The 80-Pin connector CON3 is used to extend the IOs of FPGA bank15 and bank16, the voltage level of these IOs are +3.3V standard by default, but it can be changed to other voltage level if we change the VCCO power supply of bank15 and bank16 by replacing the LDO chipset.

Four JTAG signals also connected to CON3 connector for expansion board to access the JTAG interface. The pin assignment of the CON3 connector is shown in table 2-10-3.

Table 2-10-3：Pin Assignment of CON3 Connector

CON3 PIN	Net Name	FPGA PIN	Voltage Level	CON3 PIN	Net Name	FPGA PIN	Voltage Level
1	B15_IO0	J16	3.3V	2	B15_IO25	M17	3.3V
3	B16_IO0	F15	3.3V	4	B16_IO25	F21	3.3V
5	B15_L4_P	G17	3.3V	6	B16_L21_N	A21	3.3V
7	B15_L4_N	G18	3.3V	8	B16_L21_P	B21	3.3V
9	GND	-	Ground	10	GND	-	Ground
11	B15_L2_P	G15	3.3V	12	B16_L23_P	E21	3.3V
13	B15_L2_N	G16	3.3V	14	B16_L23_N	D21	3.3V
15	B15_L12_P	J19	3.3V	16	B16_L22_P	E22	3.3V

17	B15_L12_N	H19	3.3V	18	B16_L22_N	D22	3.3V
19	GND	-	Ground	20	GND	-	Ground
21	B15_L11_P	J20	3.3V	22	B16_L24_P	G21	3.3V
23	B15_L11_N	J21	3.3V	24	B16_L24_N	G22	3.3V
25	B15_L1_N	G13	3.3V	26	B15_L8_N	G20	3.3V
27	B15_L1_P	H13	3.3V	28	B15_L8_P	H20	3.3V
29	GND	-	Ground	30	GND	-	Ground
31	B15_L5_P	J15	3.3V	32	B15_L7_N	H22	3.3V
33	B15_L5_N	H15	3.3V	34	B15_L7_P	J22	3.3V
35	B15_L3_N	H14	3.3V	36	B15_L9_P	K21	3.3V
37	B15_L3_P	J14	3.3V	38	B15_L9_N	K22	3.3V
39	GND	-	Ground	40	GND	-	Ground
41	B15_L19_P	K13	3.3V	42	B15_L15_N	M22	3.3V
43	B15_L19_N	K14	3.3V	44	B15_L15_P	N22	3.3V
45	B15_L20_P	M13	3.3V	46	B15_L6_N	H18	3.3V
47	B15_L20_N	L13	3.3V	48	B15_L6_P	H17	3.3V
49	GND	-	Ground	50	GND	-	Ground
51	B15_L14_P	L19	3.3V	52	B15_L13_N	K19	3.3V
53	B15_L14_N	L20	3.3V	54	B15_L13_P	K18	3.3V
55	B15_L21_P	K17	3.3V	56	B15_L10_P	M21	3.3V
57	B15_L21_N	J17	3.3V	58	B15_L10_N	L21	3.3V
59	GND	-	Ground	60	GND	-	Ground
61	B15_L23_P	L16	3.3V	62	B15_L18_P	N20	3.3V
63	B15_L23_N	K16	3.3V	64	B15_L18_N	M20	3.3V
65	B15_L22_P	L14	3.3V	66	B15_L17_N	N19	3.3V
67	B15_L22_N	L15	3.3V	68	B15_L17_P	N18	3.3V
69	GND	-	Ground	70	GND	-	Ground
71	B15_L24_P	M15	3.3V	72	B15_L16_P	M18	3.3V
73	B15_L24_N	M16	3.3V	74	B15_L16_N	L18	3.3V
75	NC	-		76	NC	-	
77	FPGA_TCK	V12	3.3V	78	FPGA_TDI	R13	3.3V

79	FPGA_TDO	U13	3.3V	80	FPGA_TMS	T13	3.3V

Figure 2-10-3 is the CON3 connector on core board, and the pin1 of connector is marked on the board.

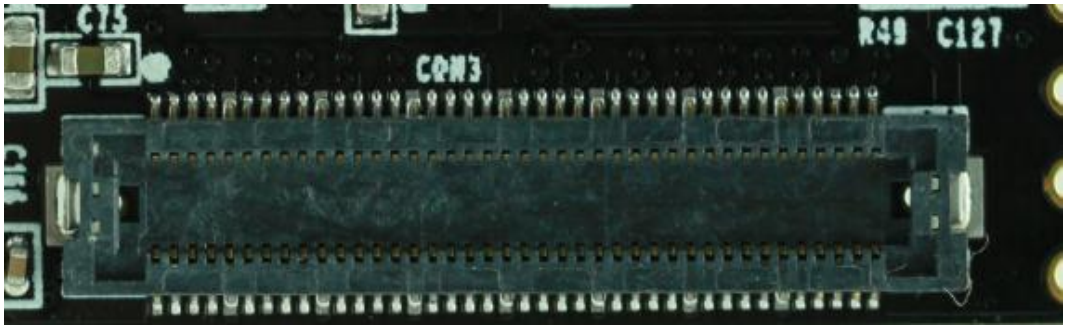


Figure 2-10-3 CON3 Connector Onboard

CON4 Connector

The 80-Pin connector CON4 is used to extend the IOs of FPGA bank16 and signals of GTP transceivers. The pin assignment of the CON4 connector is shown in table 2-10-4.

Table 2-10-4：Pin Assignment of CON4

CON4 PIN	Net Name	FPGA PIN	Voltage Level	CON4 PIN	Net Name	FPGA PIN	Voltage Level
1	NC	-	-	2		-	-
3	NC	-	-	4		-	-
5	NC	-	-	6		-	-
7	NC	-	-	8		-	-
9	GND	-	Ground	10	GND	-	Ground
11	NC	-	-	12	MGT_TX2_P	B6	Diff
13	NC	-	-	14	MGT_TX2_N	A6	Diff
15	GND	-	Ground	16	GND	-	Ground
17	MGT_TX3_P	D7	Diff	18	MGT_RX2_P	B10	Diff
19	MGT_TX3_N	C7	Diff	20	MGT_RX2_N	A10	Diff
21	GND	-	Ground	22	GND	-	Ground

23	MGT_RX3_P	D9	Diff	24	MGT_TX0_P	B4	Diff
25	MGT_RX3_N	C9	Diff	26	MGT_TX0_N	A4	Diff
27	GND	-	Ground	28	GND	-	Ground
29	MGT_TX1_P	D5	Diff	30	MGT_RX0_P	B8	Diff
31	MGT_TX1_N	C5	Diff	32	MGT_RX0_N	A8	Diff
33	GND	-	Ground	34	GND	-	Ground
35	MGT_RX1_P	D11	Diff	36	MGT_CLK1_P	F10	Diff
37	MGT_RX1_N	C11	Diff	38	MGT_CLK1_N	E10	Diff
39	GND	-	Ground	40	GND	-	Ground
41	B16_L5_P	E16	3.3V	42	B16_L2_P	F16	3.3V
43	B16_L5_N	D16	3.3V	44	B16_L2_N	E17	3.3V
45	B16_L7_P	B15	3.3V	46	B16_L3_P	C14	3.3V
47	B16_L7_N	B16	3.3V	48	B16_L3_N	C15	3.3V
49	GND	-	Ground	50	GND	-	Ground
51	B16_L9_P	A15	3.3V	52	B16_L10_P	A13	3.3V
53	B16_L9_N	A16	3.3V	54	B16_L10_N	A14	3.3V
55	B16_L11_P	B17	3.3V	56	B16_L12_P	D17	3.3V
57	B16_L11_N	B18	3.3V	58	B16_L12_N	C17	3.3V
59	GND	-	Ground	60	GND	-	Ground
61	B16_L13_P	C18	3.3V	62	B16_L14_P	E19	3.3V
63	B16_L13_N	C19	3.3V	64	B16_L14_N	D19	3.3V
65	B16_L15_P	F18	3.3V	66	B16_L16_P	B20	3.3V
67	B16_L15_N	E18	3.3V	68	B16_L16_N	A20	3.3V
69	GND	-	Ground	70	GND	-	Ground
71	B16_L17_P	A18	3.3V	72	B16_L18_P	F19	3.3V
73	B16_L17_N	A19	3.3V	74	B16_L18_N	F20	3.3V
75	B16_L19_P	D20	3.3V	76	B16_L20_P	C22	3.3V
77	B16_L19_N	C20	3.3V	78	B16_L20_N	B22	3.3V
79	NC	-		80	NC	-	

Figure 2-10-4 is the CON4 connector on core board, and the pin1 of connector is marked on the board.

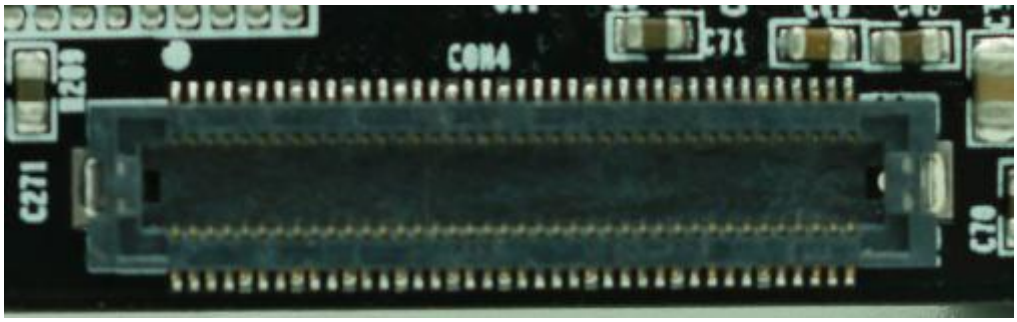


Figure 2-10-4 CON4 Connector Onboard

(十一) POWER

The power supply voltage of the AC7100 core board is DC5V and can supply from mini USB port or board-to-board connector from expansion board. Please note that the mini USB and expansion board cannot supply power to core board at the same time, it maybe damage the USB port of computer. The schematic diagram of the power supply on the board is shown in figure 2-11-1 below.

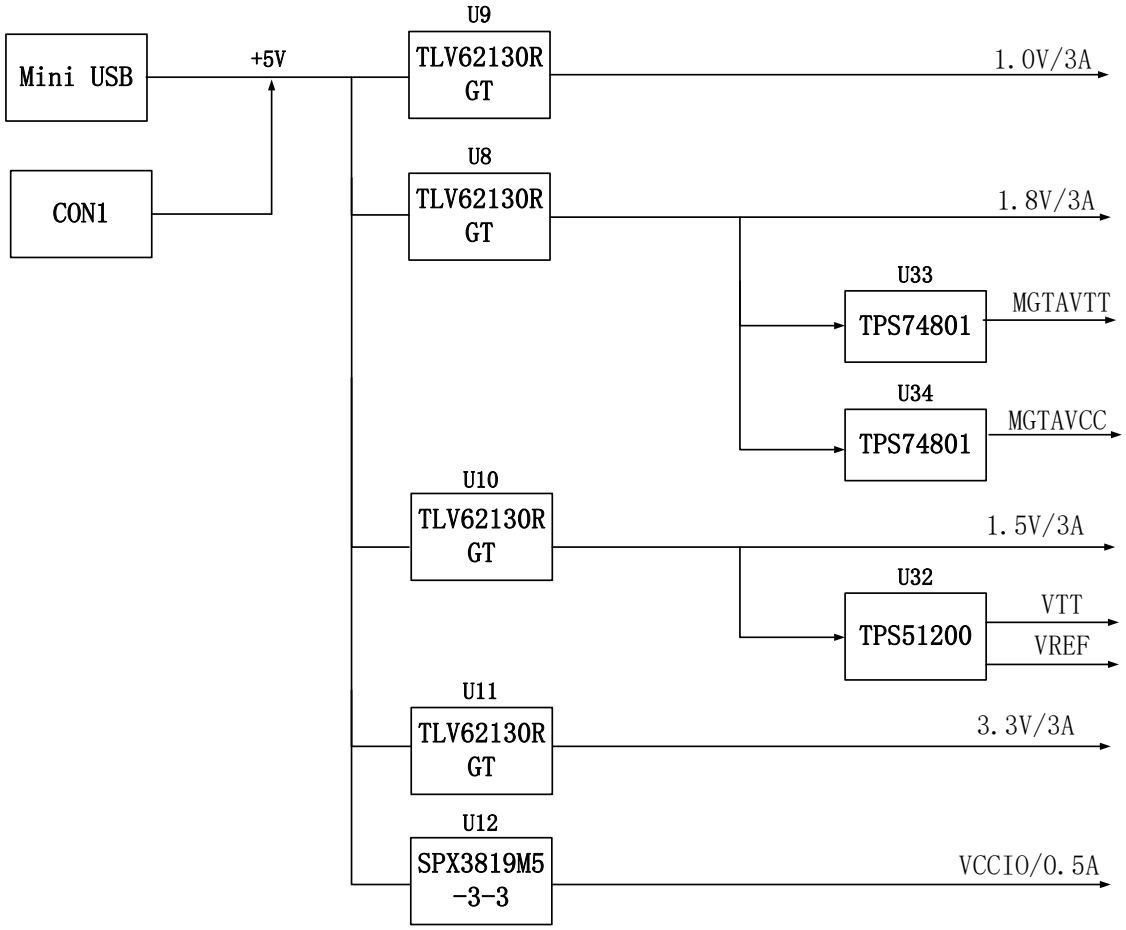


Figure 2-11-1Power Design

AC7100 core board uses the +5V power to generate +3.3V, +1.5V, +1.8V and +1.0V power output through the DC/DC power convertor. The output current of each power can be as high as 3A. AC7100 core board uses a LDO chipset of SPX3819M5-3-3 to generate +3.3V power supply for VCCIO power of FPGA bank15 and bank16. it is easy for use to change the voltage standard of IOs by replacing of the LDO chipset.

The +1.5V power generates the required VTT and VREF voltages for DDR3 through the TI TPS51200 chipset. And+1.8V power generates the MGTAVTT and MGTAVCC power of GTP transceiver through the TI LDO chipset(TPS74801).

The functions of each power distribution are shown below

Power	Distribution
+3.3V	FPGA Bank0,Bank13 , Bank14 VCCIO, QSIP FLASH, Oscillators
+1.8V	FPGA auxiliary Power, TPS74801
+1.0V	FPGA Core Power
+1.5V	DDR3, FPGA Bank34 and Bank35
VREF, VTT (+0.75V)	DDR3
VCCIO(+3.3V)	FPGA Bank15, Bank16
MGTAVTT(+1.2V)	FPGA Bank216, GTP Transceivers
MGTAVCC(+1.0V)	FPGA Bank216, GTP Transceivers

There is requirement of power supply sequencing of Artix-7 FPGA, AC7100 core board is designed to meet it, the order of power on for each power supply is as following:

+1.0V -> +1.8V -> +1.5 V, +3.3V, VCCIO

For GPT power supply sequencing of Artix-7 FPGA, the order of power on for each power supply is as following:

+1.0V -> MGTAVCC -> MGTAVTT

Power circuit on AC7100 core board is showed in Figure 2-11-2 below.

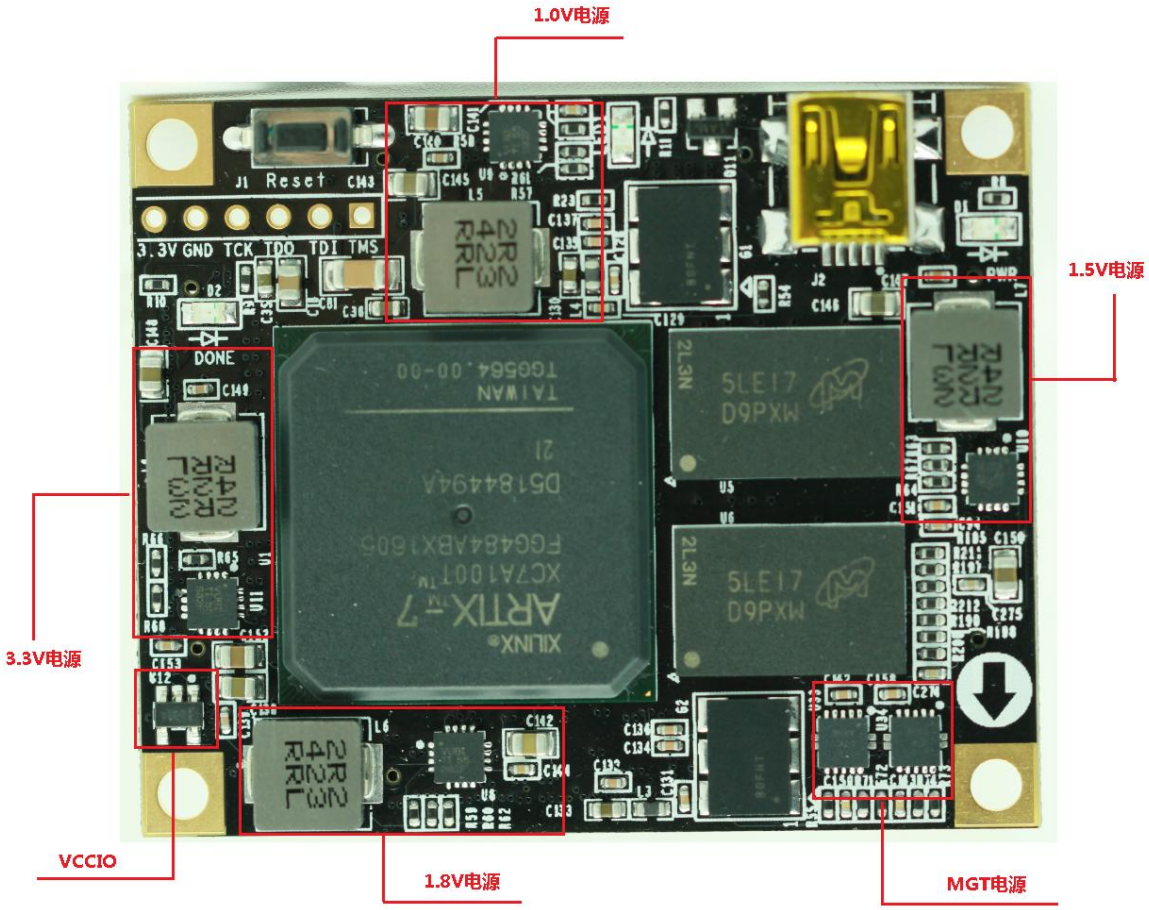
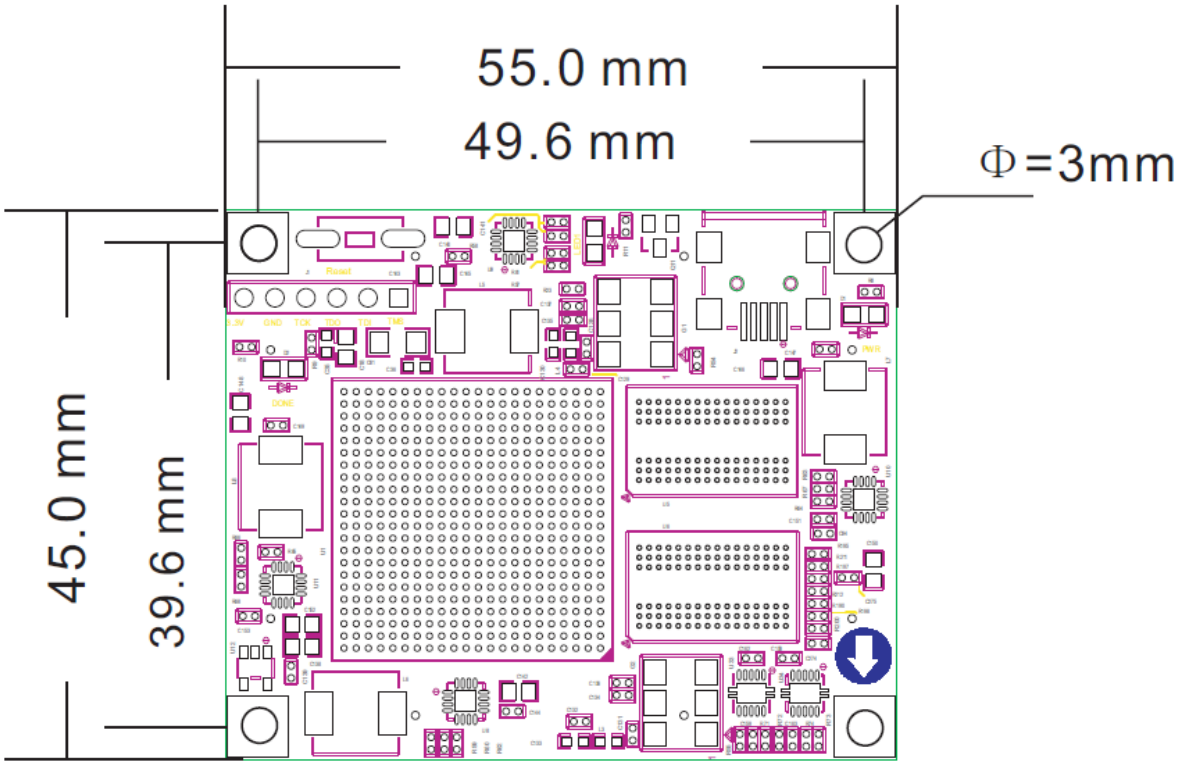
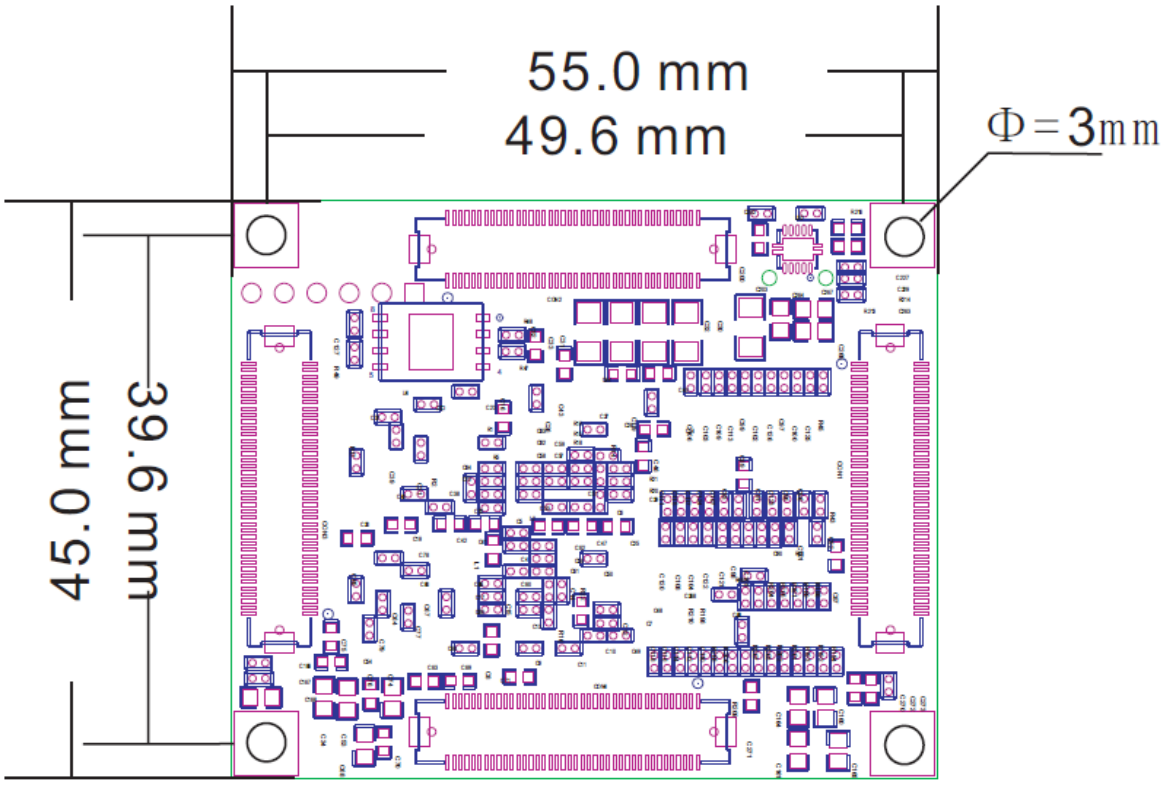


Figure 2-11-2 Power of AC7100

(十二) Mechanical

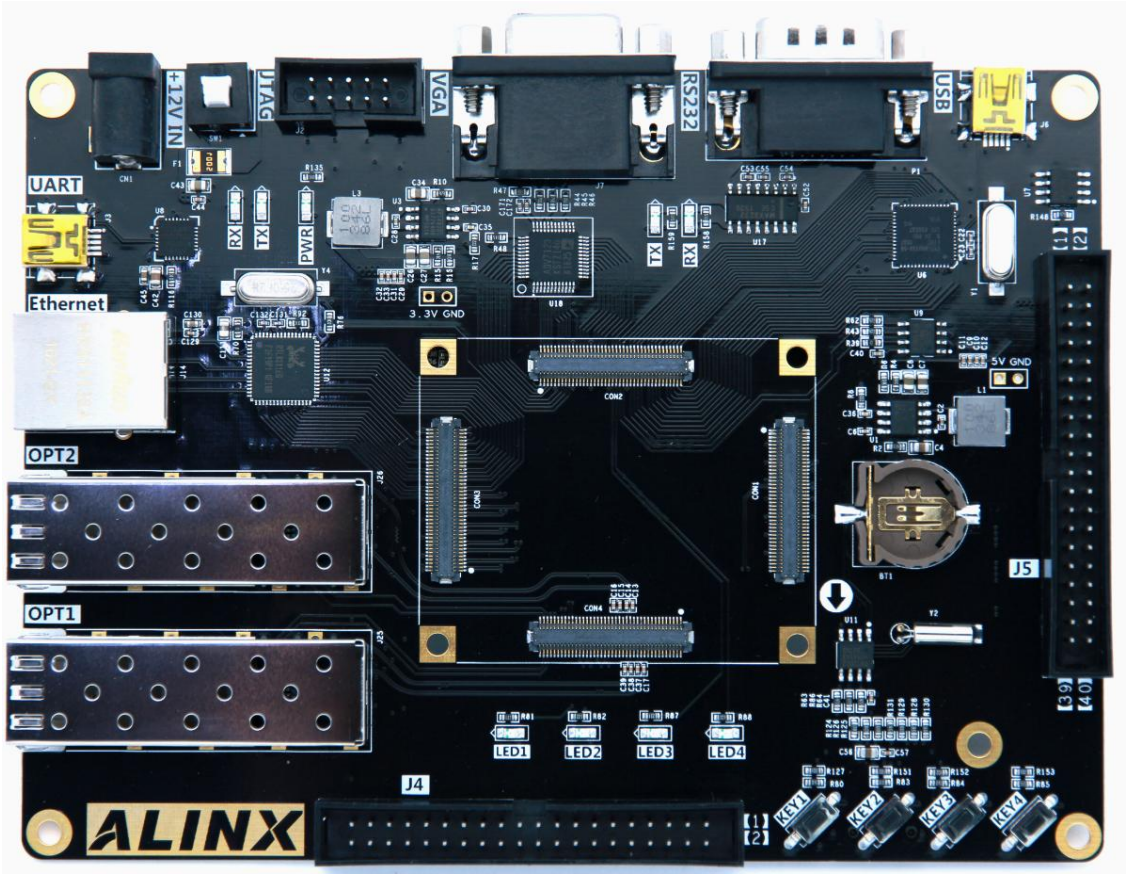


Top View



Bottom View

三、 Expansion Board



(一) Overview

The following features are provided on the AX7102 expansion board:

- One 10/100M/1000M Ethernet with RJ45 port;
- Two Port of SFP port;;
- One USB2.0 Port;
- One USB-to-serial port;
- One RS232 Serial Port;
- Real Time Clock;
- EEPROM with IIC interface;
- Micro SD Socket;
- Two 40-pin IO Headers
- 10-pin JTAG connector;
- 24-bit VGA port ;
- Four user LEDs

- Four user Buttons;

(二) Gigabit Ethernet

AX7102 board supports Gigabit Ethernet transfer by an external Realtek RTL8211EG PHY chip. The RTL8211EG chip with integrated 10/100/1000 Mbps Gigabit Ethernet transceiver also supports GMII MAC interface.

RTL8211EG will detect some specific IO level when power is on, so as to determine the operation mode. The following table describes the default setting in AX7102 board after the GPHY chip is powered on.

Configuration Pin	Description	Value
PHYAD[2:0]	PHY Address	PHY Address 为 001
SELRGV	Voltage Standard of GMII Interface	+3.3V
AN[1:0]	Auto-Negotiation Configuration	10/100/1000M Auto-Negotiation
RX Delay	RGMII Transmit Clock Timing Control	Add 2ns delay to RXC for RXD latching
TX Delay	RGMII Transmit Clock Timing Control	Add 2ns delay to TXC for TXD latching
MODE	RGMII Or GMII Interface	GMII

More information about the RTL8211EG PHY chip please refer to its datasheet, as well as the application notes, which are available on the manufacturer’ s website.

Figure 3-2-1 shows the connections between the FPGA, Gigabit Ethernet PHY, and RJ45 connector.

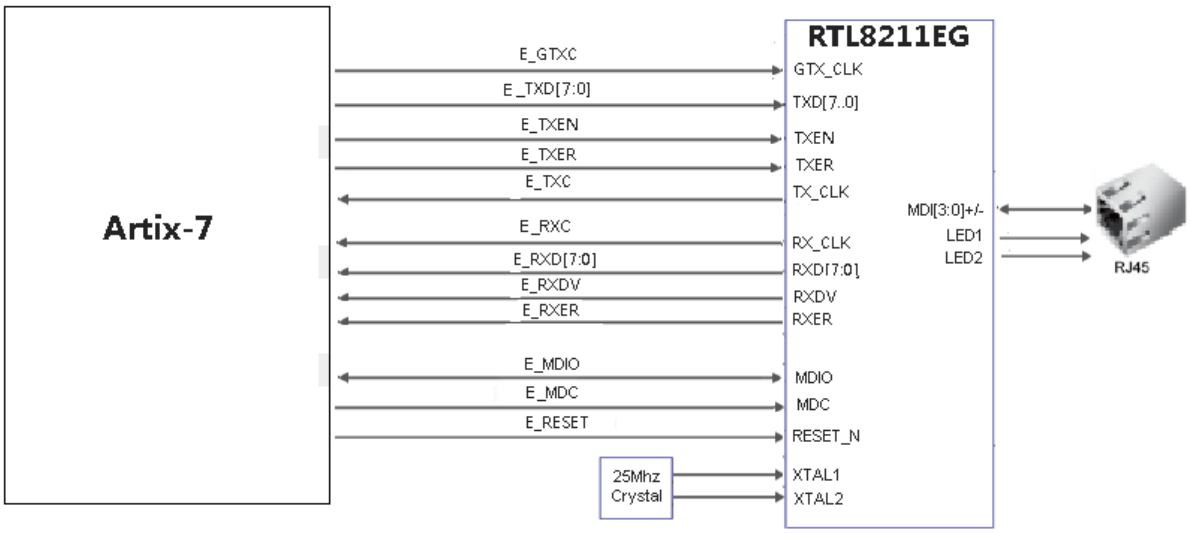


Figure 3-2-1 Connections between FPGA and Gigabit Ethernet

Figure 3-2-2 shows Gigabit Ethernet and RJ45 Connector on board.

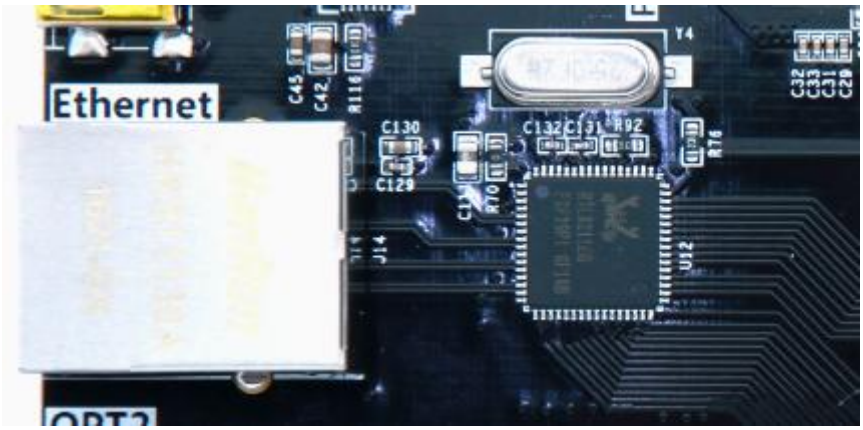


Figure 3-2-2 Gigabit Ethernet and RJ45

The pin assignment associated to Gigabit Ethernet interface is listed in Table 3-2-1.

Table 3-2-1 PIN Assignment of Gigabit Ethernet

Net Name	FPGA PIN	Comments
E_GTXC	L18	GMII Transmit Clock
E_TXD0	M15	GMII Transmit Data 0
E_TXD1	L14	GMII Transmit Data1
E_TXD2	K16	GMII Transmit Data2
E_TXD3	L16	GMII Transmit Data3
E_TXD4	K17	GMII Transmit Data4

E_TXD5	L20	GMII Transmit Data5
E_TXD6	L19	GMII Transmit Data6
E_TXD7	L13	GMII Transmit Data7
E_TXEN	M16	GMII Transmit Enable
E_TXER	M13	GMII Transmit Error
E_TXC	J17	MII Transmit Clock
E_RXC	K18	GMII Receive Clock
E_RXDV	M22	GMII Data Receive Valid
E_RXER	N19	GMII Data Receive Error
E_RXD0	N22	GMII Receive Data0
E_RXD1	H18	GMII Receive Data1
E_RXD2	H17	GMII Receive Data2
E_RXD3	K19	GMII Receive Data3
E_RXD4	M21	GMII Receive Data4
E_RXD5	L21	GMII Receive Data5
E_RXD6	N20	GMII Receive Data6
E_RXD7	M20	GMII Receive Data7
E_COL	N18	Collision In Half Duplex Mode
E_CRS	M18	Carrier Sense
E_RESET	L15	Hardware Reset
E_MDC	W10	Management Data Clock
E_MDIO	V10	Management Data

(三) SFP Interface

AX7102 expansion board has 2 channels of SFP interface, after plugging in optical module(1G or 10G) to SFP connector, optical fiber communication can done between AX7102 board and other optical fiber devices. The link speed of data traffic is up to 6.6Gb/s, and it is independent of data transfer and data receiver. The tx and rx signals of SFP interface is connected to GTP transceiver of FPGA with AC couple mode, the GTP transceiver reference clock is provided by the 148.5Mhz differential crystal oscillator which mounted on the core board. The schematic diagram of FPGA and optical fiber design is shown in figure

3-3-1.

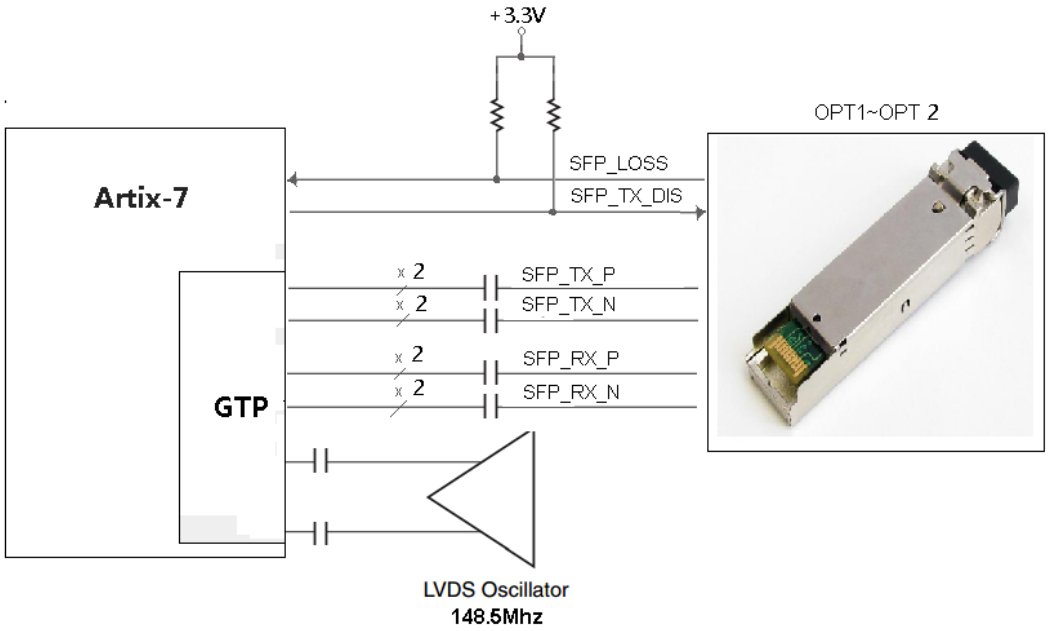


Figure 3-3-1 Hardware Design of SPF Interface

Figure 3-3-2 shows two SFP interfaces in the expansion board.

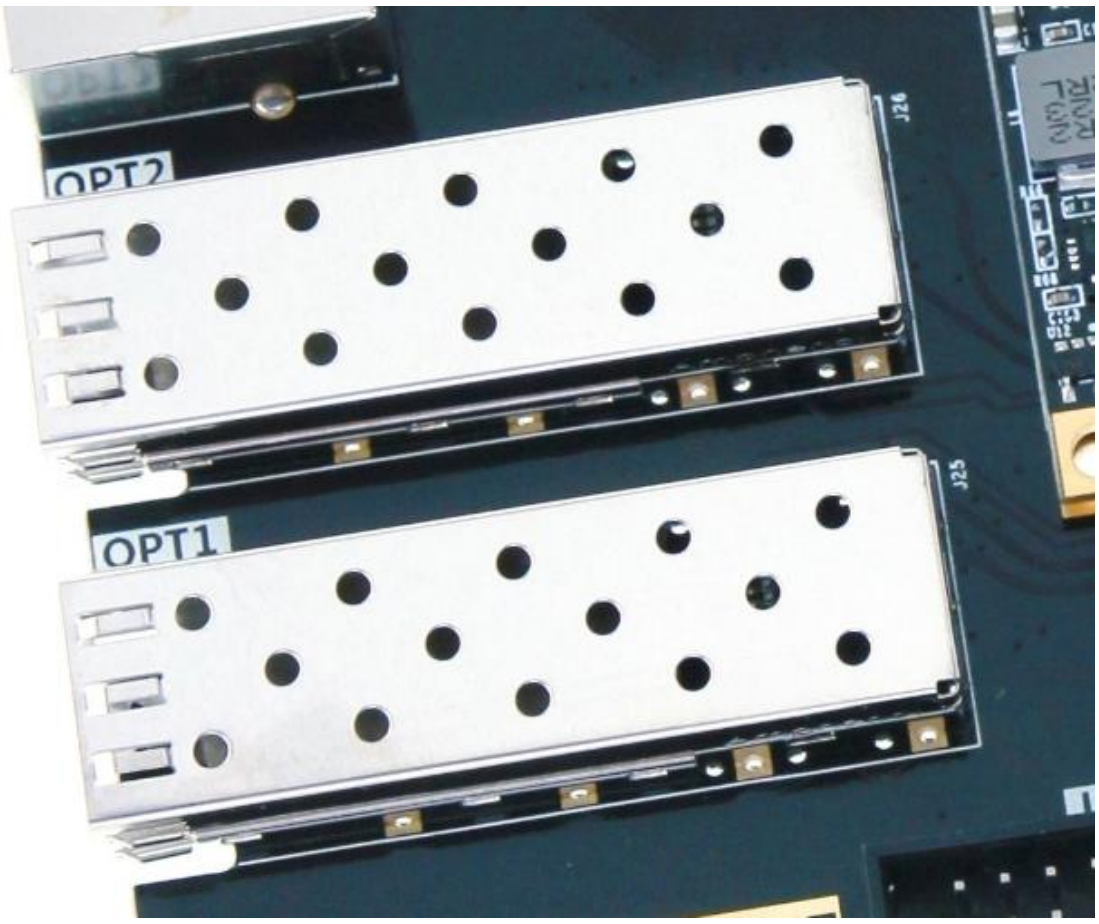


Figure 3-3-2 Two SFP Interfaces Onboard

PIN Assignment Of SFP1.

Net Name	FPGA PIN	Comments
SFP1_TX_P	B4	SFP1 Data Transfer (Positive)
SFP1_TX_N	A4	SFP1 Data Transfer (Negative)
SFP1_RX_P	B8	SFP1 Data Receiver (Positive)
SFP1_RX_P	A8	SFP1 Data Receiver (Negative)
SFP1_TX_DIS	C22	SFP1 Optical Transfer Disable
SFP1_LOSS	B22	SFP1 Optical LOSS

PIN Assignment Of SFP2.

Net Name	FPGA PIN	Commnets
SFP2_TX_P	D5	SFP2 Data Transfer (Positive)
SFP2_TX_N	C5	SFP2 Data Transfer (Negative)
SFP2_RX_P	D11	SFP2 Data Receiver (Positive)
SFP2_RX_P	C11	SFP2 Data Receiver (Negative)
SFP2_TX_DIS	C20	SFP1 Optical Transfer Disable
SFP2_LOSS	D20	SFP1 Optical LOSS

(四) VGA Port

The AX7102 board includes a 15-pin D-SUB connector for VGA output. The VGA synchronization signals are provided directly from the Artix-7 FPGA, and the Analog Devices ADV7123 triple 10-bit high-speed video DAC (only the higher 8-bits are used) is used to produce the analog data signals (red, green, and blue). It could support the SXGA standard (1280*1024) with a bandwidth of 100MHz. Figure 3-4-1 gives the associated schematic.

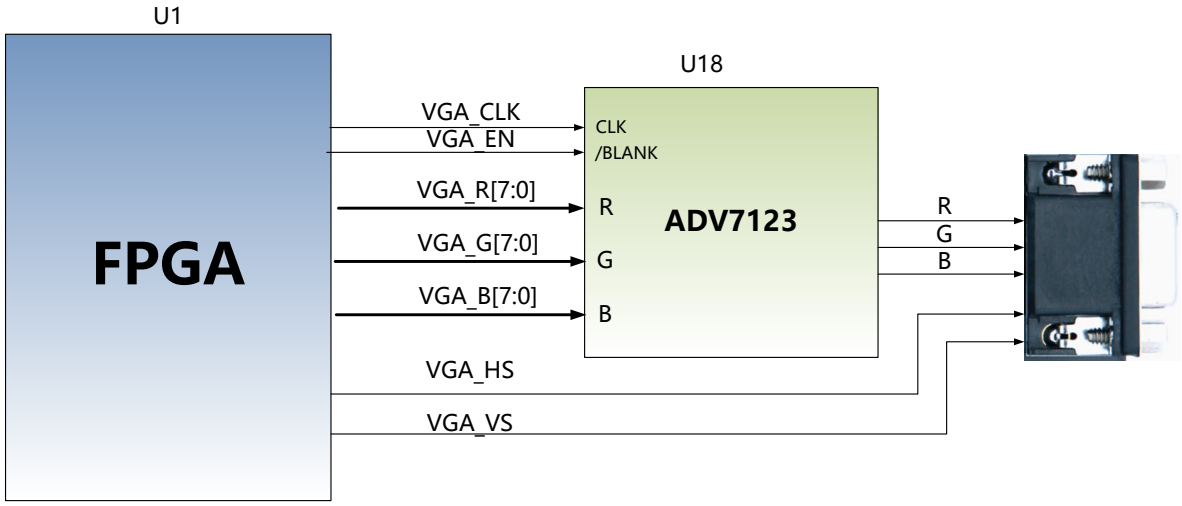


Figure 3-4-1 Connections Between FPGA and VGA

Figure 3-4-2 shows the VGA circuit in AX7102 board.

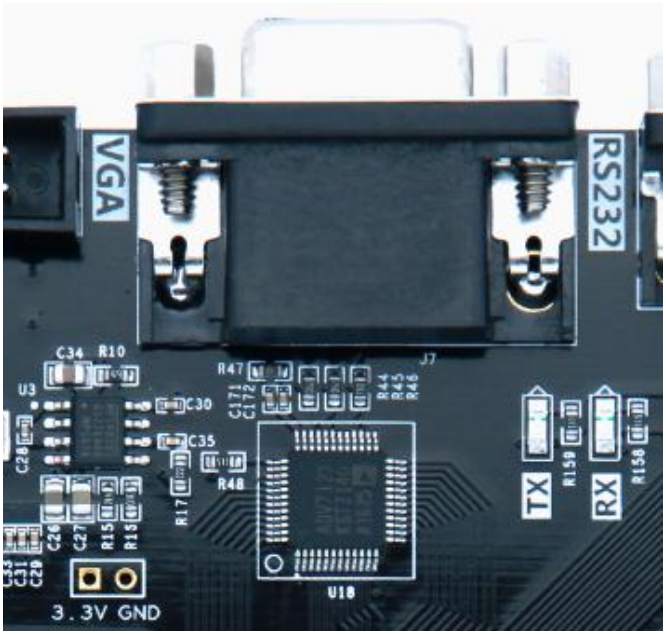


Figure 3-4-2 VGA Circuit Onboard

Pin Assignment of VGA Interface.

Net Name	FPGA PIN
VGA_CLK	U21
VGA_EN	AB20
VGA_HS	AA11
VGA_VS	AA10
VGA_R7	W15

VGA_R6	W16
VGA_R5	T14
VGA_R4	T15
VGA_R3	V13
VGA_R2	V14
VGA_R1	W11
VGA_R0	W12
VGA_G7	AA20
VGA_G6	AA21
VGA_G5	AB22
VGA_G4	AB21
VGA_G3	V15
VGA_G2	U15
VGA_G1	W17
VGA_G0	V17
VGA_B7	T21
VGA_B6	W21
VGA_B5	W22
VGA_B4	Y17
VGA_B3	T20
VGA_B2	AB18
VGA_B1	AA18
VGA_B0	AA19

(五) USB2.0

The AX7102 board provides both USB2.0 interfaces using the Cypress CY7C68013A single-chip USB controller. The device controllers are compliant with the Universal Serial Bus Specification Rev. 2.0, supporting data transfer at full-speed (12 Mbit/s) and low-speed (1.5Mbit/s).

Detailed information for using the CY7C68013A device is available in its

datasheet and programming guide, both documents can be found on the manufacturer’ s website, or in the CD\Datasheets\USB folder on the AX7102 System CD. The USB software driver need to install in PC before the USB2.0 design and test.

a 24MHz crystal is provided clock to CY7C68013A for normal operation, and the schematic diagram of the FPGA and CY7C68013A connections is shown in figure 3-5-1 below.

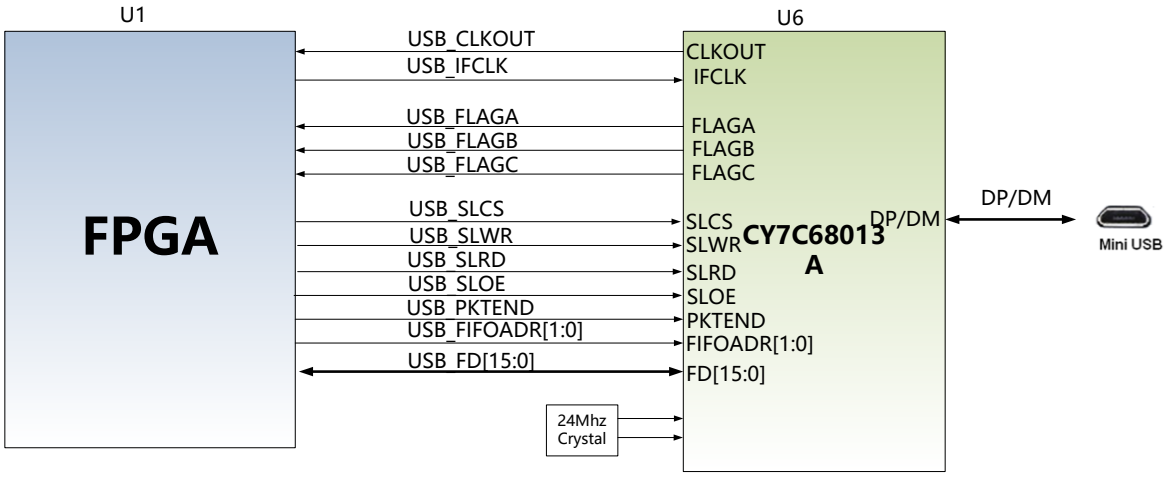


Figure 3-5-1 Connections Between FPGA and USB

Figure 3-5-2 is the USB2.0 on board, U6 is the CY7C68013A and J6 is USB port.

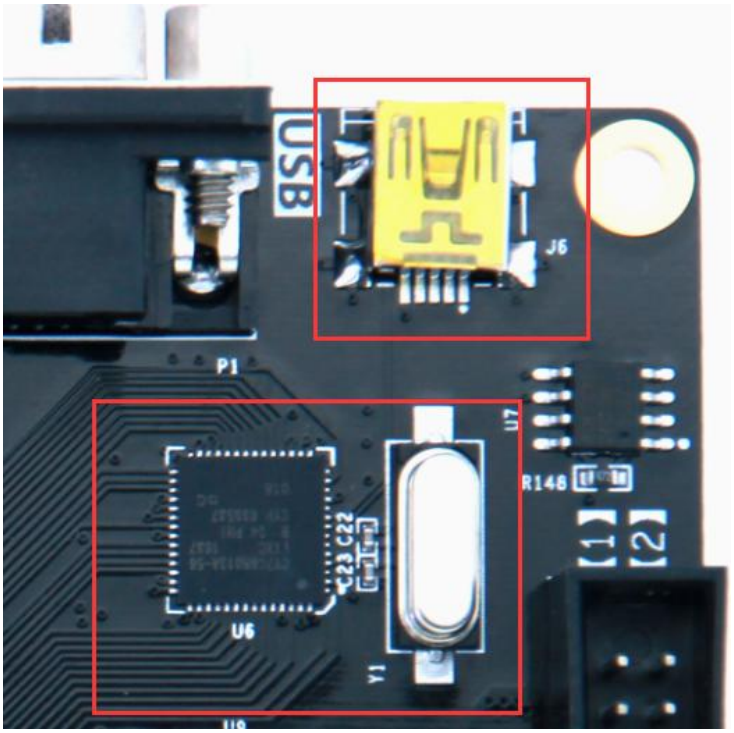


Figure 3-5-2 USB2.0 Onboard

Pin Assignment of USB2.0

Net Name	FPGA PIN	Comments
USB_CLKOUT	U18	12, 24 or 48 MHz Clock Output
USB_IFCLK	Y21	Synchronously clock
USB_FLAGA	R18	Programmable slave-FIFO output status flag signal
USB_FLAGB	R14	Programmable slave-FIFO output status flag signal
USB_FLAGC	P14	Programmable slave-FIFO output status flag signal
USB_SLCS	P16	Slave FIFO chipset select
USB_SLWR	R19	Slave FIFO write signal
USB_SLRD	P19	Slave FIFO read signal
USB_SLOE	N13	Slave FIFO Data Output Enable
USB_PKTEND	P20	Commit the FIFO packet data to the endpoint
USB_FIFOADR[0]	N14	FIFO address 0
USB_FIFOADR[1]	N15	FIFO address 1
USB_FD[0]	Y22	USB bidirectional data Bit0
USB_FD[1]	W20	USB bidirectional data Bit1
USB_FD[2]	W19	USB bidirectional data Bit2
USB_FD[3]	Y19	USB bidirectional data Bit3
USB_FD[4]	Y18	USB bidirectional data Bit4
USB_FD[5]	V22	USB bidirectional data Bit5
USB_FD[6]	U22	USB bidirectional data Bit6
USB_FD[7]	T18	USB bidirectional data Bit7
USB_FD[8]	R17	USB bidirectional data Bit8
USB_FD[9]	R16	USB bidirectional data Bit9
USB_FD[10]	P15	USB bidirectional data Bit10

USB_FD[11]	N17	USB bidirectional data Bit11
USB_FD[12]	P17	USB bidirectional data Bit12
USB_FD[13]	U16	USB bidirectional data Bit13
USB_FD[14]	T16	USB bidirectional data Bit14
USB_FD[15]	U17	USB bidirectional data Bit15

(六) SD Socket

Many applications use a large external storage device, such as SD Card or CF card, for storing data. The AX7102 board provides the hardware needed for SD Card access. FPGA can access the SD Card in SPI mode and SD Card 4-bit or 1-bit mode. Figure 3-6-1 shows the related design of SD interface.

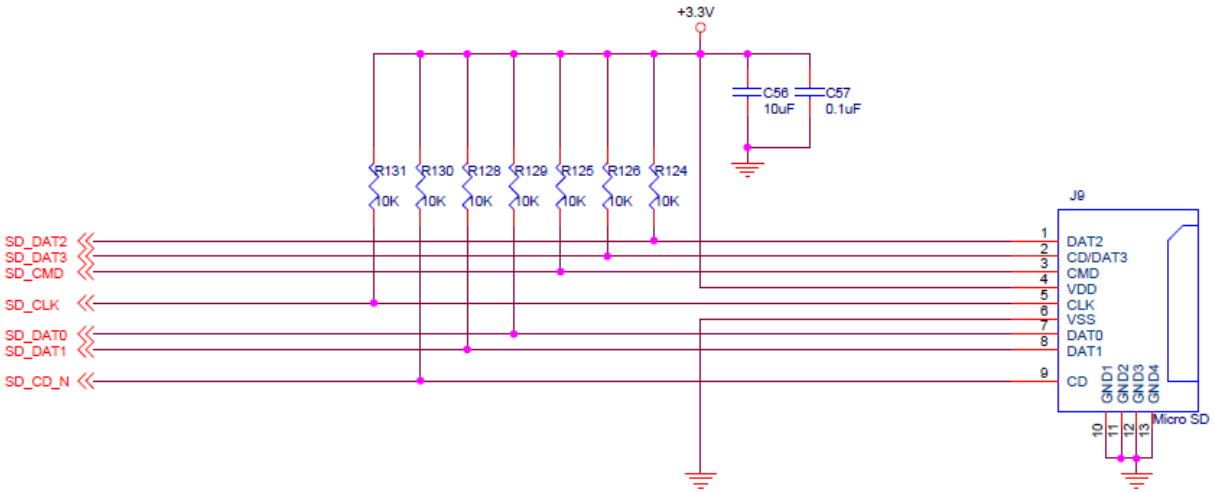


Figure 3-6-1 Design of SD Interface

SD card socket is on the bottom of the AX7102 board, the Figure 3-6-2 shows the SD card socket on board.

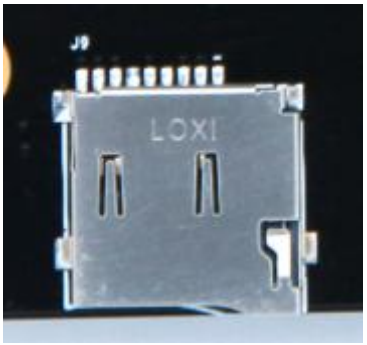


Figure 3-6-2 SD Card Socket On Board

Pin Assignment of SD Socket

SD Mode	
Net Name	FPGA PIN
SD_CLK	C14
SD_CMD	C15
SD_CD_N	B16
SD_DAT0	E17
SD_DAT1	F16
SD_DAT2	A14
SD_DAT3	A13

(七) USB Serial Port

The board provides a MINI USB interface connector(J3) as a UART serial port to communicate with PC computer or other device. In AX7102 board, we use CP2102 chipset as an USB to UART bridge. When connecting an USB cable, FPGA board can communicate with PC for UART communication. The hardware design of USB UART is showed as Figure 3-7-1.

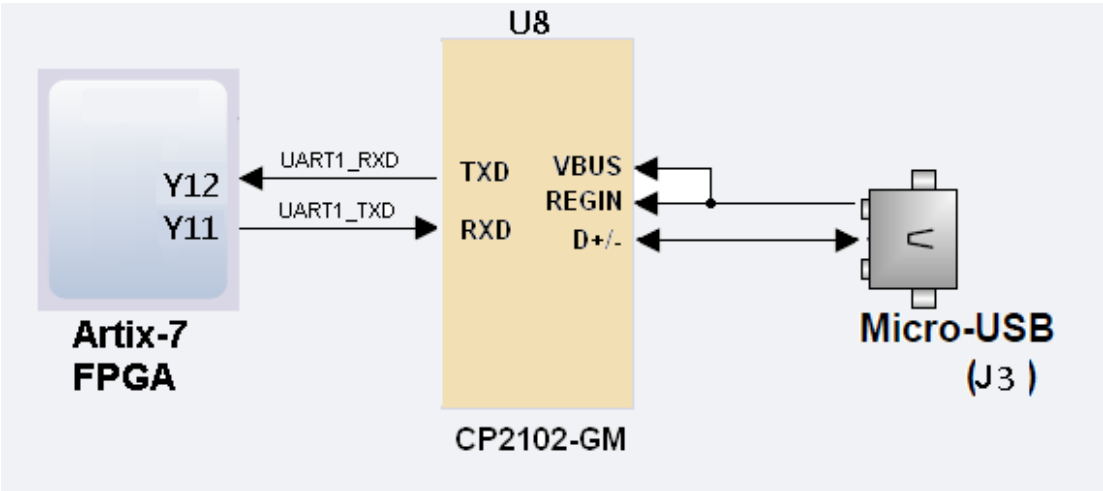


Figure 3-7-1 USB UART Interface

Figure 3-7-2 shows the USB UART onboard.

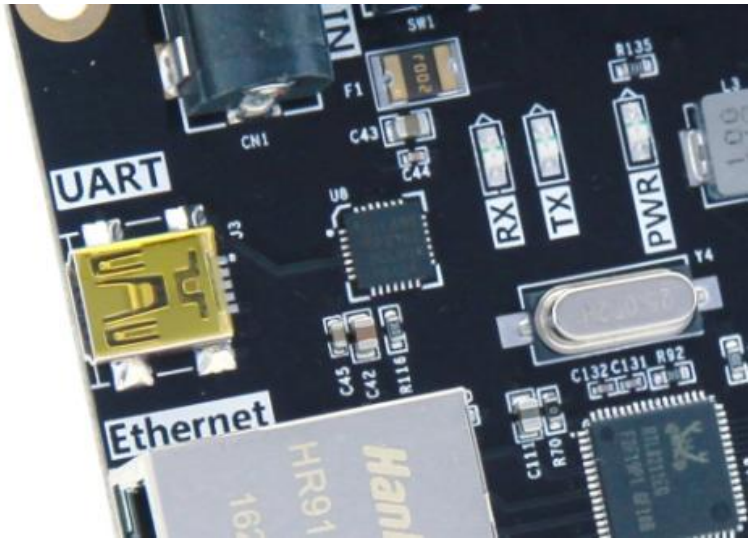


Figure 3-7-2 USB UART Onboard

There are two LEDs on board to indicate the UART operation status, the LED7 is used to indicate receiving status, and the LED8 is used to indicate sending status. The indication LEDs is design as Figure 3-7-3.

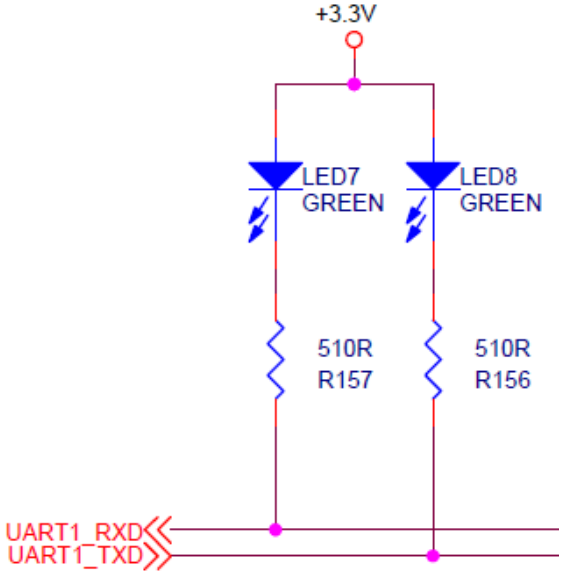


Figure 3-7-3 USB UART LED Indication

PIN Assignment of USB UART.

Net Name	FPGA PIN
UART1_RXD	Y12
UART1_TXD	Y11

(八) RS232 Port

The AX7102 board uses the MAX3232 transceiver chip and a 9-pin DB9 connector for RS-232 communications. Figure 3-8-1 shows the related hardware design of RS-232 interface.

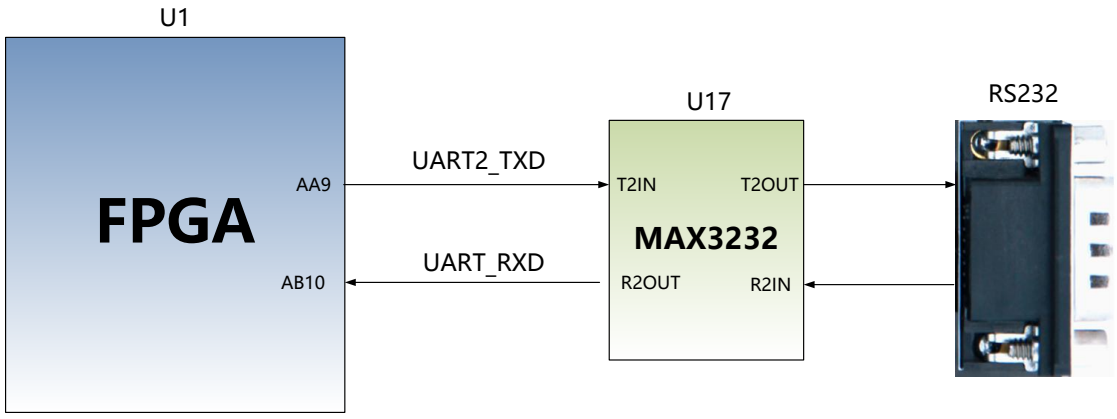


Figure 3-8-1 Hardware Design of RS232 Interface

Figure 3-8-2 shows the RS232 interface onboard.

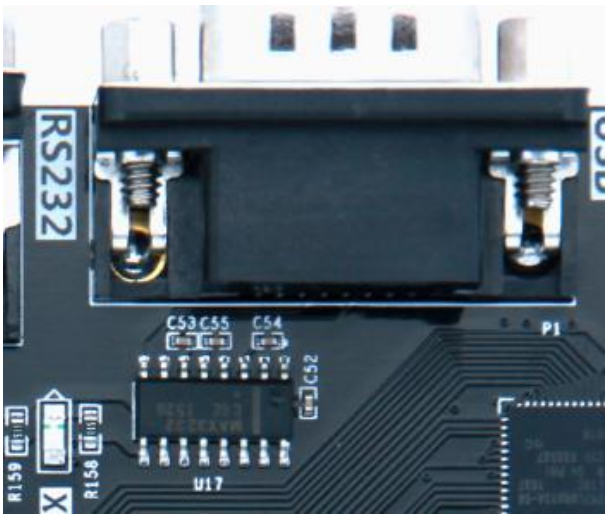


Figure 3-8-2 RS232 interface onboard

Pin Assignment of RS232 Interface.

Net Name	FPGA PIN
UART2_RXD	AB10
UART2_TXD	AA9

(九) EEPROM 24LC04

One 4Kbit EEPROM is used to store the data and serial number as well as the board information and other data. It is connected to FPGA IO using the I2C bus. The data in EEPROM will not lost even board is power off. The hardware design of EEPROM is showed as Figure 3-9-1

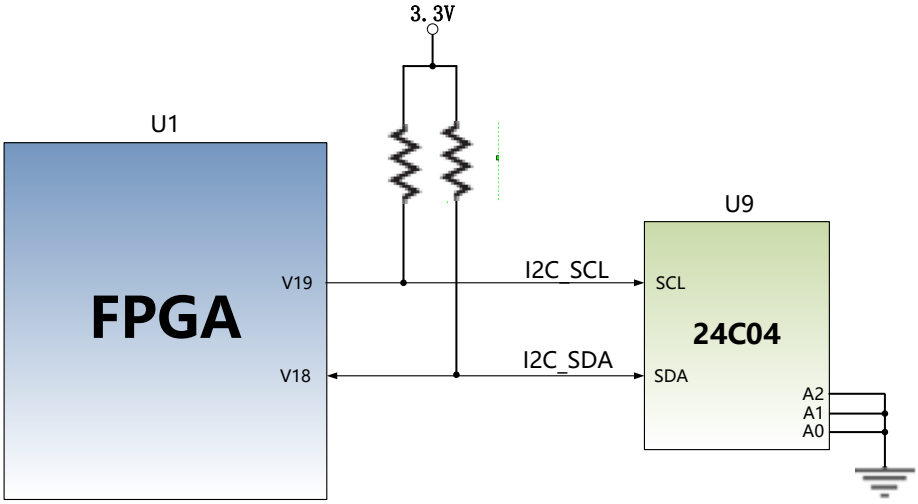


Figure 3-9-1 EEPROM Hardware Design

Figure 3-9-2 shows the EEPROM on board.

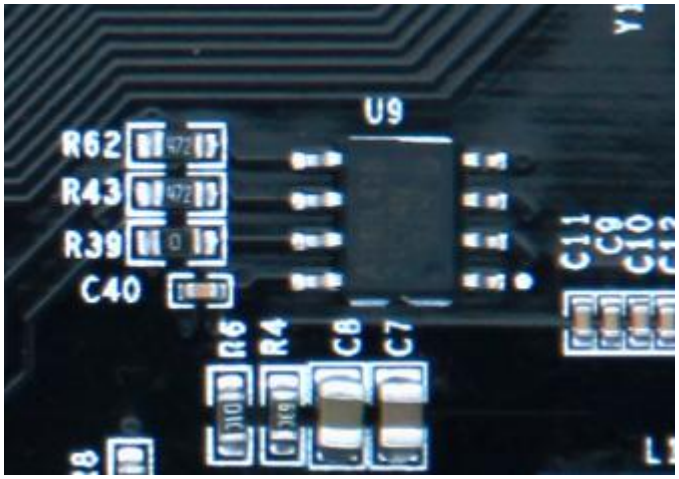


Figure 3-9-2 EEPROM Onboard

EEPROM PIN Assignment

Net Name	FPGA PIN
I2C_SCL	V19
I2C_SDA	V18

(十) RTC

A real time clock (DS1302) is connected to FPGA with serial interface. the DS1302 will provide the time information(Year/Weeks/Hours/Seconds/Minutes) to FPGA system. An external 32.768KHz clock is required to providing accurate clock source for DS1302 chipset normal operation. In order that RTC can run normally even board is power down, a battery need to be equipped, the P/N of battery is CR1220. The hardware design of RTC is showed as Figure 3-10-1.

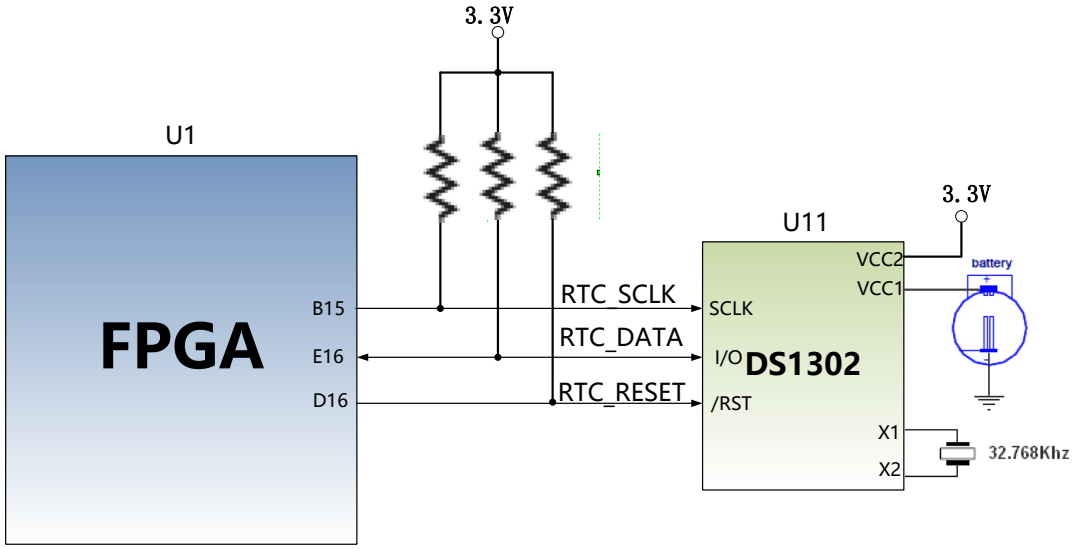


Figure 3-10-1 DS1302 Hardware Design

Figure 3-10-2 is RTC circuit on AX7102 board.

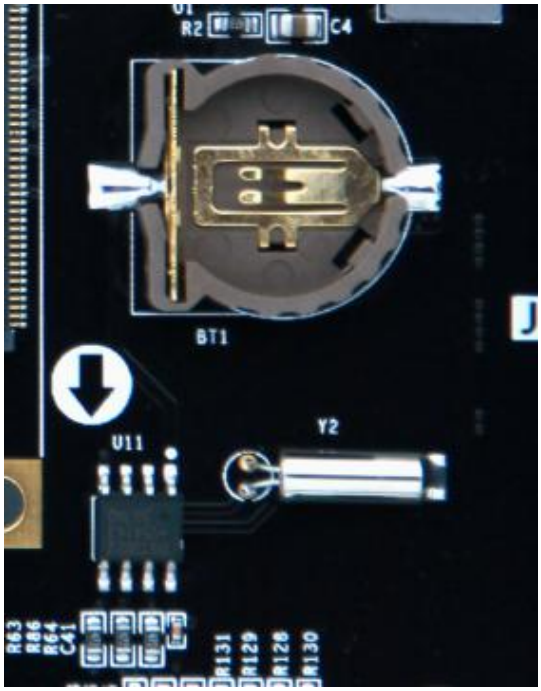


Figure 3-10-2 RTC Circuit on Board

DS1302 Pin Assignment.

Net Name	FPGA PIN
RTC_SCLK	B15
RTC_DATA	E16
RTC_RESET	D16

(十一) GPIO Expansion Headers

The AX7102 Board provides 40-pin expansion header. The header connects directly to 34 pins of the Artix-7 FPGA, and also provides +5.0V, +3.3V and GND.

The FPGA IO pins on the expansion headers is connected to a 33ohm resistor for protection against high or low voltage level. Figure 3-11-1 and Figure 3-11-3 shows the connection circuitry of these two 40-pin expansion headers.

Figure 3-11-1 shows the connection of J4 expansion header

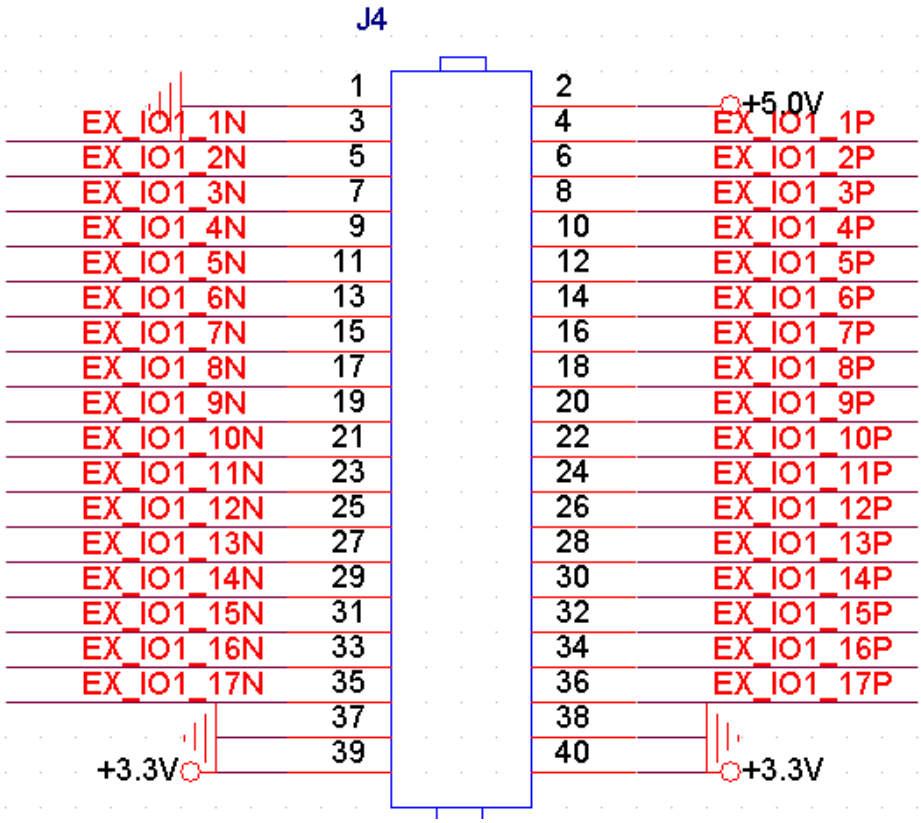


Figure 3-11-1 Connection of J4 expansion header

Figure 3-11-2 is the header of J4 on AX7102 board, the Pin1, Pin2 of connector is marked on PCB board.

Figure 3-11-2 Header of J4 Onboard

Pin Assignment of J4 Expansion Header.

J4 Pin	FPGA Pin	J4 Pin	FPGA Pin
1	GND	**2**	+5V
3	K14	**4**	K13
5	H14	**6**	J14
7	H15	**8**	J15
9	G13	**10**	H13
11	J21	**12**	J20

13	G16	**14**	G15
15	H19	**16**	J19
17	G18	**18**	G17
19	J16	**20**	F15
21	K22	**22**	K21
23	H22	**24**	J22
25	G20	**26**	H20
27	G22	**28**	G21
29	D22	**30**	E22
31	D21	**32**	E21
33	A21	**34**	B21
35	M17	**36**	F21
37	GND	**38**	GND
39	+3.3V	**40**	+3.3V

Figure 3-11-3 shows the connection of J5 expansion header.

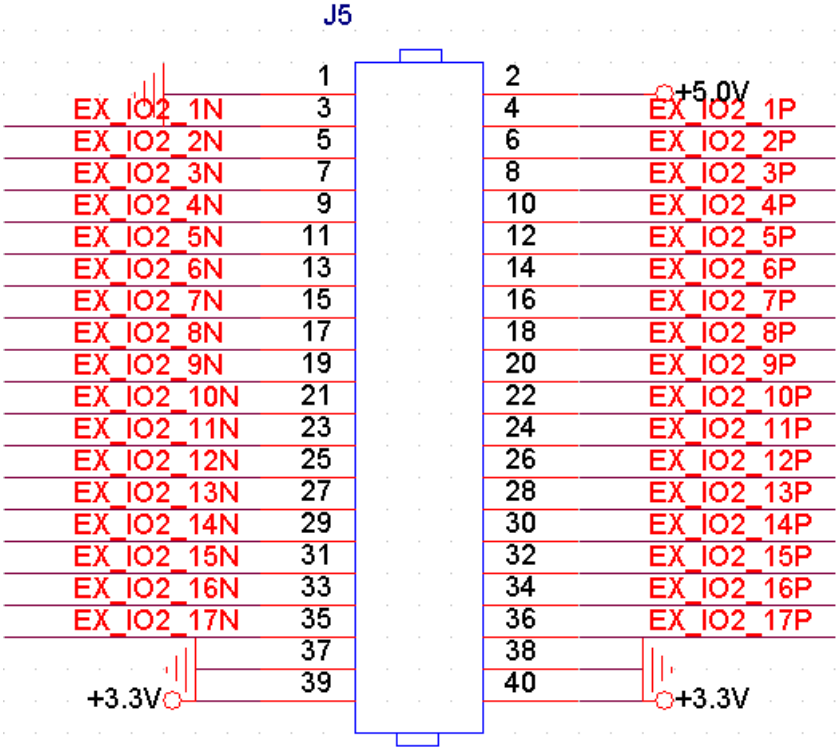


Figure 3-11-3 Connection of J5 expansion header

Figure 3-11-4 is the header of J5 on AX7102 board, the Pin1, Pin2 of connector is marked on PCB board.

Figure 3-11-4 Header of J4 Onboard

Pin Assignment of J5 Expansion Header.

J4 Pin	FPGA Pin	J4 Pin	FPGA Pin
1	GND	**2**	+5V
3	AB15	**4**	AA15
5	AA14	**6**	Y13
7	AB17	**8**	AB16
9	AA16	**10**	Y16
11	AB12	**12**	AB11
13	Y14	**14**	W14
15	C19	**16**	C18
17	F14	**18**	F13
19	E14	**20**	E13
21	D15	**22**	D14
23	B13	**24**	C13
25	AB13	**26**	AA13
27	A19	**28**	A18
29	E18	**30**	F18
31	F20	**32**	F19
33	A20	**34**	B20
35	D19	**36**	E19
37	GND	**38**	GND
39	+3.3V	**40**	+3.3V

(十二) JTAG Interface

The AX7102 Board reserves a 10Pin JTAG interface for downloading programs to FPGA QSPI FLASH. Each pin of JTAG interface on the expansion headers is connected to two diodes and a resistor that provides protection against high and low voltages. Figure 3-12-1 shows hardware design of JTAG interface.

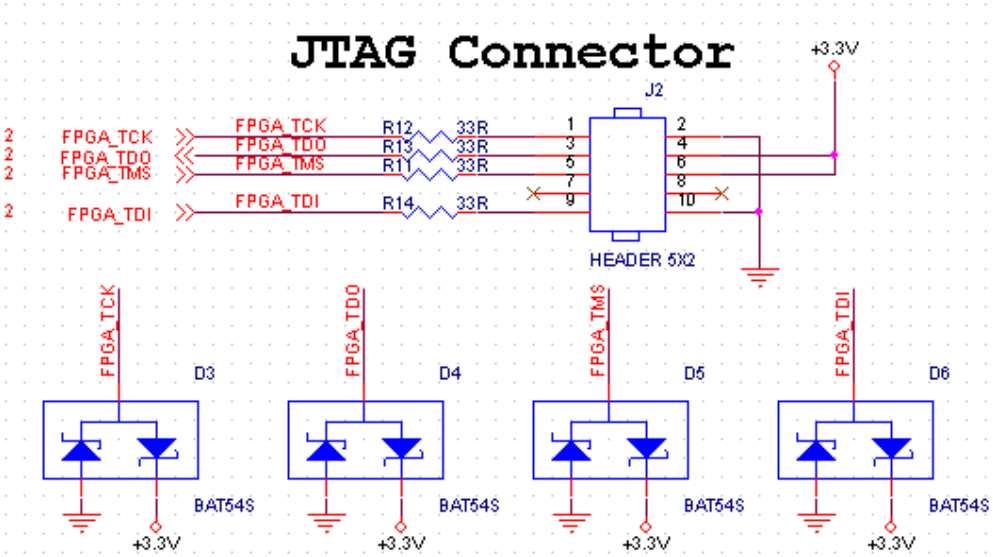


Figure 3-12-1 JTAG Interface

JTAG connector is standard 10pin connector, the pitch is 2.54mm. Figure 3-12-2 shows the onboard JTAG connector .

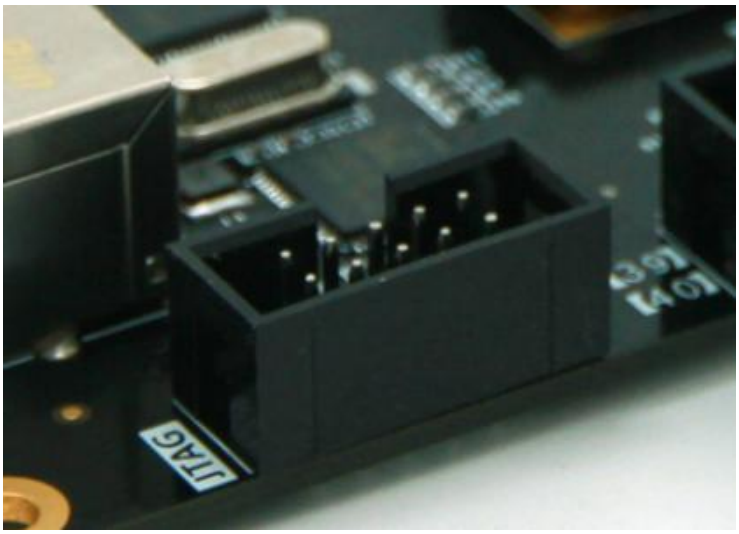


Figure 3-12-2 Onboard JTAG Connector

(十三) Buttons

AX7102 expansion board has four user buttons, all of buttons are active low

voltage when buttons are pressed down. The hardware design of the four user buttons is shown in Figure 3-13-1.

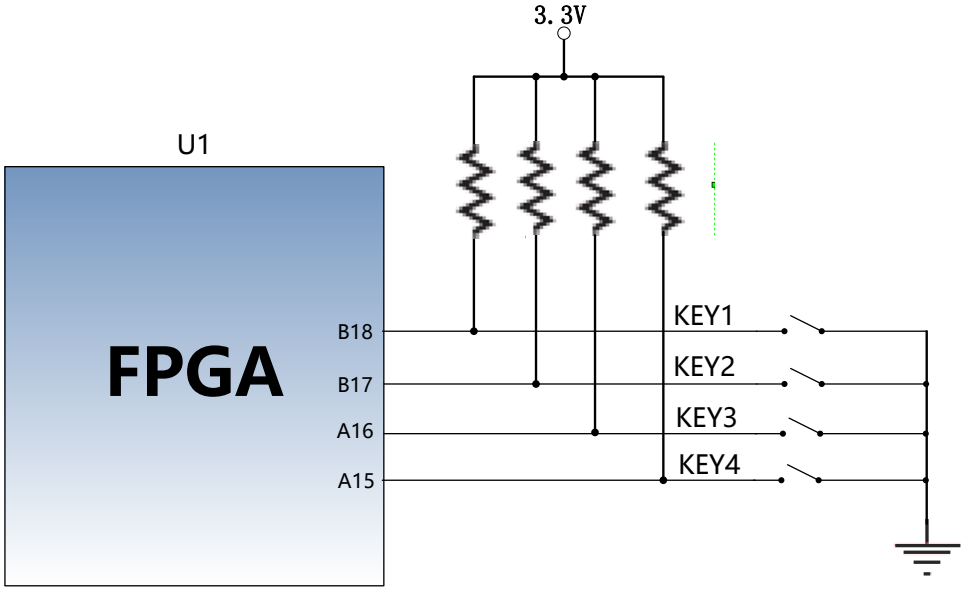


Figure 3-13-1 Design of User Buttons

Figure 3-13-2 is the four buttons onboard.

Figure 3-13-2 Four Buttons Onboard

Pin Assignment of Buttons.

Net Name	FPGA PIN
KEY1	B18
KEY2	B17
KEY3	A16
KEY4	A15

(十四) LED

The expansion board has four user RED LEDs. These four RED LEDs will light on when low voltage is output from FPGA IO. The design of LEDs is showed as

Figure 3-14-1.

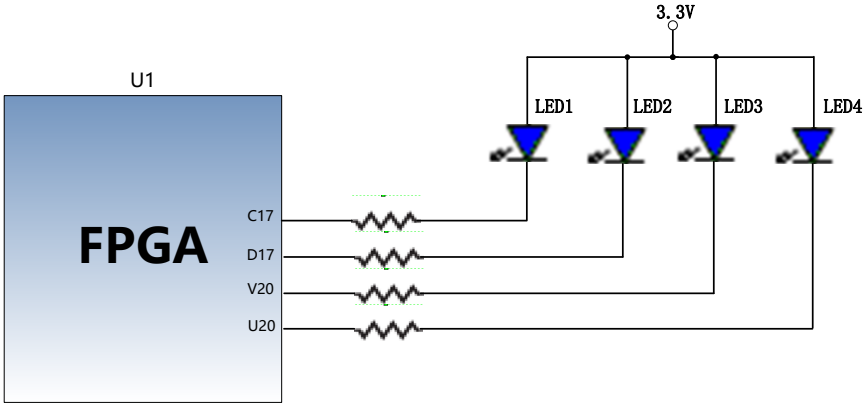


Figure 3-14-1 Four User LEDs

Figure 3-14-2 is four user LEDs on expansion board.

Figure 3-14-2 Four User LEDs Onboard

Pin Assignment of User LEDs.

Net Name	FPGA PIN
LED1	C17
LED2	D17
LED3	V20
LED4	U20

(十五) POWER

AX7102 board power input voltage is DC12V, please use the AC adapter we provided. The DC12V will generate two power of +5.0V and +3.3V through the MP1482 DC/DC convertor. The converted +5.0V power is used for the power supply of core board. The power design of AX7102 is showed as Figure 3-15-1.

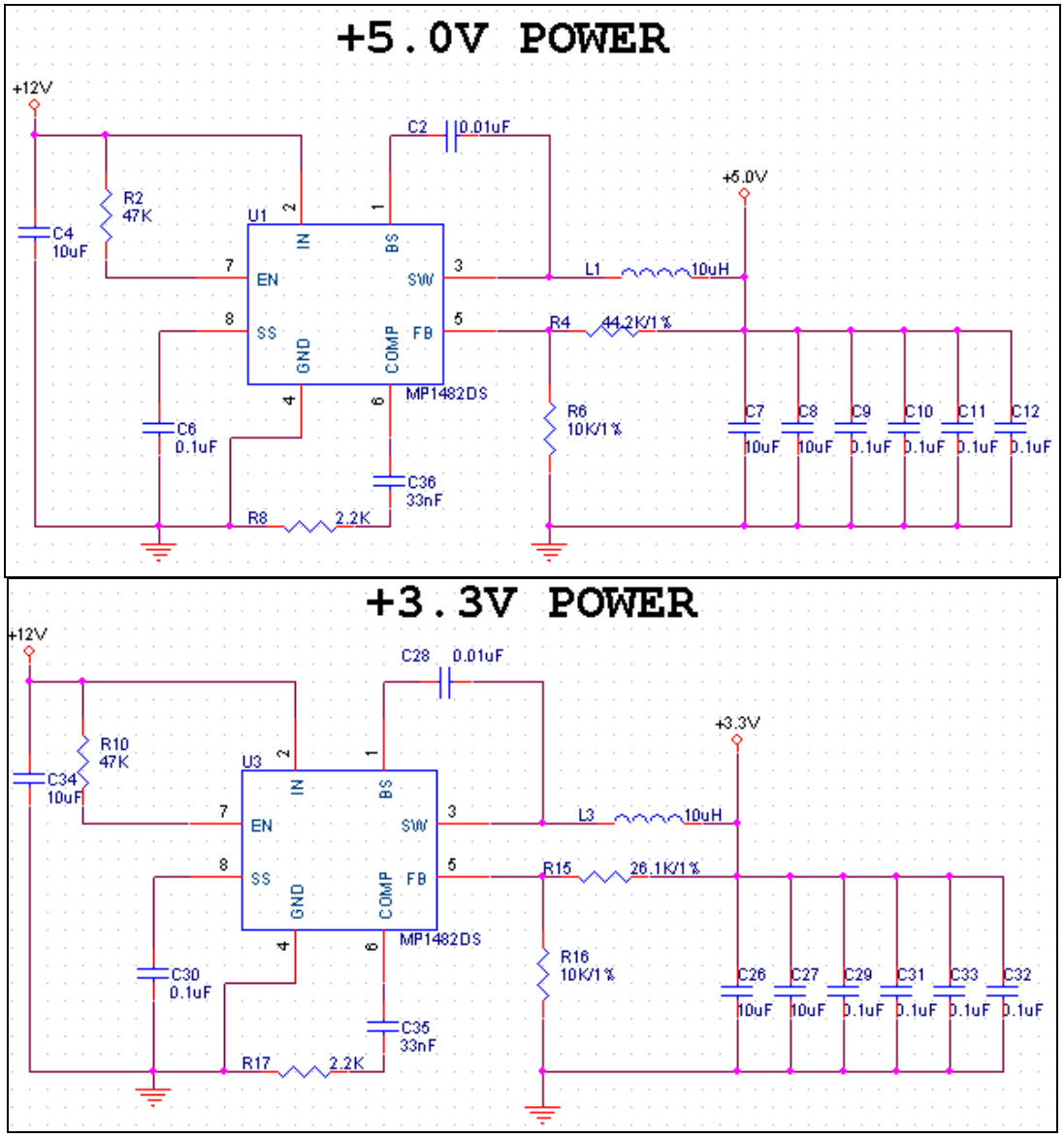


Figure 3-15-1 Power Design of AX7102

Figure 3-15-2 and Figure 3-15-3 is the DC/DC circuit on board.

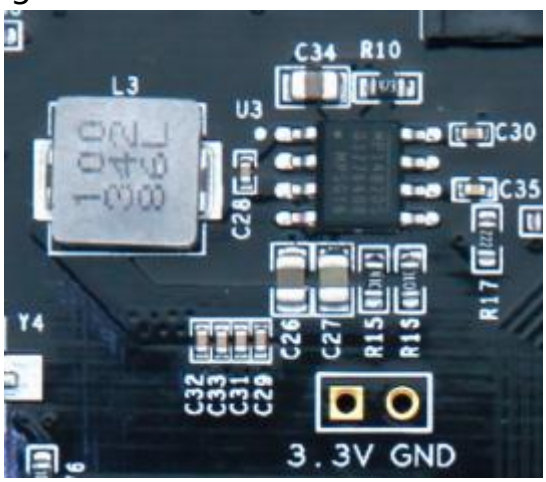


Figure 3-15-2 Power Circuit of +3.3V

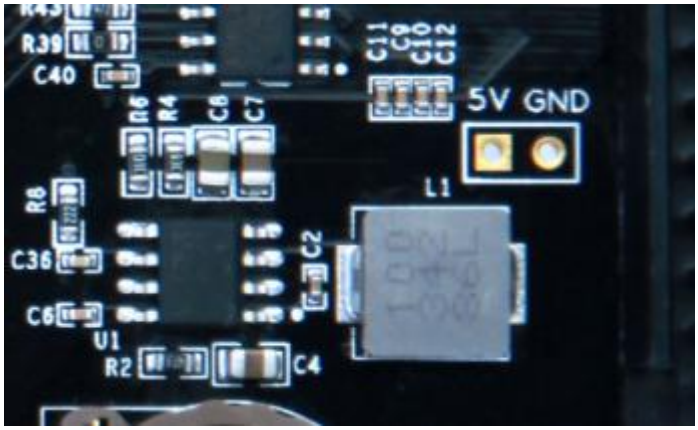


Figure 3-15-3 Power Circuit of +5.0V