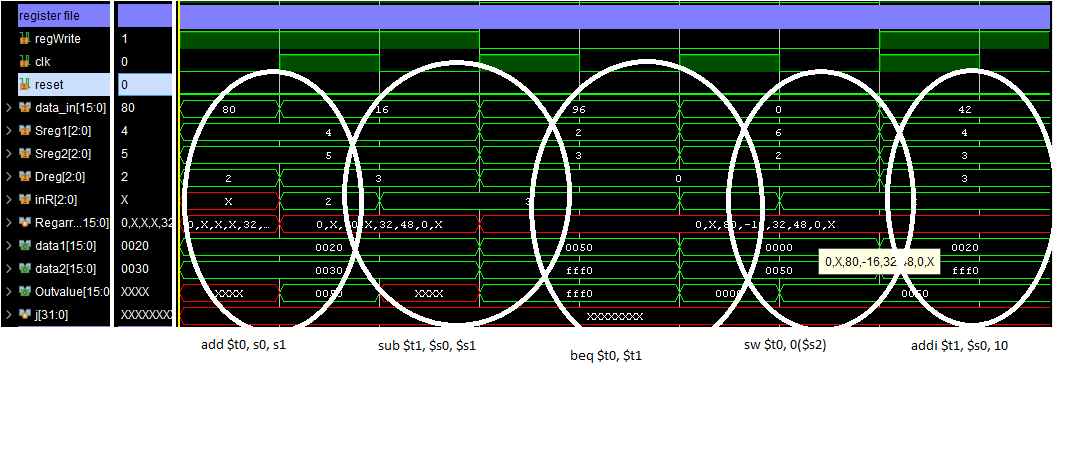
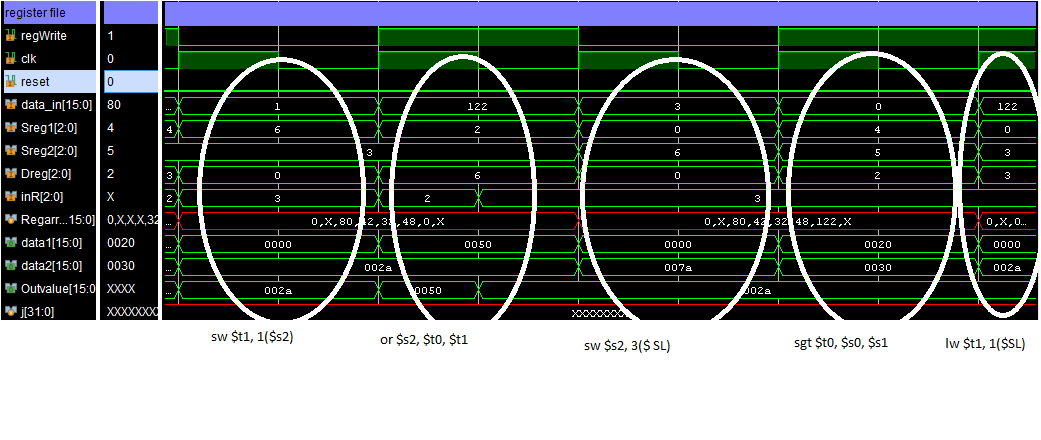


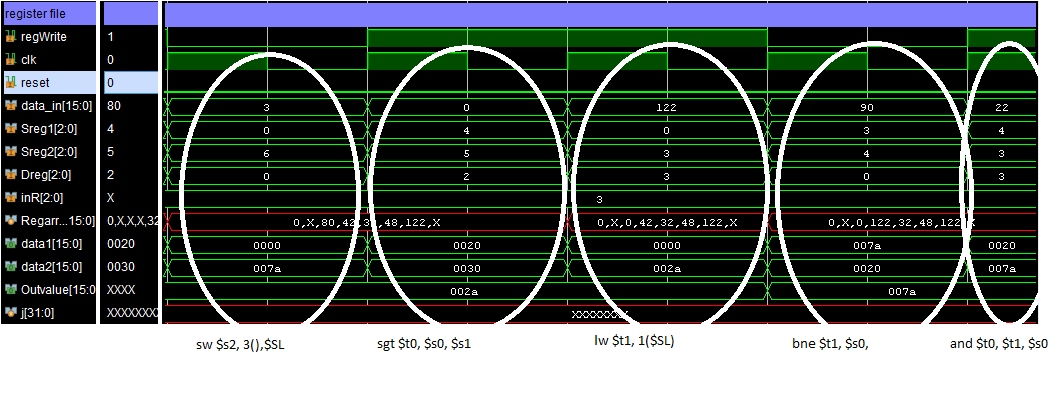
Top-level component comprising the block memory and the instruction memory connected to the datapath.

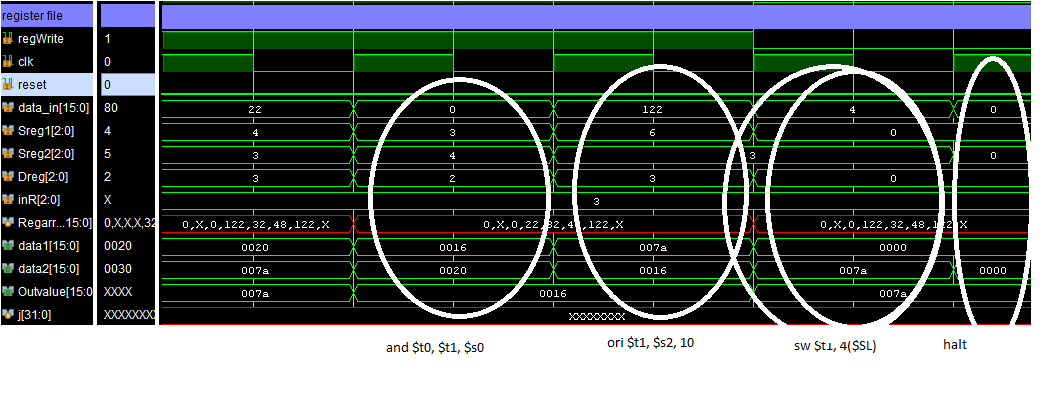
**SIMULATION RESULTS**

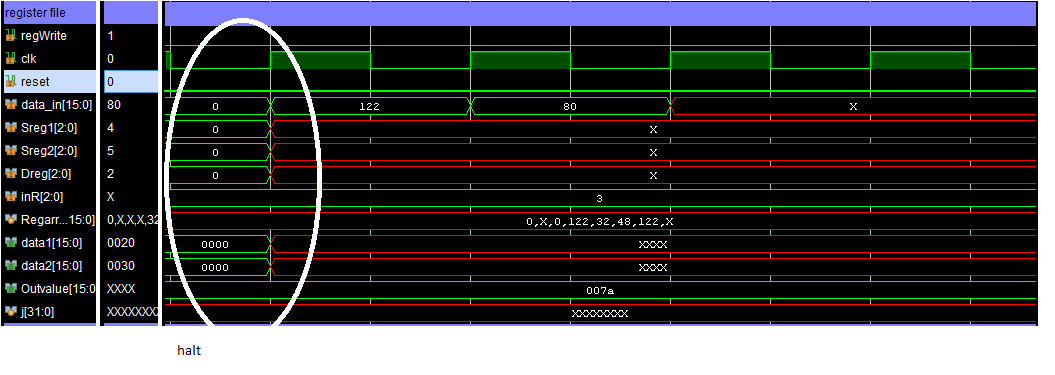
**Register file**

****

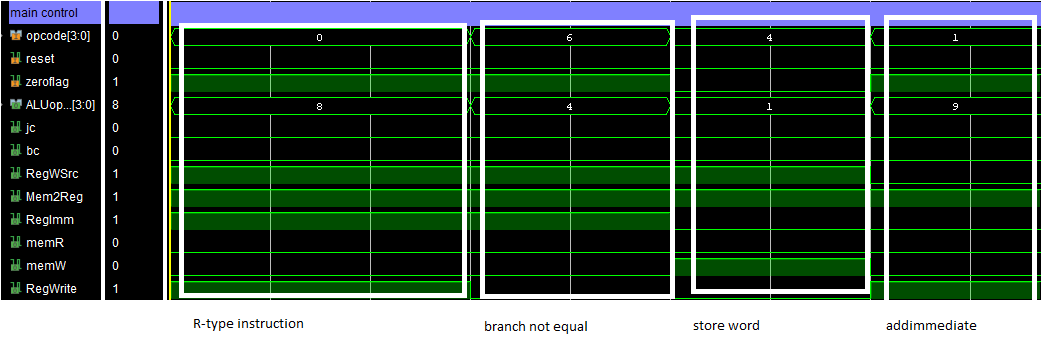
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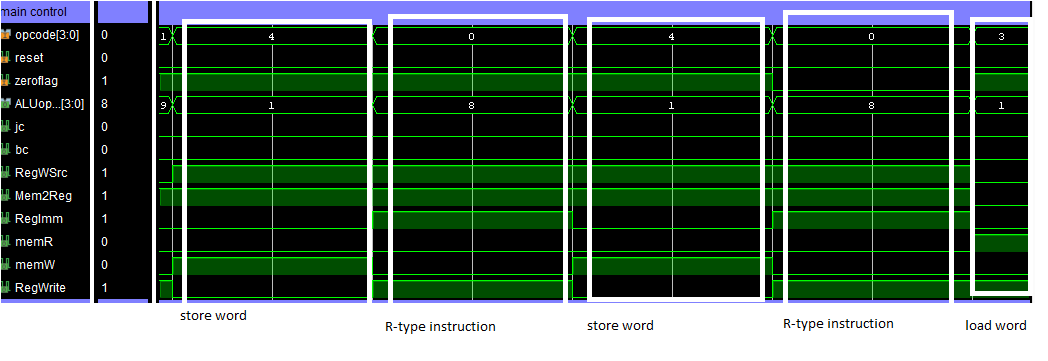


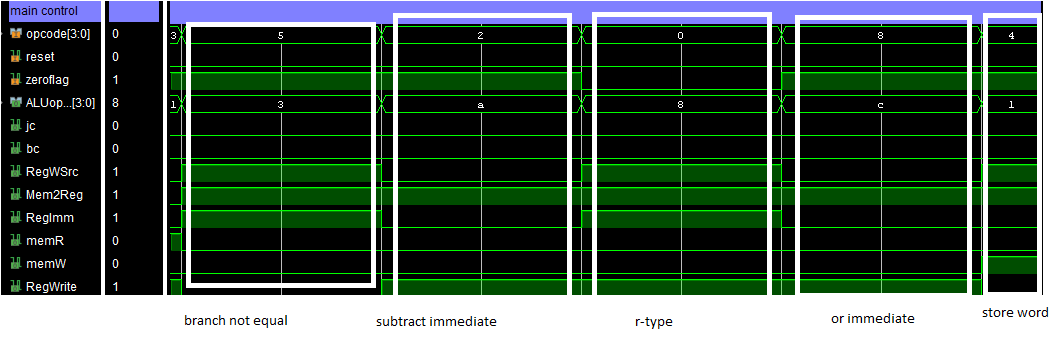


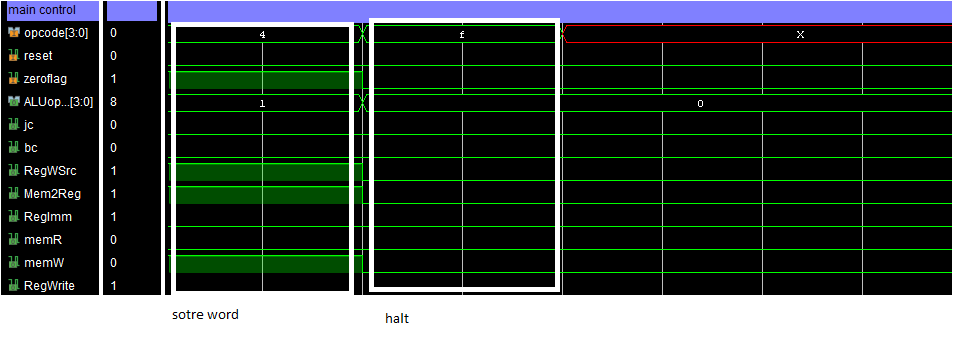


Control

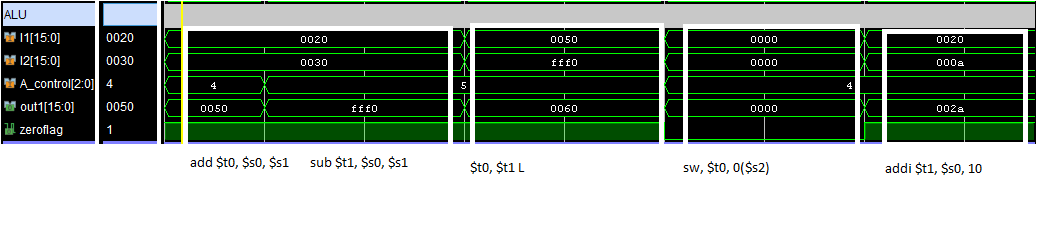


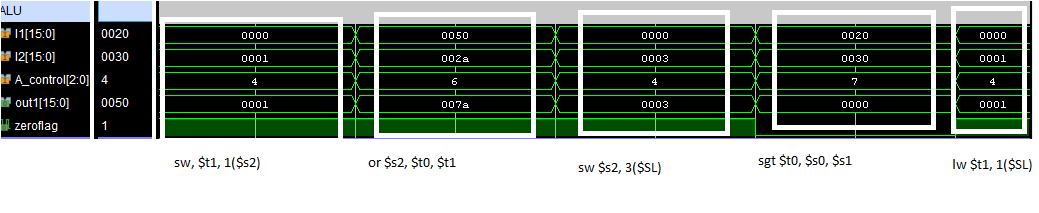


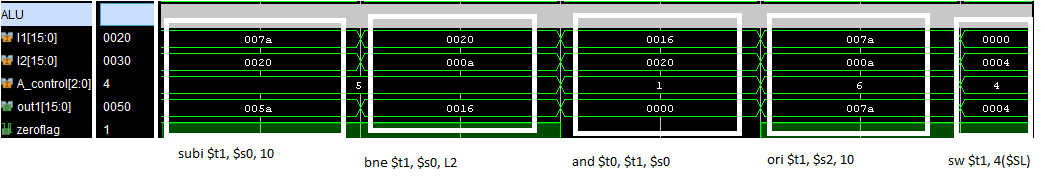


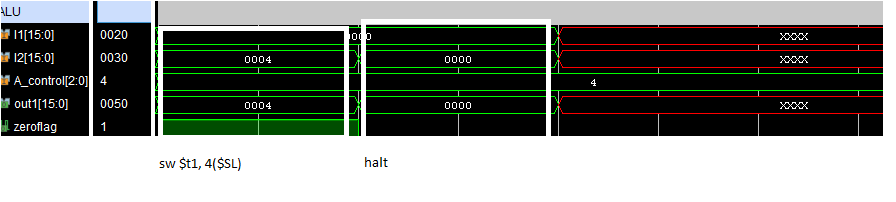


**ALU**

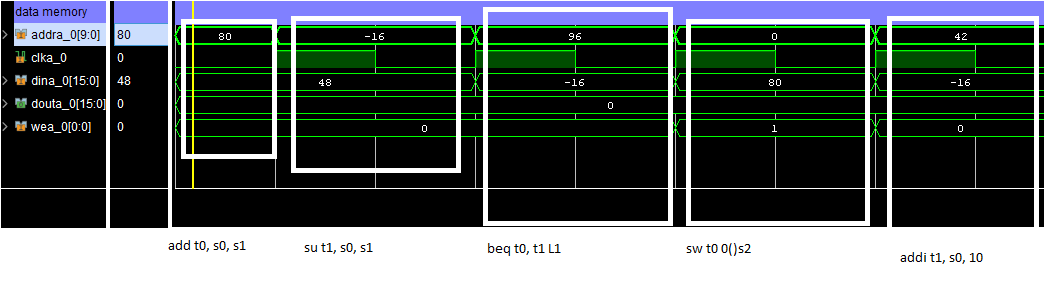
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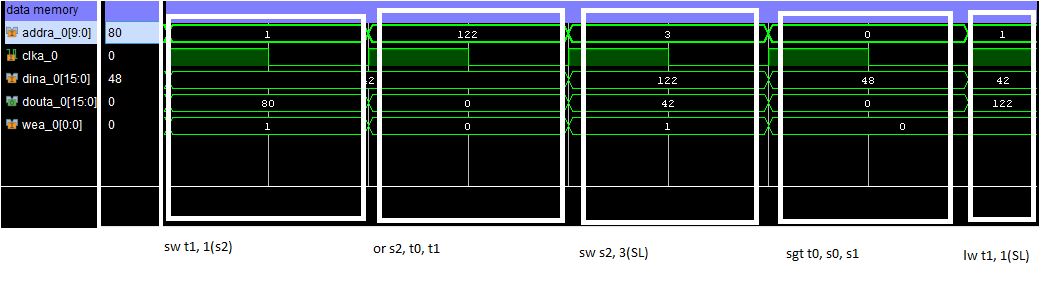
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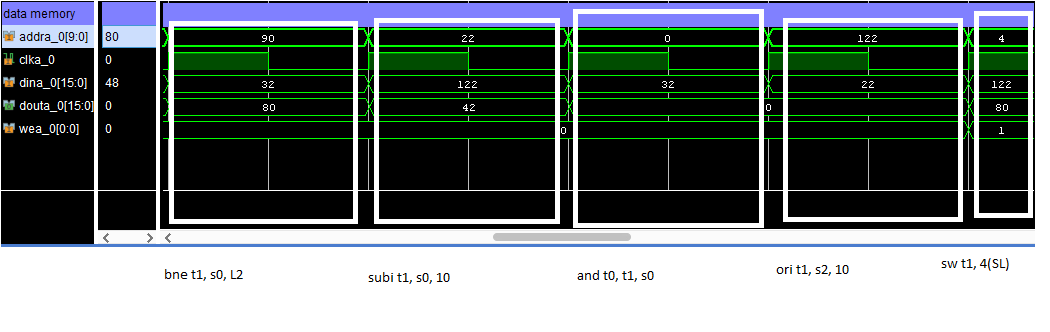
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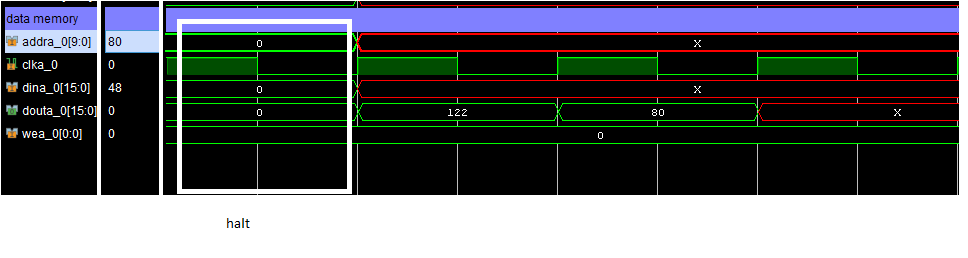
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**Data memory**

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**Assembly code and machine code**

|  |  |
| --- | --- |
| Add $t0, $s0, $s1 | 0000100101010000 |
| Sub $t1, $s0, $s1 | 0000100101011001 |
| Beq $t0, $t1 L1 | 0110010011000010 |
| Sw $t1, 0($s2) | 0100110010000000 |
| Addi $t1, $s0, 10 | 0001100011001010 |
| Sw $t1, 1($s2) | 0100110011000001 |
| L1 Or $s2, $t0, $t1 | 0000010011110011 |
| Sw $s2, 3($SL) | 0100000110000011 |
| Sgt $t0, $s0, $s1 | 0000100101010111 |
| lw $t1, 0($SL) | 0011000011000001 |
| Bne $t0, $s0, L2 | 0101011100000011 |
| Subi $t1, $s0, 10 | 0010100011001010 |
| And $t0, $t1, $s0 | 0000011100010010 |
| L2 Ori $t1, $s2, 10 | 1000110011001010 |
| Sw $t1, 4($SL) | 0100000011000100 |
| Halt | 1111000000000000 |