5 Replies Latest reply: Sep 5, 2014 12:06 PM by caseyh

Lifu Aug 14, 2014 2:09 PM

Galileo UART driver

This question is **Assumed Answered.**

One of our customer is porting their OS onto x86 UART driver. We got a question about UART dirver which I have little exeperience on. Is there anyone who knows this area ca comment/confirm this?

*"We are looking into UART registers and as per **section 18.5 of the Quark data sheet**, we are able to read the BAR0 contents from Yocto linux ,with Bus 0, Device:20 Functio for UART1 and Bus:0 Device:20 Function:1 offset:10h UART0(ref **Section 6.3**)*

In Yocto we got BAR0 as 0x9000F000 (Physical address) with the following procedures.
PCI configuration for UART0 (BAR0 Bus:0, Device:20 Function:1 offset:10h)
MyCfgAddr[23:16] = 0; MyCfgAddr[15:11] = 20; MyCfgAddr[10:8] = 1;
MyCfgAddr[7:0] = 10h; MyCfgAddr[31] = 1;
outl(0xCF8, MyCfgAddr)
Register_Snapshot = inl(0xCFC) // got the address 0x9000F000
Using mmap (map from physical to logical address) we mapped all other registers and got similar values as mentioned in the data sheet (also shown in the below thread).

Similarly we are able to get the base address of UART1 as 0x9000B000 (function 5). To confirm this we have written a char into TX buffer of UART1 and it displayed in the deb with Galileo board.

So we believe that UART registers are memory mapped."

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JPMontero_Intel Jun 26, 2014 11:44 AM (in response to Lifu)

1. Re: Galileo UART driver

You are trying to access UART, but currently you can only access UART1, right?
Regards
JPMontero_Intel

Actions

Lifu Jun 26, 2014 6:54 PM (in response to JPMontero_Intel)

2. Re: Galileo UART driver

Yes, i think that's customer's case. I do not have their RTOS code though.

Actions

JPMontero_Intel Jul 10, 2014 3:57 PM (in response to Lifu)

3. Re: Galileo UART driver

Hi Lifu

We are currently working on obtaining more information regarding this post. As soon as we have an answer we will post it here.
Regards,
JPMontero_Intel

Actions

mon2 Jul 10, 2014 4:13 PM (in response to Lifu)

4. Re: Galileo UART driver

Hi. From the Quark datasheet, 18.5.10, the diagram shows that Bit 0 of this BAR0 is hardwired to be 0. As per the PCI spec, if the bit is 0 then the value in this BAR will be a m address. If it is 1, then the address is in I/O space. Same for BAR1.

Regards

Kumar

Actions

caseyh Sep 5, 2014 12:06 PM (in response to Lifu)

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5. Re: Galileo UART driver

Hello Lifu,

Does Sanjiv's reply below address your question? Please let us know if you still require assistance.

Best Regards,
Casey H.

Actions