स्वदेशी Microprocessor

Shakti- Peripherals

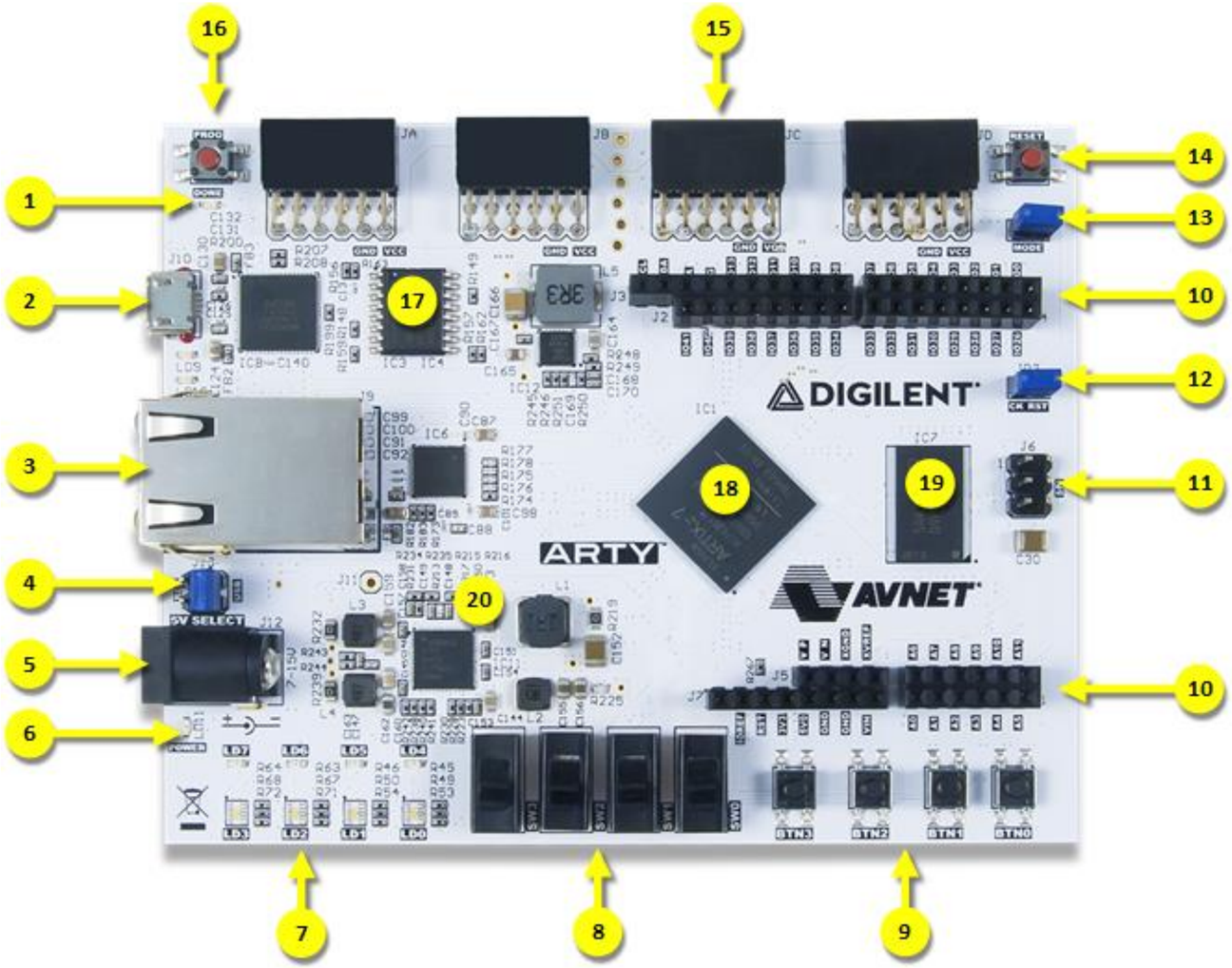
Overview

रा.इ.सू.प्रौ.सं
NIELIT

Agenda

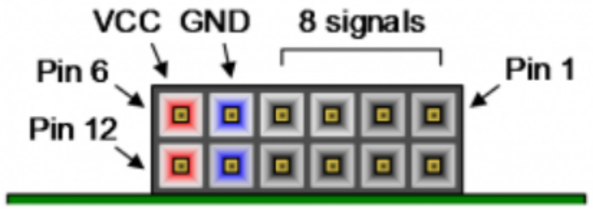
- Arty A7 on board connectors & Mapping
- Memory Mapping
- Pin Mapping
- GPIO Peripheral registers and configurations
- GPIO Library and Application Development

ARTY A7 – ARTIX-7 - 35T

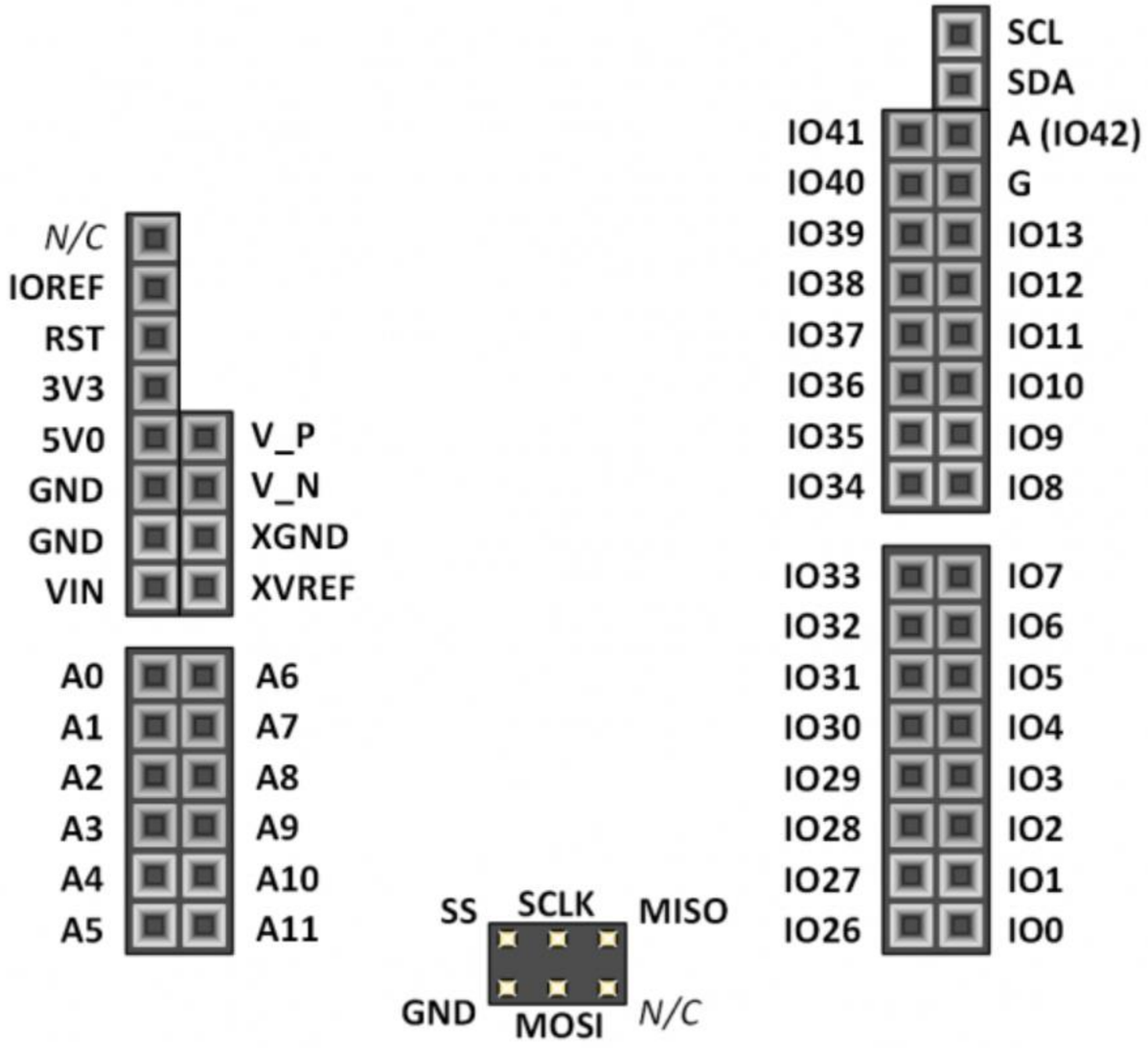


Callout	Description	Callout	Description
1	FPGA programming DONE LED	11	SPI header (Arduino/chipKIT compatible)
2	Shared USB JTAG / UART port	12	chipKIT processor reset jumper
3	Ethernet connector	13	FPGA programming mode (JTAG/ Flash)
4	Power select jumper (Ext. supply / USB)	14	chipKIT processor reset
5	Power jack (for optional ext. supply)	15	Pmod headers
6	Power good LED	16	FPGA programming reset button
7	User LEDs	17	SPI Flash
8	User slide switches	18	Artix FPGA
9	User pushbuttons	19	Micron DDR3 memory
10	Arduino/chipKIT shield connectors	20	Analog devices ADP 5052 power supply

Pmod Connectors



	Pmod JA	Pmod JB	Pmod JC	Pmod JD
Pmod Type	**Standard**	**High-Speed**	**High-Speed**	**Standard**
Pin 1	G13	E15	U12	D4
Pin 2	B11	E16	V12	D3
Pin 3	A11	D15	V10	F4
Pin 4	D12	C15	V11	F3
Pin 7	D13	J17	U14	E2
Pin 8	B18	J18	V14	D2
Pin 9	A18	K15	T13	H2
Pin 10	K16	J15	U13	G2


N/C
IOREF
RST
3V3
5V0
GND
GND
VIN
V_P
V_N
XGND
XVREF
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
SS
SCLK
MISO
GND
MOSI
N/C
SCL
SDA
IO41
IO40
IO39
IO38
IO37
IO36
IO35
IO34
A (IO42)
G
IO13
IO12
IO11
IO10
IO9
IO8
IO33
IO32
IO31
IO30
IO29
IO28
IO27
IO26
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IO0

Pin Mapping

Pin Name	Shield Function	Arty Connection
IO0-IO13, IO26-IO41, A (IO42)	General purpose I/O pins	See Section titled “Shield Digital I/O”
SCL	I2C Clock	See Section titled “Shield Digital I/O”
SDA	I2C Data	See Section titled “Shield Digital I/O”
SCLK	SPI Clock	See Section titled “Shield Digital I/O”
MOSI	SPI Data out	See Section titled “Shield Digital I/O”
MISO	SPI Data in	See Section titled “Shield Digital I/O”
SS	SPI Slave Select	See Section titled “Shield Digital I/O”
A0-A5	Single-Ended Analog Input	See Section titled “Shield Analog I/O”
A6-A11	Differential Analog Input	See Section titled “Shield Analog I/O”
V_P, V_N	Dedicated Differential Analog Input	See Section titled “Shield Analog I/O”

XGND	XADC Analog Ground	Connected to net used to drive the XADC ground reference on the FPGA (VREFN)
XVREF	XADC Analog Voltage Reference	Connected to 1.25 V, 25mA rail used to drive the XADC voltage reference on the FPGA (VREFP)
N/C	Not Connected	Not Connected
IOREF	Digital I/O Voltage reference	Connected to the Arty 3.3V Power Rail (See the "Power Supplies" section)
RST	Reset to Shield	Connected to the red "RESET" button and a Digital I/O of the FPGA. When JP2 is shorted, it is also connected to the DTR signal of the FTDI USB-UART bridge.
3V3	3.3V Power Rail	Connected to the Arty 3.3V Power Rail (See the "Power Supplies" section)
5V0	5.0V Power Rail	Connected to the Arty 5.0V Power Rail (See the "Power Supplies" section)
GND, **G**	Ground	Connected to the Ground plane of Arty
VIN	Power Input	Connected in parallel with the external power supply connector (J12). See the "Power Supplies" section for information on powering Arty from this pin.

Memory Map Arty7_35T

Sl.No	Peripheral	Base Address Start	Base Address End
1.	Memory (TCM)	0x80000000	0x8001FFFF
2.	Debug	0x00000010	0x0000001F
3.	PWM 0	0x00030000	0x000300FF
4.	PWM 1	0x00030100	0x000301FF
5.	PWM 2	0x00030200	0x000302FF
6.	PWM 3	0x00030300	0x000303FF
7.	PWM 4	0x00030400	0x000304FF

Sl.No	Peripheral	Base Address Start	Base Address End
8.	PWM 5	0x00030500	0x000305FF
9.	SPI 0	0x00020000	0x000200FF
10.	SPI 1	0x00020100	0x000201FF
11.	UART0	0x00011300	0x00011340
12.	UART1	0x00011400	0x00011440
13.	CLINT	0x02000000	0x020BFFFF
14.	GPIO	0x00040100	0x000401FF
15.	PLIC	0x0C000000	0x0C01001F
16.	I2C	0x00040000	0x000400FF
17.	XADC	0x00041000	0x00041400

PIN Mapping Artix7_35T

Sl. No	Pin Description	Pin mapping	Peripheral
1.1	GPIO0	CKIO0 (J4[1],IO - Lower	GPIO
1.2	GPIO1	CKIO1 (J4[3],IO - Lower)	
1.3	GPIO2	CIIO2 (J4[5],IO - Lower)	
1.4	GPIO3	CKIO3 (J4[7],IO - Lower)	
1.5	GPIO4	CKIO4 (J4[9],IO - Lower)	
1.6	GPIO5	CKIO5 (J4[11],IO - Lower)	
1.7	GPIO6	CKIO6 (J4[13],IO - Lower)	
1.8	GPIO7	CKIO7 (J4[15],IO - Lower)	
1.9	GPIO8	CKIO8 (J2[1],IO - Higher)	
1.10	GPIO9	CKIO9 (J2[3],IO - Higher)	
1.11	GPIO10	CKIO10 (J2[5],IO - Higher)	
1.12	GPIO11	CKIO11 (J2[7],IO - Higher)	
1.13	GPIO12	CKIO12 (J2[9],IO - Higher)	

Sl. No	Pin Description	Pin mapping	Peripheral
1.14	GPIO13	CKIO13 (J2[11],IO - Higher)	
1.15	GPIO14	CKIO26 (J4[2],IO - Lower)	
1.16	GPIO15	CKIO27 (J4[4],IO - Lower)	
2.1	SDA	CK_SDA(J3[1])	I2C
2.2	SCL	CK_SCL (J3[2])	
3.1	UART0 TX	J10	UART
3.2	UART0 RX	J10	
4.1	UART1 TX	JC[7] - 3P	
4.2	UART1 RX	JC[8] - 3N	
5.1	PWM 0	JD[1]	PWM PINS
5.2	PWM 1	JD[2]	
5.3	PWM 2	JD[3]	
5.4	PWM 3	JD[4]	
5.5	PWM 4	JD[7]	
5.6	PWM 5	JD[8]	

Sl. No	Pin Description	Pin mapping	Peripheral
6.1	SPI0 CS	JB[1] - 1P	SPI0
6.2	SPI0 SCLK	JB[2] - 1N	
6.3	SPI0 MISO	JB[3] - 2P	
6.4	SPI0 MOSI	JB[4] - 2N	
7.1	SPI1 CS	JB[7] - 3P	SPI1
7.2	SPI1 SCLK	JB[8] - 3N	
7.3	SPI1 MISO	JB[9] - 4P	
7.4	SPI1 MOSI	JB[10] - 4N	
8.1	ADC 4	CKA0	Single ended ADC
8.2	ADC 5	CK A1	
8.3	ADC 6	CK A2	
8.4	ADC 7	CK A3	
8.5	ADC 15	CK A4	

Sl. No	Pin Description	Pin mapping	Peripheral
8.6	ADC 0	CK A5	
9.1	ADC 12P	CK A6	Double ended ADC
9.2	ADC 12N	CK A7	
10.1	ADC 13P	CK A8	Double ended ADC
10.2	ADC 13N	CK A9	
11.1	ADC 14P	CK A10	Double ended ADC
11.2	ADC 14N	CK A11	

GPIO

- Compliance to the AMBA Specification for easy integration into SoC implementation.
- Sixteen individually programmable input/output pins.
- Default to input at reset.
- Provision for Bit masking in both read and write operations through address lines.

GPIO – Software Control

- Data Register
- Data Direction Register

GPIO Data Register

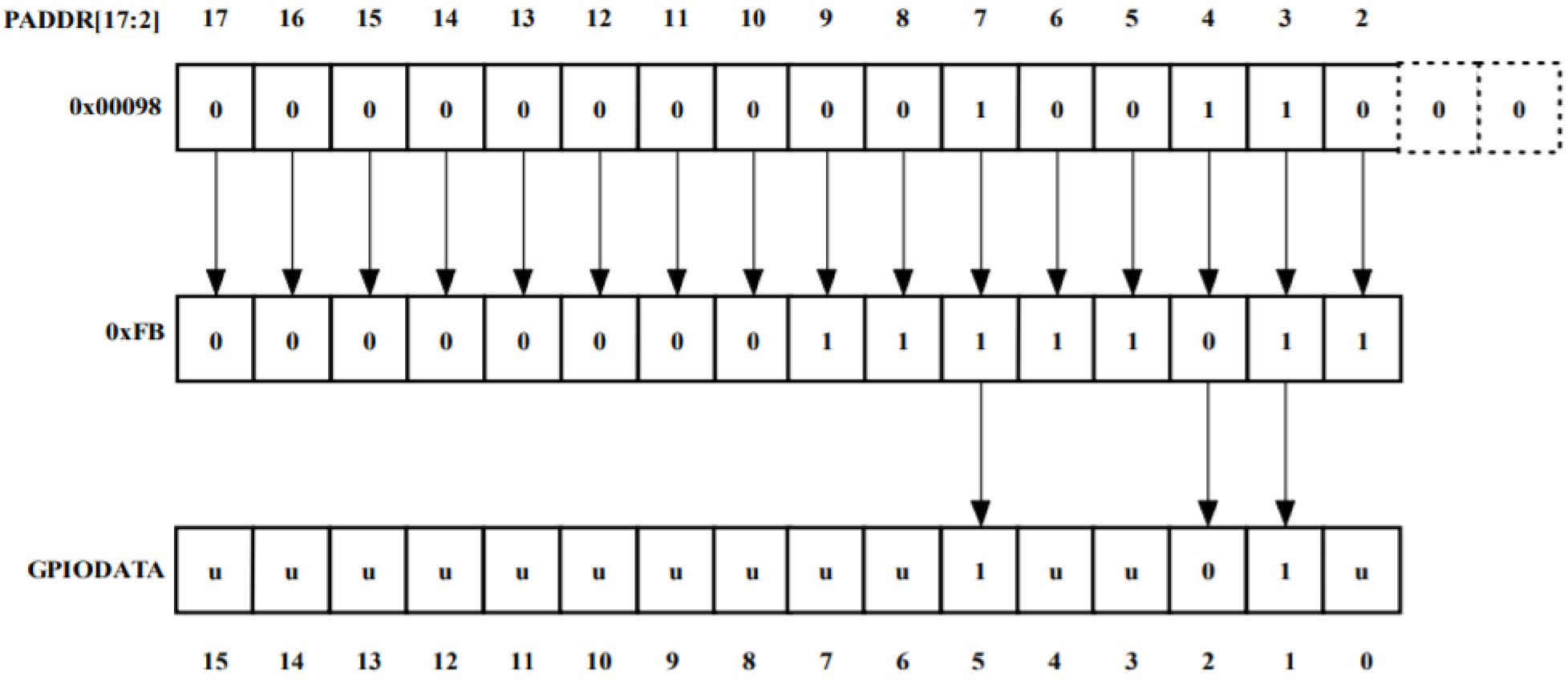
- The sixteen address lines used are PADDR [17: 2]
- PADDR[17:2], must be HIGH for making GPIO as output LOW will not make any effect.

Bits	Name	Type	Function
15:0	Data register	Read/ write	Input data Output data

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

GPIO Data register

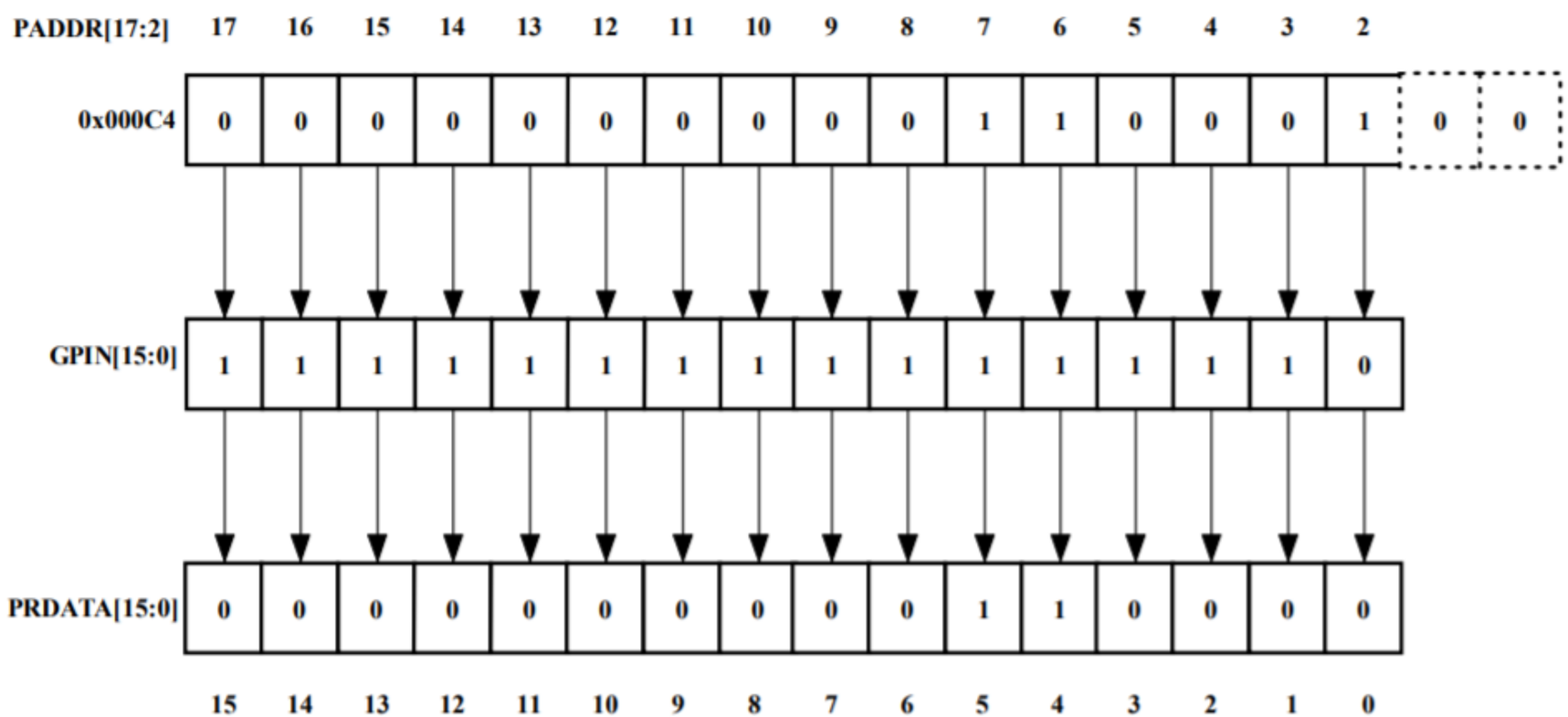
GPIO Write Operation



Example 1: Write to address 0x00098

GPIO Read operation

- Read from address GPIODATA + 0x000C4 = 0b00000000000011000100 PADDR[17:2] = 0b000000000110001.



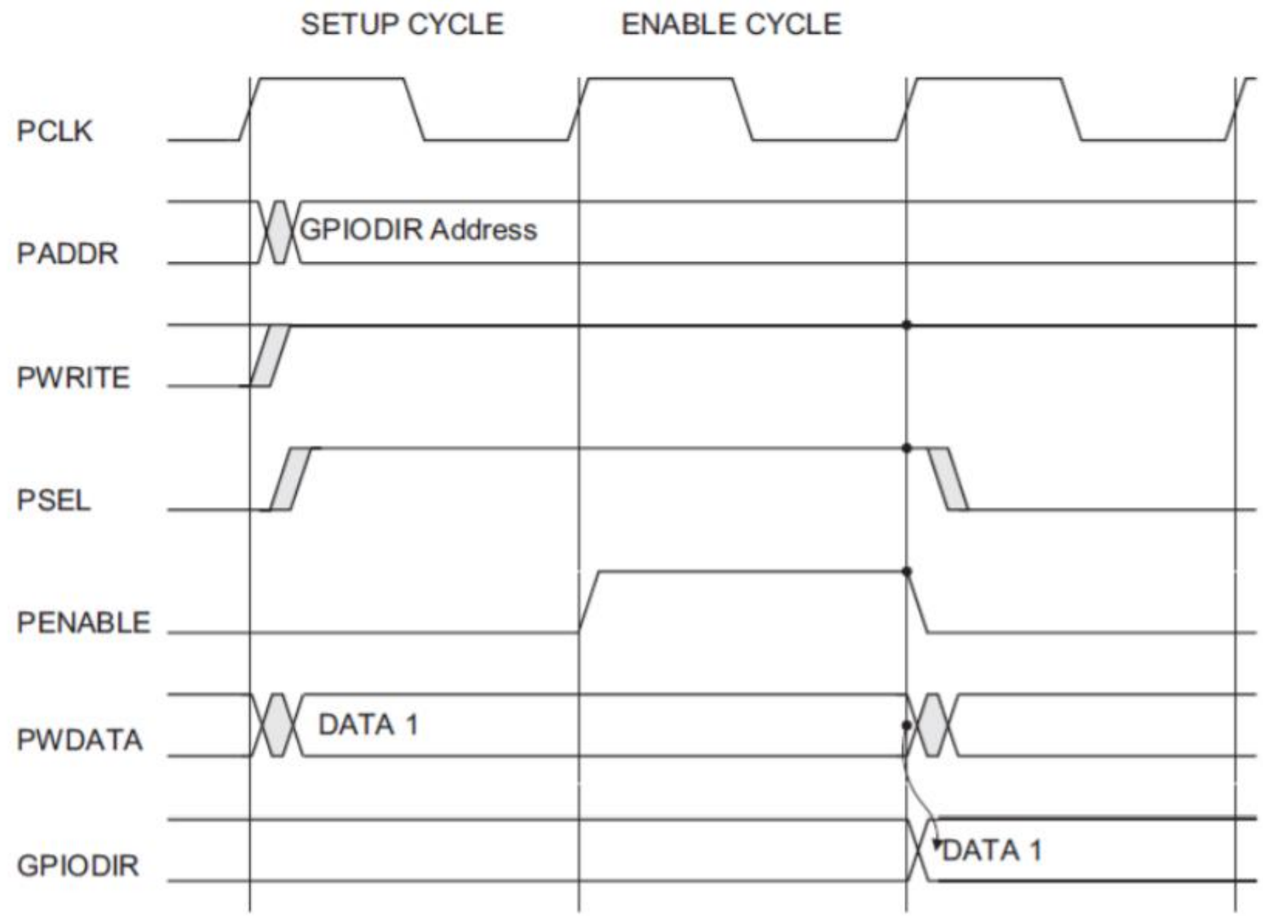
Data Direction Registers -GPIODIR

Bits	Name	Type	Function
15:0	Data direction register	Read/ write	Bits set, pins output Bits cleared, pins input

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Input mode	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Output mode	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

GPIODIR register

Write to Data Direction register:



GPIO Register

Address	Type	Width	Reset value	Name	Description
GPIO base + 0x00000 GPIO base + 0x3FFFC	Read/write	16	0x00000	GPIODATA	GPIO data register
GPIO base + 0x40000	Read/write	16	0x00000	GPIODIR	GPIO datadirection register

GPIO Bus interface

Name	Type	Source/ destination	Description
PRESETn	Input	Reset controller	Bus reset signal, active LOW.
PADDR [18:2]	Input	APB	Subset of APB address bus.
PCLK	Input	APB	APB clock, used to time all bus transfers.
PENABLE	Input	APB	APB enable signal. **PENABLE** is asserted HIGH for one cycle of **PCLK** to enable a bus transfer.
PRDATA [15:0]	Output	APB	Subset of unidirectional APB read data bus.
PSEL	Input	APB	GPIO select signal from decoder. When set to 1 this signal indicates the slave device is selected by the APB bridge, and that a data transfer is required.
PWDATA [15:0]	Input	APB	Subset of unidirectional APB write data bus.
PWRITE	Input	APB	APB transfer direction signal, indicates a write access when HIGH, read access when LOW.

Signals to Pad

Name	Type	Pad type	Description
nGPEN[15:0]	Output	PAD	GPIO output pad enable signal, active low
GPOUT[15:0]	Output	PAD	GPIO output pad data signal driver.
GPIN[15:0]	Input	PAD	GPIO input data from pad. Values on these pins can be read through the APB interface path in software control mode.

Programming

- Application:
- write_word(GPIO_DIRECTION_CNTRL_REG, Value);
- write_word(GPIO_DATA_REG, 0x00FFFFFF);

BSP:

- #define GPIO_DIRECTION_CNTRL_REG (uint32_t*) (GPIO_START + (0 * GPIO_OFFSET))
- #define GPIO_DATA_REG (uint32_t*) (GPIO_START + (1 * GPIO_OFFSET))

- #define GPIO_START 0x00040100 //GPIO Start Address
- #define GPIO_OFFSET 0x08 /*!Generic offset used to access GPIO registers*/

- #define GPIO0 (1 << 0)
- #define GPIO1 (1 << 1)
- #define GPIO2 (1 << 2)
- #define GPIO3 (1 << 3)
- #define GPIO4 (1 << 4)
- #define GPIO5 (1 << 5)
- #define GPIO6 (1 << 6)

GPIO Examples

- On board LEDs
- Ob board Buttons
- Remote Light Control
- Sound Sensing