ASIC PROJECT REPORT

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Design

We worked on the hardware implementation of Advanced Encryption Standard.

Synthesis

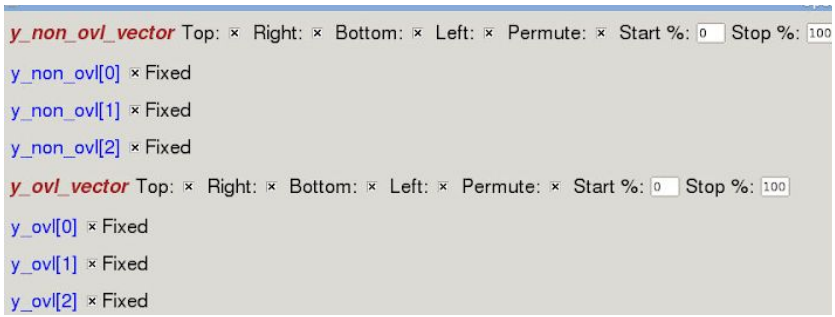
```
=== code ===

Number of wires:                200
Number of wire bits:            242
Number of public wires:         200
Number of public wire bits:     242
Number of memories:               0
Number of memory bits:            0
Number of processes:              0
Number of cells:                240
```

Placement

Inputs

Regarding density, We ended up at 0.7 to avoid placement issues.
We also decreased the aspect ratio to 0.25 to pass DRC.

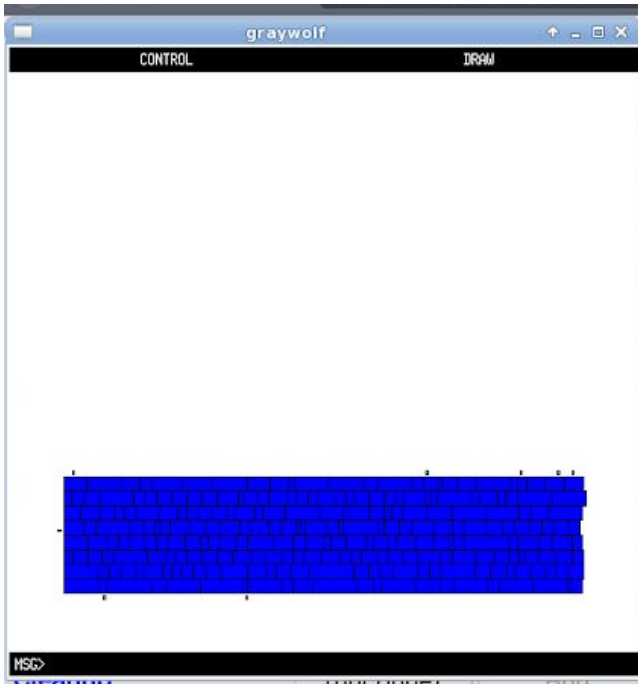
We put a condition to place certain pins in order for convenience.



Results

```
------------------------------
Total stdcells     :247
Total cell width   :2.77e+05
Total cell height  :2.41e+05
Total cell area    :2.70e+08
Total core area    :2.70e+08
Average cell height:9.76e+02
```

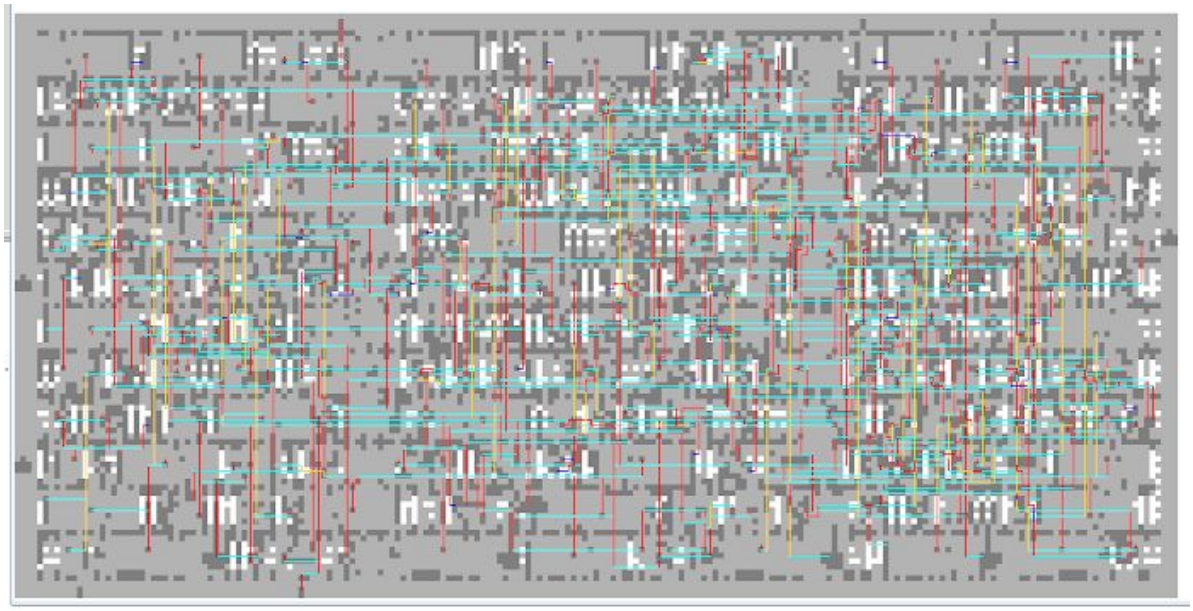
```
Running place2def.tcl
DEF database: 200 units per micron
Limits: xbot = -469.0 ybot = -389.0 xtop = 23401.0 ytop = 11857.0
Core values: 63 0 23373 11712
Offsets: 63 0
4 routing layers
101 horizontal tracks from -366.0 to 11956.0 step 122 (M1, M3, ...)
191 vertical tracks from -378.0 to 23688.0 step 126 (M2, M4, ...)
Summary: Total components = 522
  Fill cells  = 275
  Other cells = 247
Done with place2def.tcl
```



STA

Maximum path delay	2803 ps
Minimum path delay	389 ps
Maximum Frequency	327.804 MHz

Routing



```
Diagnostic: Design name: "code"
  Processed 3 vias total.
  Processed 576 subcell instances total.
  Processed 10 pins total.
  Processed 247 nets total (0 fixed).
  Processed 2 special nets total (4 fixed).
```

With no failed routes.

Post-STA

Maximum path delay	2823.3 ps
Minimum path delay	391.4 ps
Maximum Frequency	325.729 MHz

LVS

We passed clean through LVS. No issues here.

DRC

First, we got an error count of 13. It disappeared when we lowered the aspect ratio to 0.25. But, again we started to get an error count of 6 when we decided to put a condition on pin placement.

Comments

Considering the above design with relatively fewer cells and with DRC errors, we tried other designs like RISC-16 and DNA sequence alignment accelerator, many of them were getting synthesised in cloudV, but openGalaxy was throwing some errors like “D-latch not found”.