Design of Handshake Based Pulse Synchronizer

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I. Abstract

A modern SoC has multiple clock domains. If these different clock domains are not properly synchronized, metastability events are bound to happen and may result in inappropriate behavior of the SoC. A Synchronizer help us to mitigate/reduce the effect of metastability. A synchronizer is a digital circuit that converts signal from a different clock domain into the recipient clock domain so that it can be captured without introducing any metastability failure. There are different types of synchronizers used in various situations such as:

- Flip-flop based synchronizer (Two flip-flop synchronizer)
- Handshaking based synchronizers
- Mux based synchronizers
- Two clock FIFO synchronizer

This paper presents the design of a handshake based pulse synchronizer that is used to synchronize a pulse generated in source clock domain to destination clock domain. A pulse cannot be synchronized directly using 2 Flip Flop synchronizer, while synchronizing from fast clock domain to slow clock domain using 2 Flip Flop synchronizer, the pulse can be skipped which can cause the loss of pulse detection & hence subsequent circuit which depends upon it, may not function properly. In handshake based pulse synchronizer, synchronization of a pulse generated into source clock domain is guaranteed into destination clock domain by providing an acknowledgement. This method of providing an acknowledgement overcomes the drawback of pulse synchronizer.

II. Circuit Details

The circuit is divided into two namely, digital and analog part which cumulatively makes up the mixed signal circuit. The digital part is composed of a set of flip flops clocked at different frequencies, a set of 2:1 MUX, a NOT gate and an OR gate. The analog portion is comprised of AND gate implemented using CMOS logic. The AND gate is implemented using a NAND gate followed by a NOT gate. Both NAND and NOT gate have been implemented using nfet and pfet available in the SKY130 PDK. The pulse signal in clock domain A cannot be directly passed to clock domain B, so we first convert the pulse to a level signal. This method ensures that pulse signal is passed from fast clock domain to a slower clock domain without any error. On the other side, we use an AND gate to recreate the pulse signal in another clock domain.
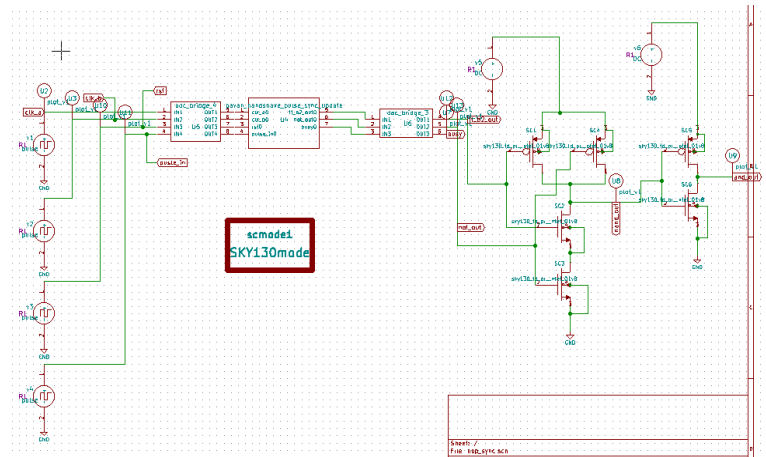
III. Implemented Circuit

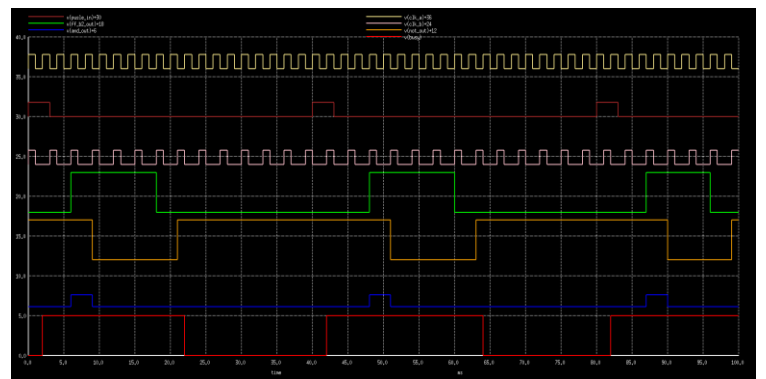Fig. 1. Handshake Based Pulse Synchronizer Circuit

IV. Observed Waveform

Fig. 2. Timing Diagram for Handshake Based Pulse Synchronizer

REFERENCES

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