4 Bit Ring Counter using D Flip Flop

Jagarlamudi PavanKalyan

Department of ECE_NRI Institute of Technology.

pavanjagarlamudi6@gmail.com, 1 August 2022

Abstract ---This paper presents the design of a 4 bit ring counter using D flip flop where it uses the output of the last flip flop which is given as input to the starting flip flop, which can encode and decode the logics. In digital electronics most of the electronic devices work on counters designed by group of flip flops with different mode of modules represented by states of cycles. Here we are looking up with a synchronous counter which operations based on the Single input clock signal to all flops.

1. Design Description

Ring counter is known as circular shift register which is used to control the sequence operation of digital system by using the timing signals. Also known as straight ring counter which circulates a single one or zero bit around the ring. Clock pulse is applicable to all the flip flops simultaneously where the propagation delays of a ring counter which is nearly constant to number of bits in the code. In hardware implementations where registers are more expensive than combinational logic, this ring counter can represent N states, where is the number of bits in the code. In this counter output of each stage is connected to the input of successive stage. The output of the last flip flop is connected as data input to the first flip flop as shown in the circuit diagram clearly.

2. Working Principle

Initially, at any given point of time, only one flip flop is set and the remaining flip flops are cleared i.e: 0001. After the first clock Pulse. 1 is shifted to second flip flop and the counter output is 0010. This counting continues till the counter counts 1000 at 4th clock pulse.

Clock	Q4	Q3	Q2	Sequence Q1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	1	0	0
4	1	0	0	0

Table: Counting Sequence of Ring Counter

In this counter, the numbers of possible states are “n”. That means he number of states is equal to the number of flip flops used.

3. Circuit Design

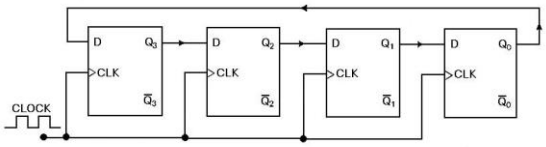


Figure 2: Flip flop based Design.

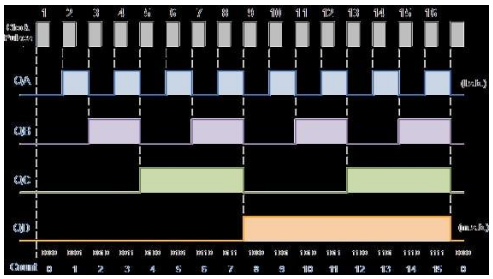
4. Initial Coding

```
module DFlipFlop
(
  input wire    reset_n,
  input wire    clk,
  input wire    d,
  output wire   q,
  output wire   q_n
);

  wire w1, w2, w3, w4, w5, w6;

  //master
  nand na1(w1, d, ~clk);
  nand na2(w2, ~clk, ~d);
  nand na3(w3, w1, w4);
  nand na4(w4, w3, w2);

  //slave
  nand na5(w5, w3, clk);
  nand na6(w6, clk, ~w3);
  nand na7(q, reset_n, w5, q_n);
  nand na8(q_n, q, w6);endmodule
```

Test Bench

```
  DFlipFlop ff2(reset_n, q[1], qn2, q[2], qn2);
  DFlipFlop ff3(reset_n, q[2], qn3, q[3], qn3);

endmodule
```

5 Output Waveform



6 References:

1. Electronic Devices and Circuits by Salivahanan, Suresh Kumar, (Third Edition), M.C. Graw Hill Education.
2. Switching Theory and Logic design (STLD) by, Sia publications.
3. https://www.elprocus.com/ring-counter-in-process/
4. Electronic Devices and Circuit Theory by Robert L Boylestad, Louis Nashelsky, Pearson Tenth Edition.