Pavan B G

Electronics & Communication Engineering

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SUMMARY

Pre-final year Electronics and Communication Engineering student with a strong foundation in semiconductor fundamentals, device physics, and MOSFET operation. Strong interest in VLSI design and a motivated approach to learning chip design concepts, digital circuits, and semiconductor technology. Actively building the knowledge and skills needed to pursue a career in VLSI and contribute to semiconductor innovation.

EDUCATION:

Acharya Institute of Engineering, Bengaluru, India

Bachelor of Engineering, **Electronics and Communication Engineering** (CGPA-8.7) **(Ongoing) 2025**

Vidyanidhi IND PU College Tumakuru PCMB (93.33%) **2023**

Shubhodaya High School Gubbi SSLC (96.16%) **2021**

CERTIFICATIONS & ACHIEVEMENTS:

Certified Professional in RTL Design, **HCL GUVI**
Certified Professional in Verification, **HCL GUVI**
Digital Electronics – **Udemy**
Arduino & Microcontroller development – **Udemy**

PROJECTS:

Analysis and RTL Design of Lossless Image Compression Algorithms for Medical Applications — Link
- Designed Verilog-based architectures for DPCM, RLE, and Huffman Coding to achieve lossless image compression.
- Performed area, power, and delay analysis in Vivado to evaluate hardware efficiency.
- Verified compression accuracy and image reconstruction using MATLAB.

RTL Design and Verification of a RISC Processor — Link
- Designed and implemented a 5-stage pipeline RISC processor in Verilog.
- Verified functionality using Verilog testbenches, performed synthesis and implementation on Xilinx.

SRAM Bit-Cell Modeling (6T/8T) – Transistor-Level Simulation
- Modeled 6T/8T SRAM cells using LTspice with NMOS/PMOS transistor-level circuits.
- Simulated read, write, and hold operations to analyze bit-cell behavior.
- Evaluated stability and noise margins to understand memory reliability.

SKILLS:

- **RTL & VLSI:** Verilog RTL, Digital IC Design, FSM, Logic Synthesis, STA, Functional Verification, CMOS, MOSFET Characteristics, VLSI Design Flow
- **Tools:** Xilinx Vivado, cadence,LTspice, GTKWave, EDA Playground
- **Programming:** Python, TCL, SystemVerilog
- **Soft Skills:** Problem Solving, Communication, Teamwork

DECLARATION

I hereby declare that the information provided in this resume is true and accurate to the best of my knowledge.