**Assignment 3: Exploring Memory Hierarchy Design in gem5**

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MSCS-531-A01: Computer Architecture and Design

Professor. Vanessa Cooper

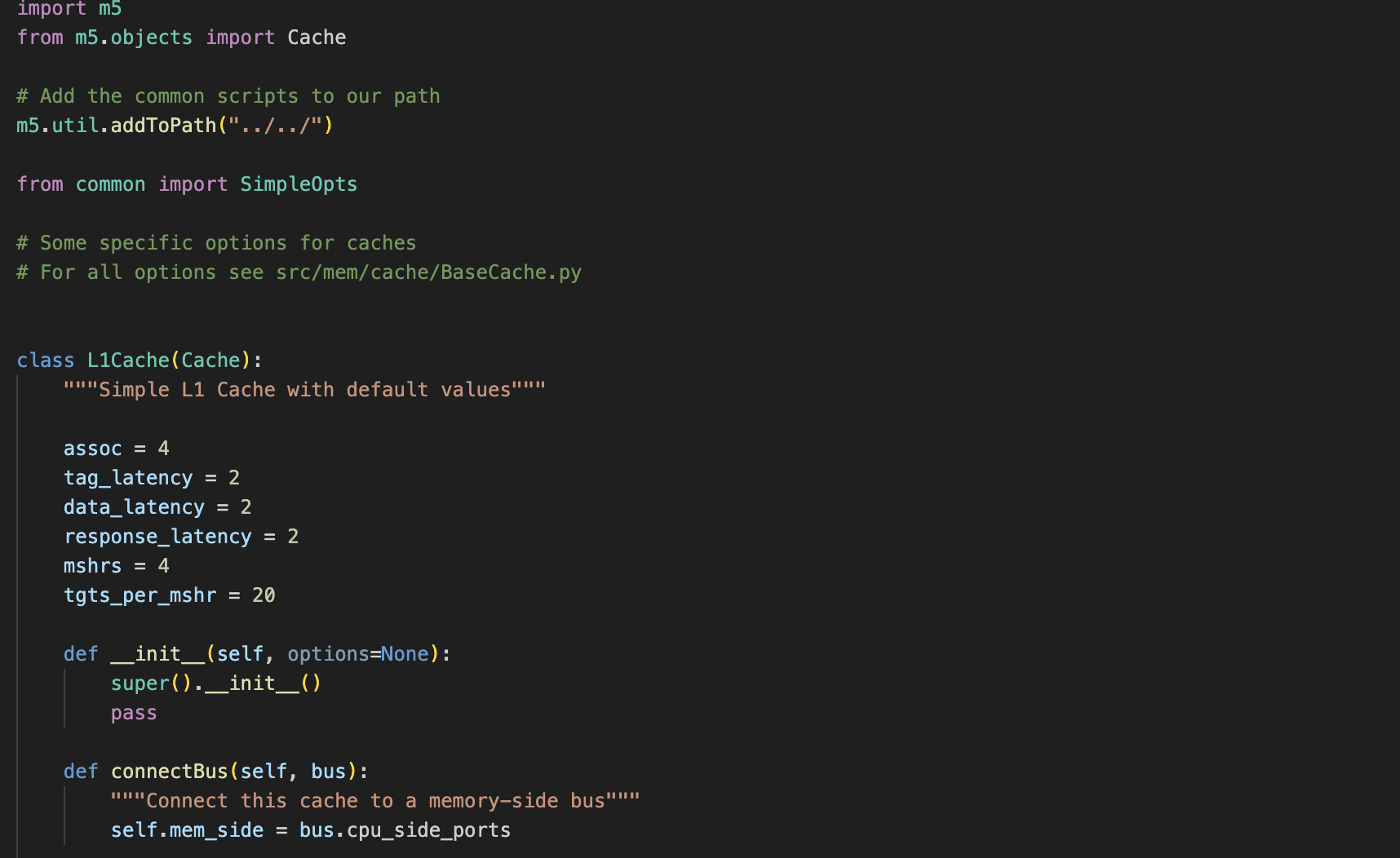
Date: 9/13/2025

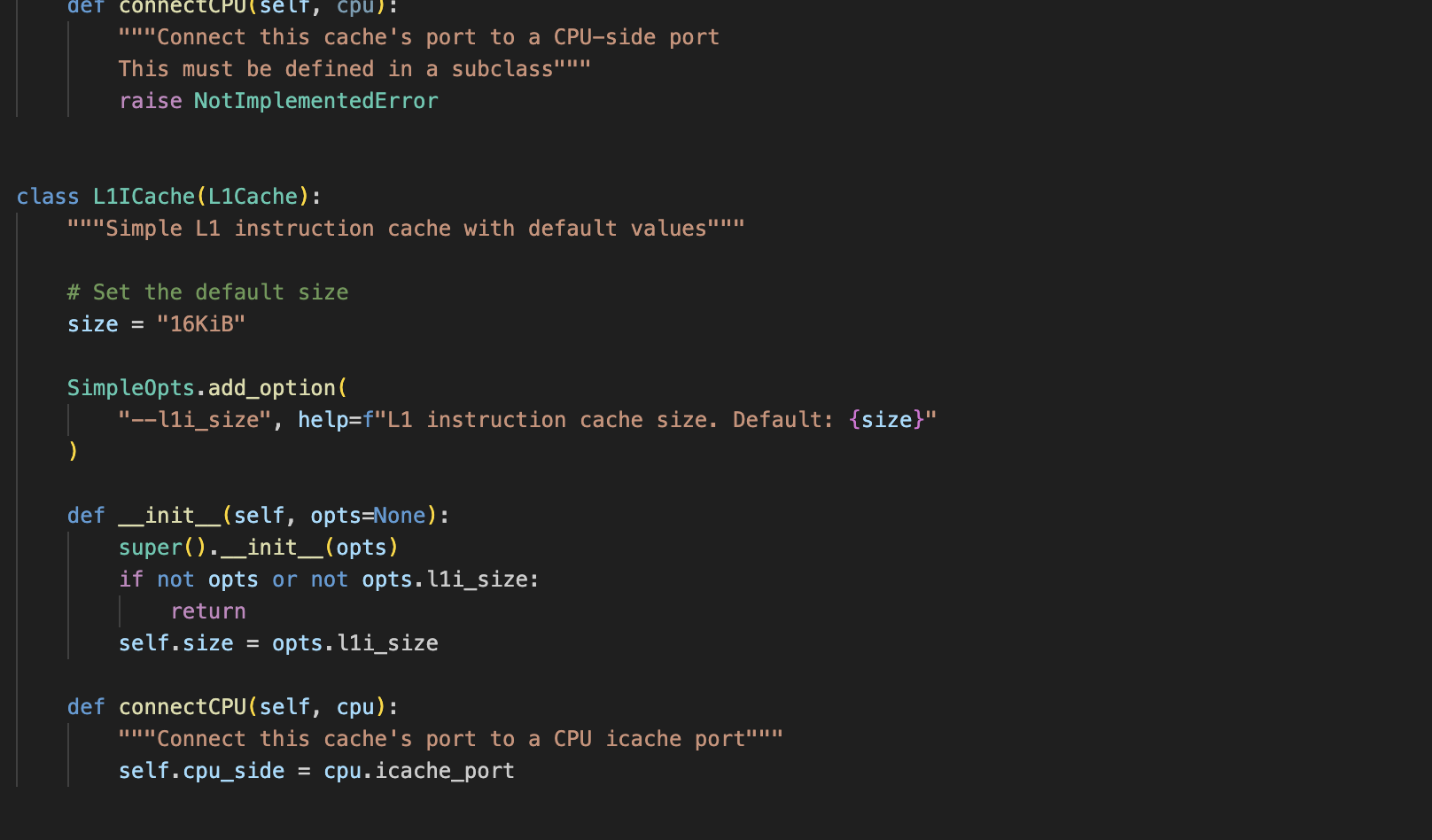
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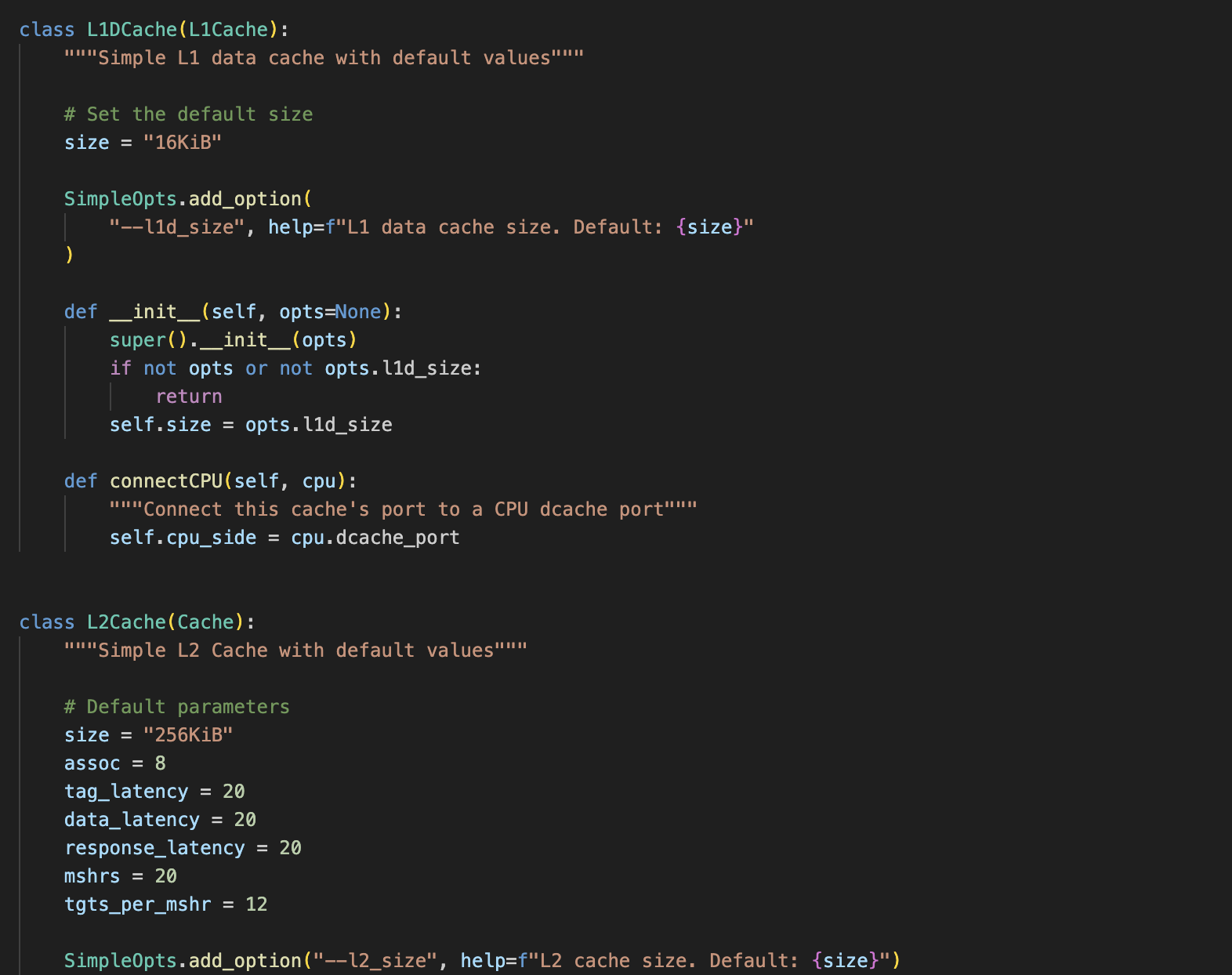
**Configuration files**

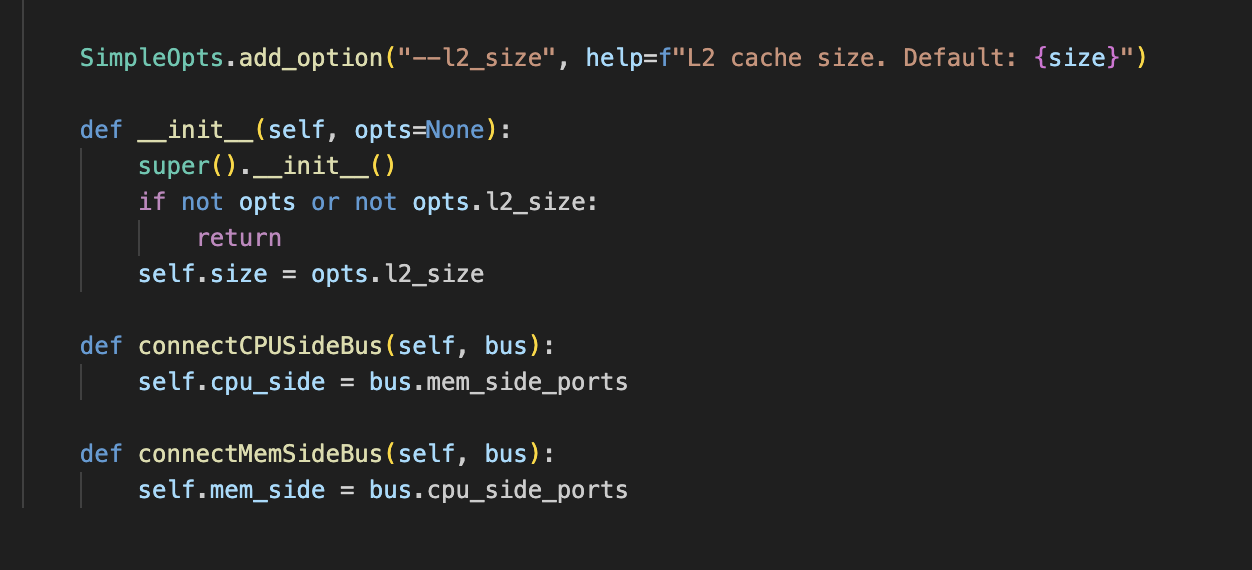
**Cache.py:**

**Used to change the cache values using command line aruguments**



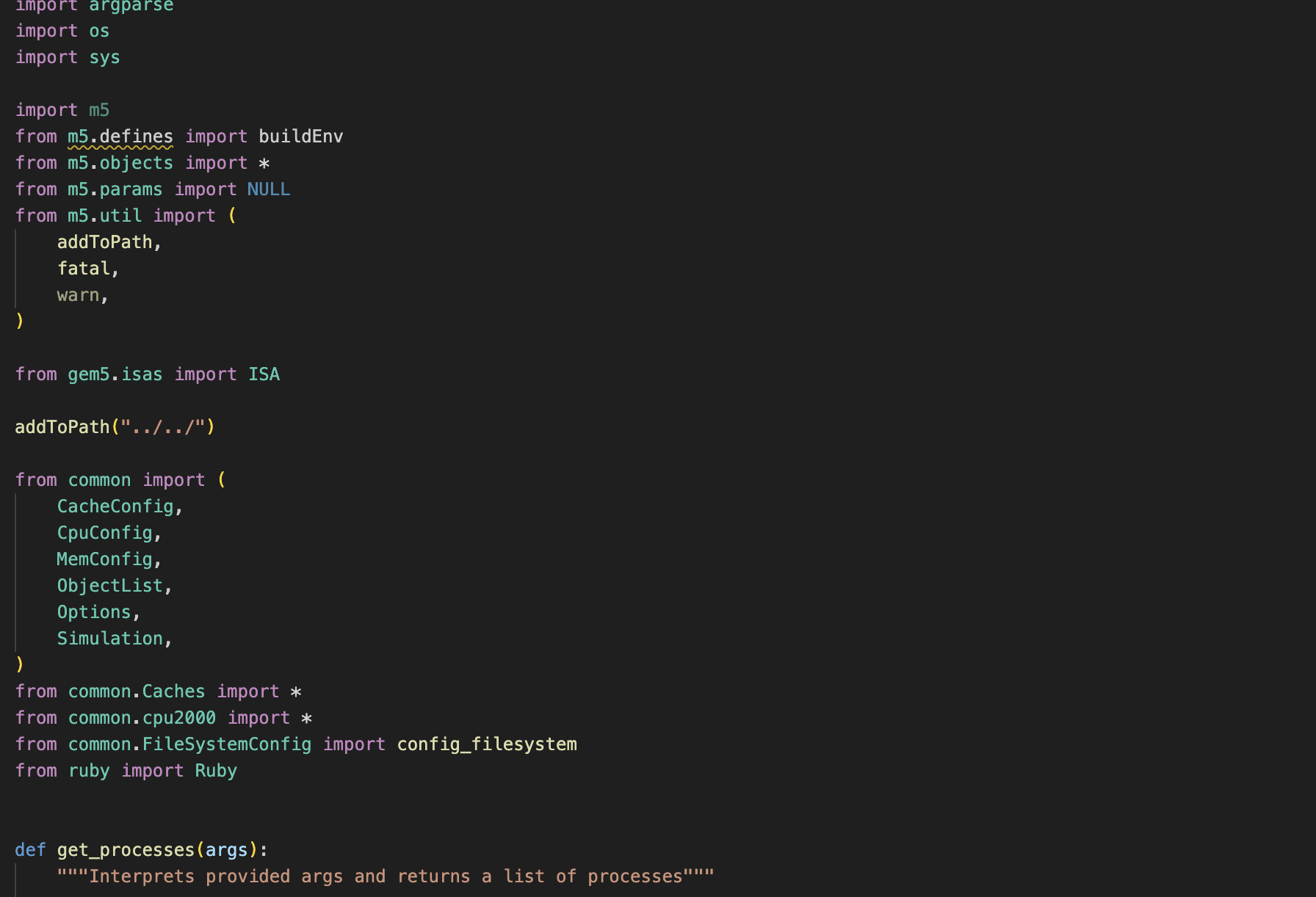


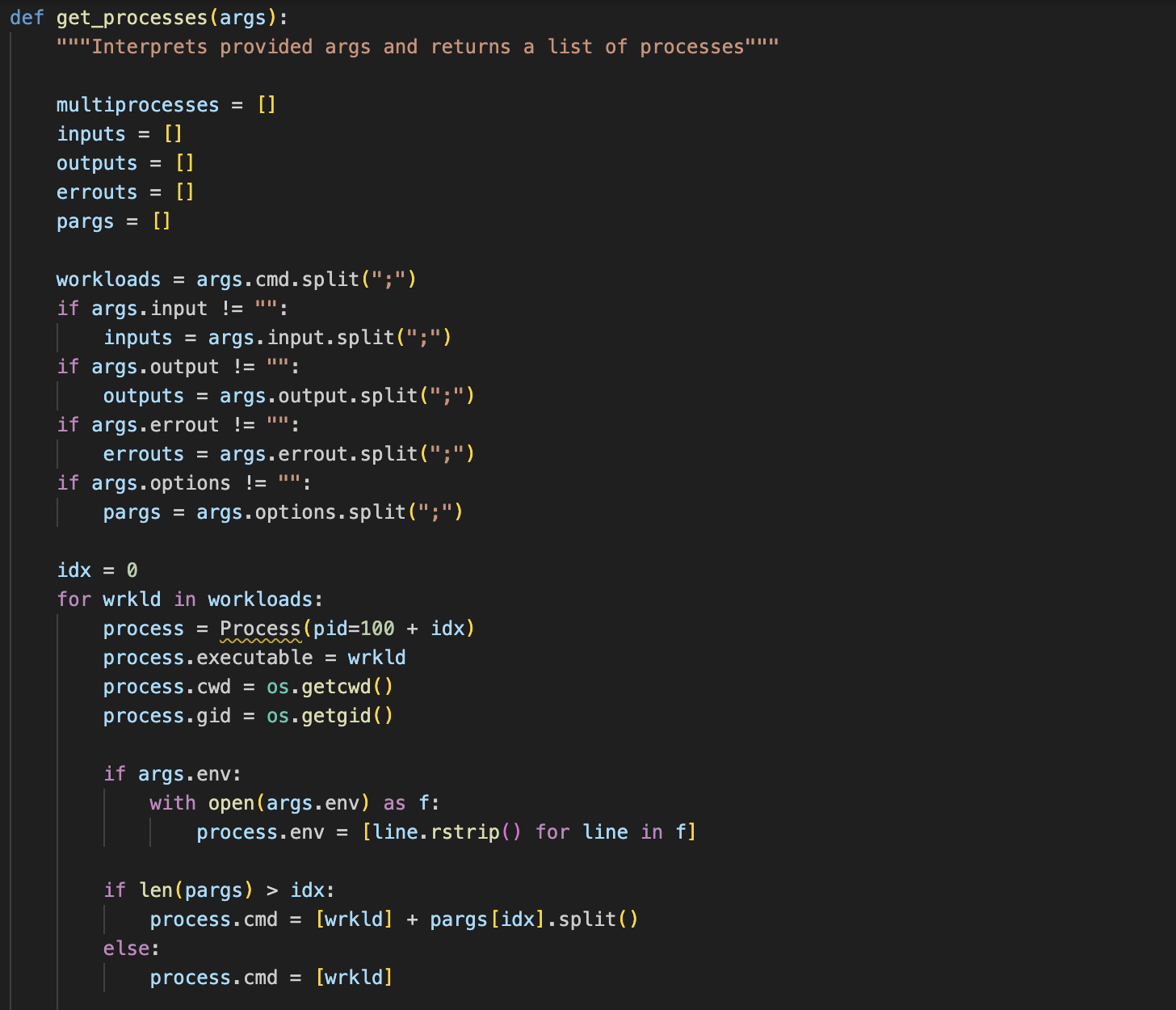


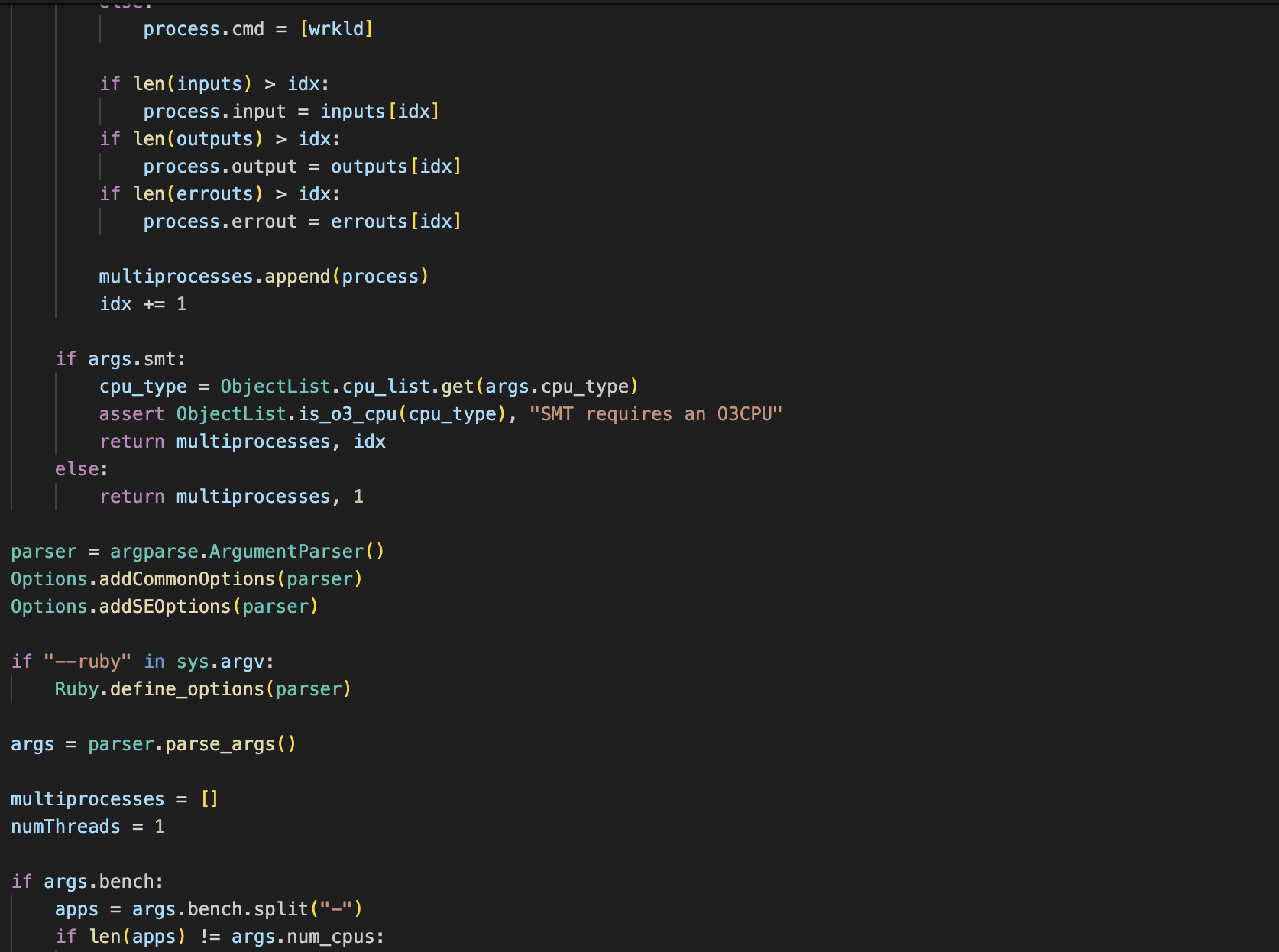


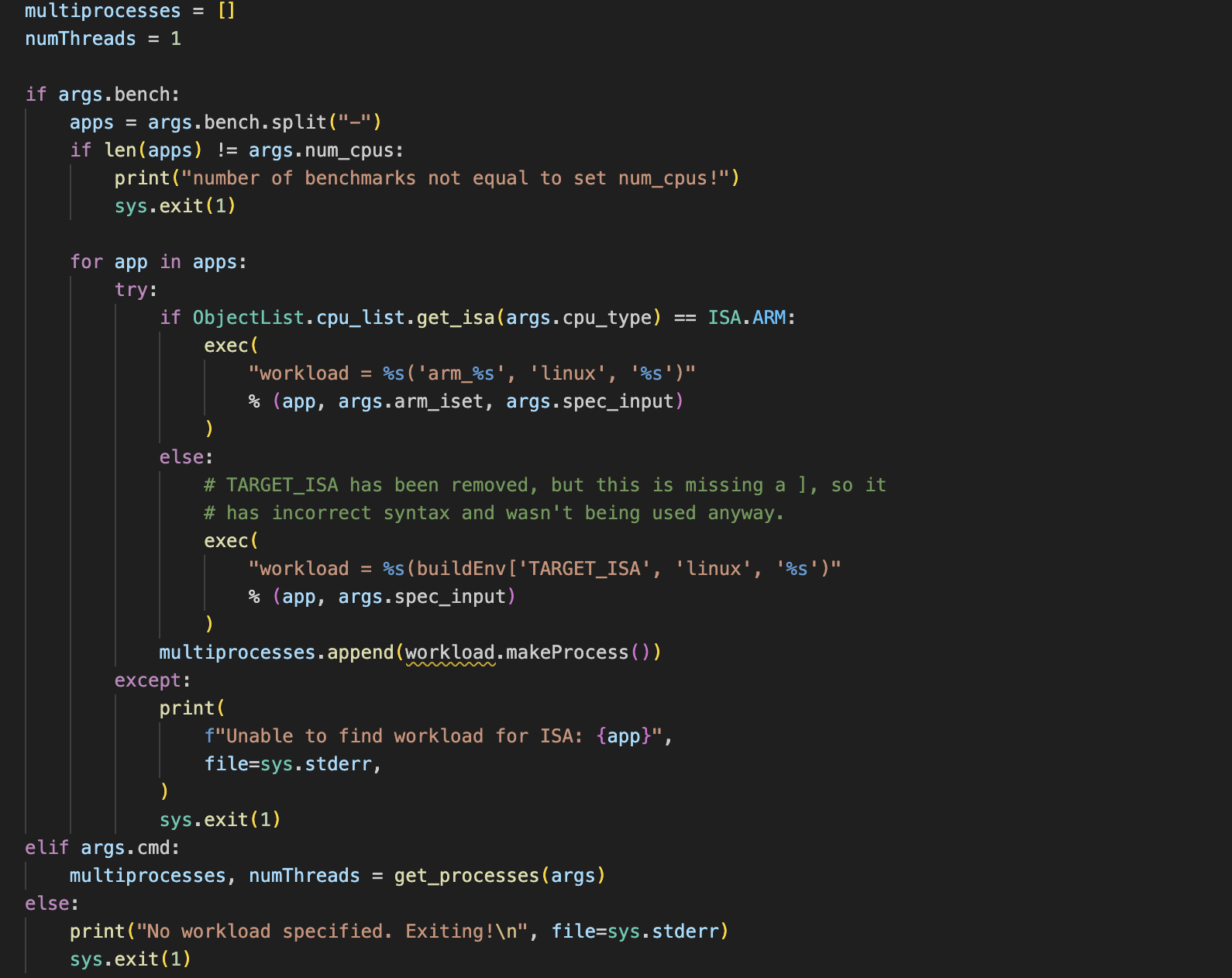
**Se.py**

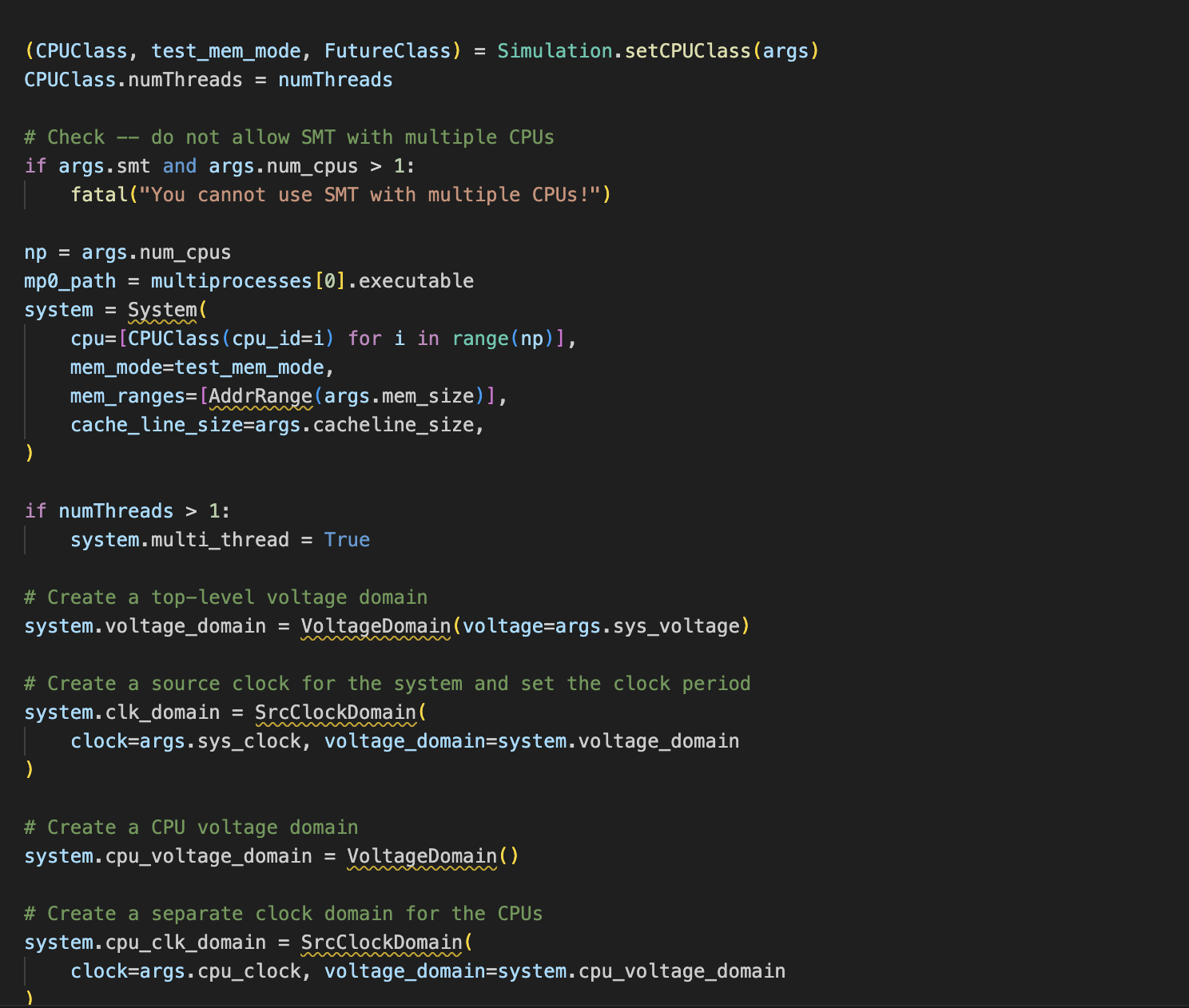
**Used this file to give input values for cache sizes and associative values**

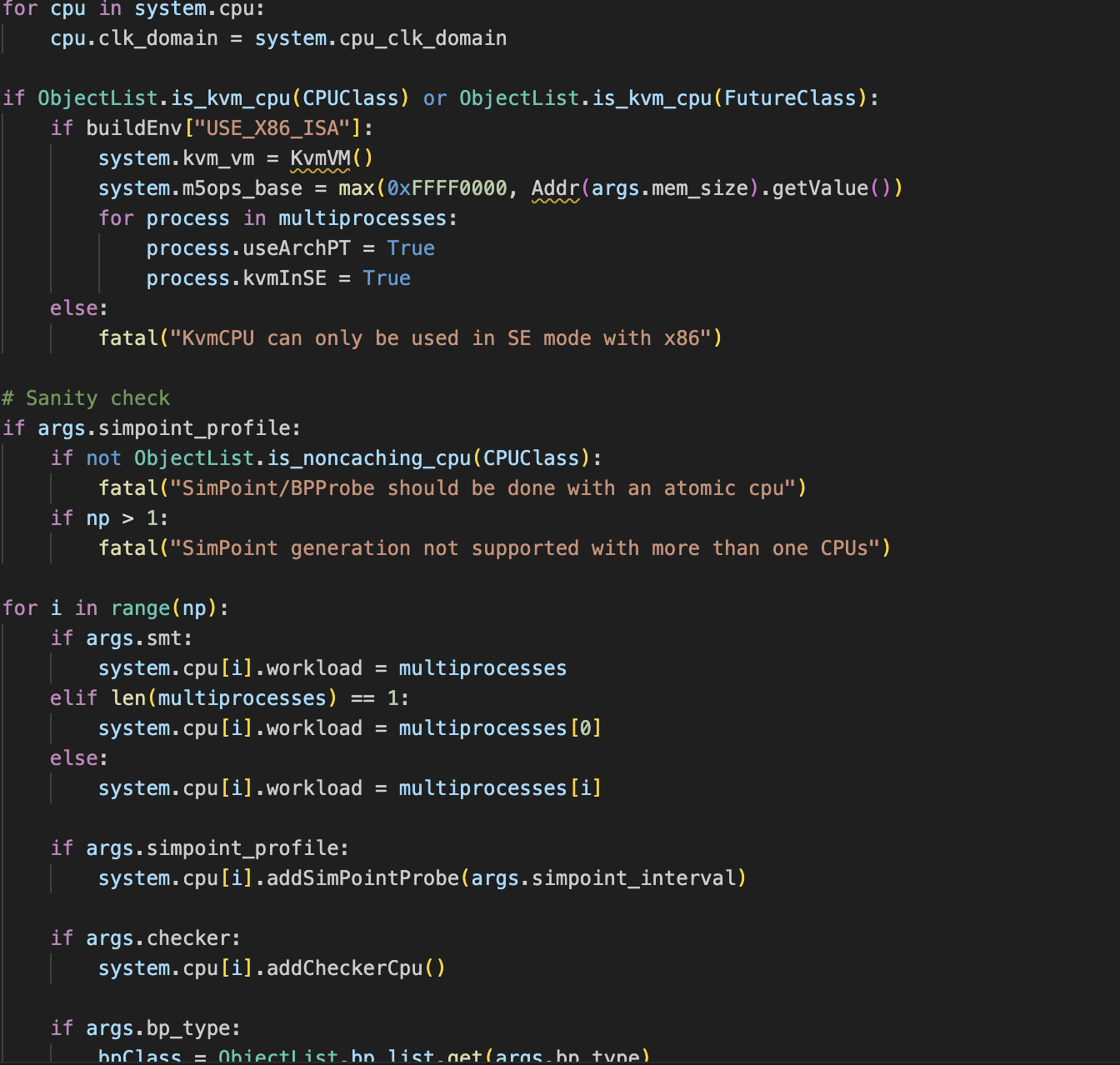
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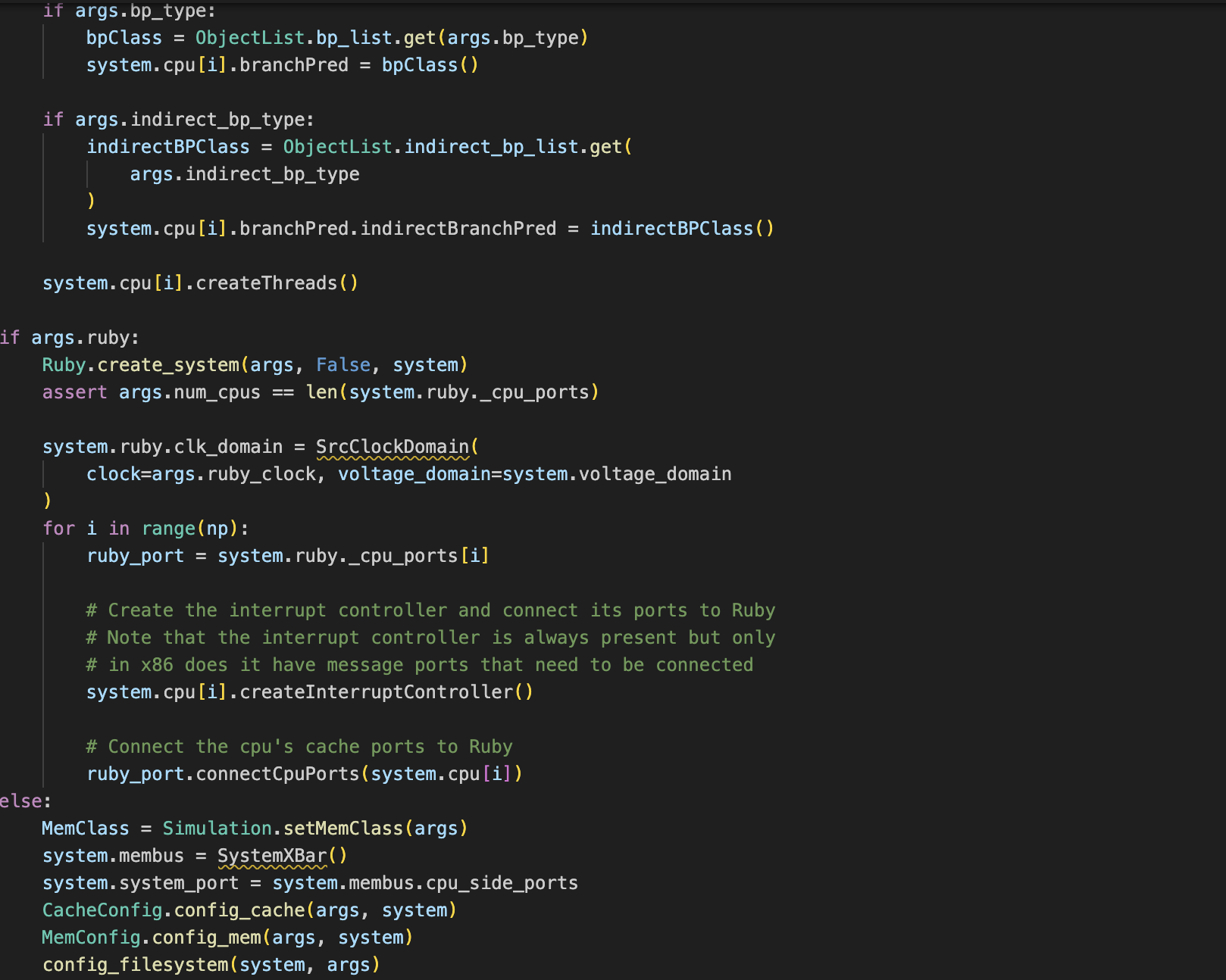
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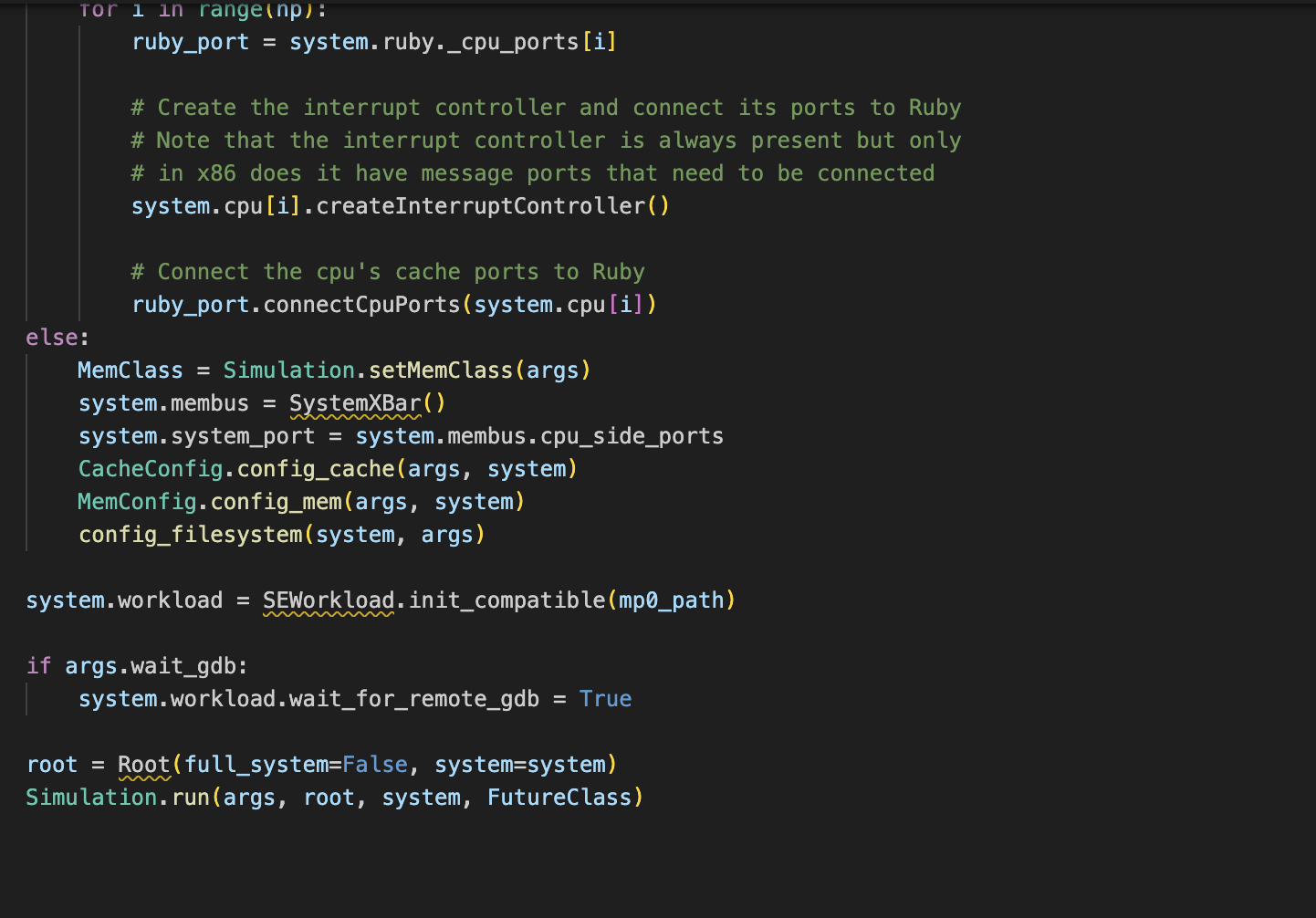
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