ARM-Embedded-Path

CMSIS-Basics

Pavel Pys

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Overview

- Introduction
- ARM-Architecture

Introduction
What is the target of this journey?

In these slides, I want to document my learning progress in handling ARM microcontrollers, in my case from the company ST-Microelectronics. Ultimately, this slide set should become a reference work. - Hanover 21.10.2025

Introduction
What is the ARM architecture?

- A microprocessor architecture developed by the British computer company Acorn in 1983. Initially, ARM stood for Acorn RISC Machine, and was later changed to Advanced RISC Machines.
- The company does not manufacture the chips itself, but instead grants different licenses to semiconductor development companies, which then manufacture based on this architecture.

Introduction
What is the ARM architecture?

Today, many renowned chip manufacturers build their chips on the ARM architecture.

Notable manufacturers:

- Apple
- Qualcomm Inc.
- Samsung Electronics
- Huawei Technologies Co. Ltd.
- ST-Microelectronics
- ...

Introduction
Market share of ARM chips

The market share of ARM-based chips is very large, but depends on the system. In mobile phones, it was already about 98% in 2005 (at least one ARM processor).

In data and server centers, ARM is currently growing rapidly, though its goal of reaching 50% market share by the end of 2025 is considered ambitious by some analysts.

Introduction
What are the advantages of ARM?

The ARM architecture offers several advantages:

- ARM uses the RISC principle.
- ARM cores are small and can be easily combined.
- Low costs and licensing flexibility.
- Large ecosystem.
- High performance per watt (efficiency).
- Good security features.
- Wide range of applications.

ARM
What is a Microcontroller Architecture?

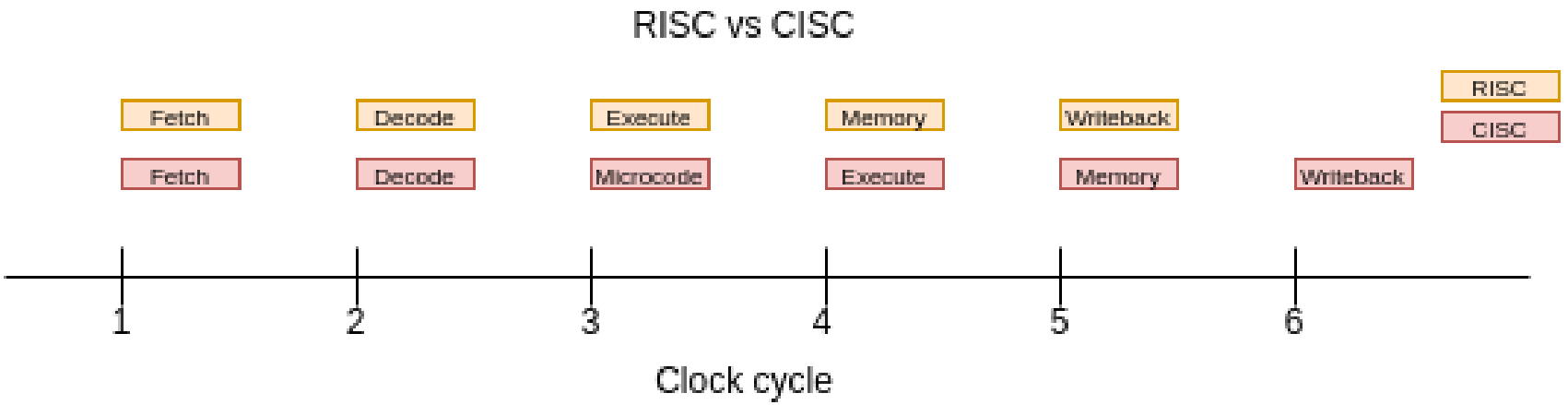
A microcontroller architecture describes the internal structure and functionality of a microcontroller – meaning how the individual components on the chip are interconnected and how they work together.

The architecture consists of: CPU, memory, bus system, peripherals, clock source, and power supply as well as reset logic.

ARM
What is a Microcontroller Architecture?

In summary: A microcontroller architecture is the blueprint of how CPU, memory, peripherals, buses, and clock sources work together on a single chip to execute tasks efficiently.

ARM
RISC vs CISC



The graphic shows the pipelines of RISC and CISC. RISC processes instructions in parallel (one new instruction per clock cycle), while CISC processes longer and more complex instructions sequentially.

ARM
Architecture Structure

Register-based design (e.g., 16-32 registers) with a pipeline architecture for parallel instruction execution.

Harvard or Von Neumann structure depending on the type.

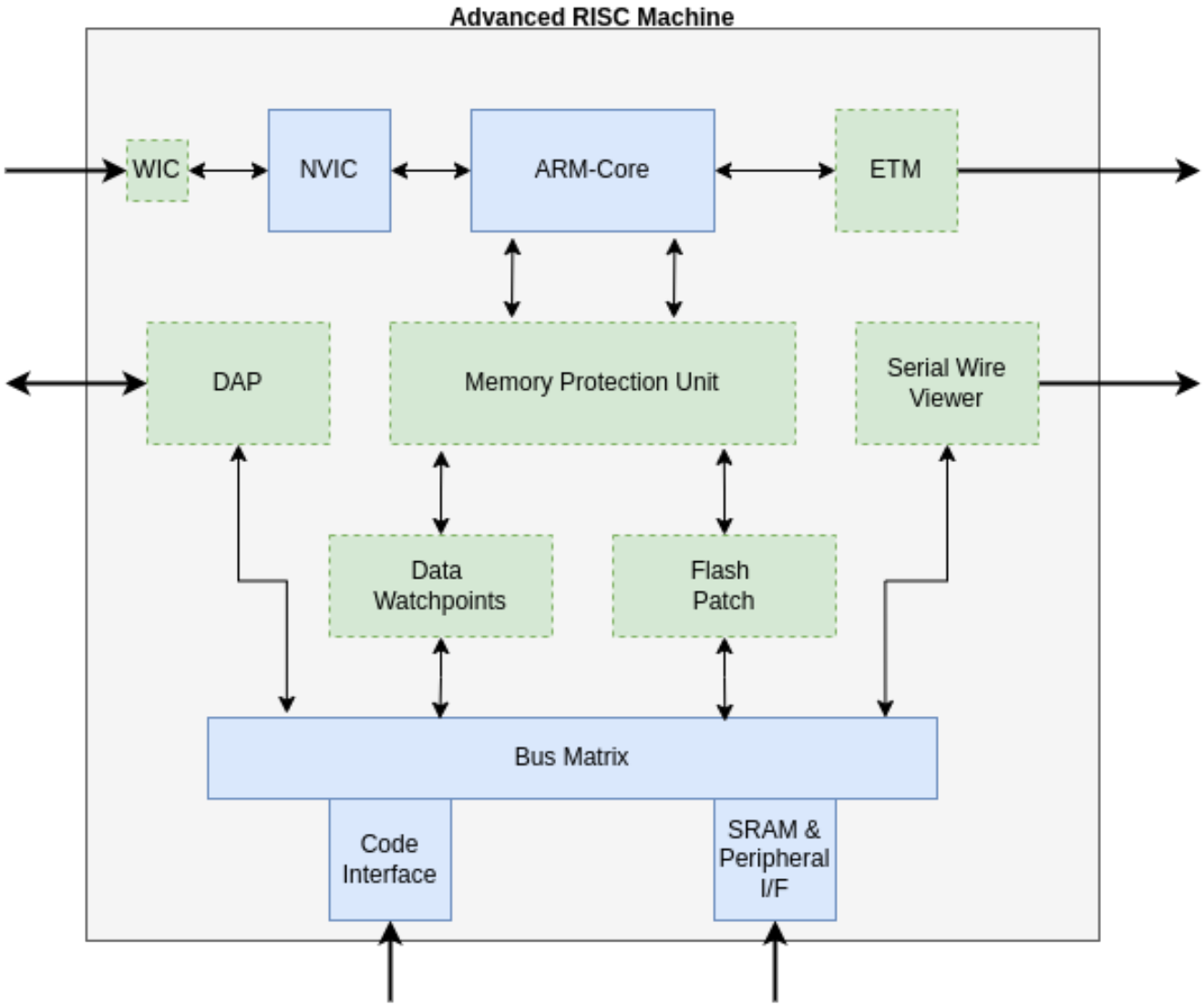
Components:

- ALU (Arithmetic Logic Unit)
- Register set (R0-R15)
- Program Counter, Stack Pointer
- Interrupt Controller
- Bus interfaces (AHB, APB...)

ARM
Architecture Structure

Cortex-M microcontrollers typically implement a modified Harvard architecture, where instruction and data buses are separate internally, but share a unified memory space.

ARM
ARM - Cortex M Block-Diagram



ARM
WIC - Wake-up Interrupt Controller

In deep sleep (core clock and NVIC logic powered down), the WIC acts as a shadow interrupt latch, allowing selected IRQs to wake the system.

Control of WIC behavior through:

- NVIC->ISER (enable/disable interrupts)
- NVIC priorities and BASEPRI/PRIMASK (only unmasked and sufficiently prioritized IRQs can wake the system)
- Sleep depth via SCB->SCR.SLEEPDEEP (Deep Sleep vs. normal Sleep)
- WFI/WFE (how you enter sleep)
- Peripheral wake sources (EXTI edge, RTC alarm, USART-RX, I^2C address match, etc.)

NVIC is tightly coupled to the Cortex-M core through the System Control Block (SCB), forming the Exception Model

ARM
NVIC - Nested Vector Interrupt Controller

The Nested Vector Interrupt Controller (NVIC) is the hardware block in the ARM Cortex-M core that:

- Accepts, prioritizes, nests, and forwards interrupts (IRQs) to the CPU,
- Can mask, enable, set/clear pending interrupts,
- Integrates exception handling (Reset, NMI, HardFault, SysTick, etc.) using the same mechanisms.

It is directly integrated into the core, not in the periphery, and coupled with the System Control Block (SCB).

ARM
ARM Core

The ARM core is the actual processing core (CPU core) in the microcontroller - meaning the logical unit that executes code, performs arithmetic operations, processes interrupts, and communicates with memory and peripherals via buses.

In this case (STM32F103), this is an ARM Cortex-M3, based on the ARMv7-M architecture.
This means:

- 32-bit RISC processor
- Harvard architecture (separate buses for code and data)
- Pipeline design
- Thumb-2 instruction set (compact mix of 16- and 32-bit instructions)

ARM
ARM Core: Architectural Features

Harvard Architecture:
Separate buses for code (I-Bus) and data (D-Bus) $\rightarrow$ enables parallel reading of instructions and data

Thumb-2 Instruction Set:
Mix of 16- and 32-bit instructions $\rightarrow$ compact code with full functionality

NVIC Integration:
Interrupt handling directly in the core $\rightarrow$ no external interrupt controllers needed

Sleep and Deep Sleep Modes:
Power saving functions via WFI/WFE instructions

ARM
ARM Core: Architectural Features

Harvard Concept in Action:

- Instructions are fetched via the I-Bus from Flash memory
- Data (variables, peripheral registers) via the D-Bus
- System and debug accesses (DMA, DAP, Trace) via the S-Bus

This allows the Cortex-M3 to simultaneously read an instruction and access data.

ARM
ARM Core: Conclusion

The ARM Cortex-M3 core is a 32-bit RISC processor with:

- Efficient pipeline design,
- Integrated interrupt controller,
- Memory protection (MPU),
- Integrated debug/trace architecture (CoreSight),
- And ideal for deterministic real-time and embedded applications (e.g., in your STM32F103).

It is the heart of the microcontroller - all other components (Flash, SRAM, Timer, UART, etc.) are built around it as peripherals.

ARM
DAP - Debug Access Port

The DAP (Debug Access Port) is the interface between your debugger (e.g., ST-Link, J-Link) and the internal debug and trace units of your ARM core.

The DAP acts as the ”debug router” between the external world and the CoreSight internals.

The DAP consists of an AP (Access Port) and DP (Debug Port) interface – e.g. SW-DP for SWD or JTAG-DP for JTAG.

ARM
MPU - Memory Protection Unit

The MPU (Memory Protection Unit) is a hardware unit in the ARM core that divides memory into regions and monitors access rights (read/write/execute) for each region.

It prevents your code from accidentally writing to ”forbidden” areas or executing from unauthorized memory.

It is thus a mini memory protection system, similar to an MMU (Memory Management Unit) in a PC - but simpler and without virtual addresses.