1.create a new Verilog source file named “adder 2bit.v” with the module named “adder 2bit”. You can use your full adder module created in lab6

module adder_2bit(Carry, Sum, A, B); // 2-bit adder module with inputs A, B and

outputs Sum, Carry

input wire [1:0] A, B; // 2-bit input wires A and B

output wire [1:0] Sum; // 2-bit output for Sum

output wire Carry; // Output Carry

wire Cinter; // Intermediate carry wire

// Instantiate first full adder

Full_adder add1(Sum[0], Cinter, A[0], B[0], 1'b0); // Add least significant bits

// Instantiate second full adder

Full_adder add2(Sum[1], Carry, A[1], B[1], Cinter); // Add most significant bits

endmodule

2. If the circuit in Figure 7 utilizes the 2-bit carry ripple adder designed in Lab 3, what would be the maximum clock rate f given that each gate delay is 4ns? You can refer to your post-lab deliverable answer

Critical Path Delay = adder delay + clock to q of sum

Clock To Q to Carry = 2*4+1*4+1*4=16ns.

1/16ns = **62.5MHz**

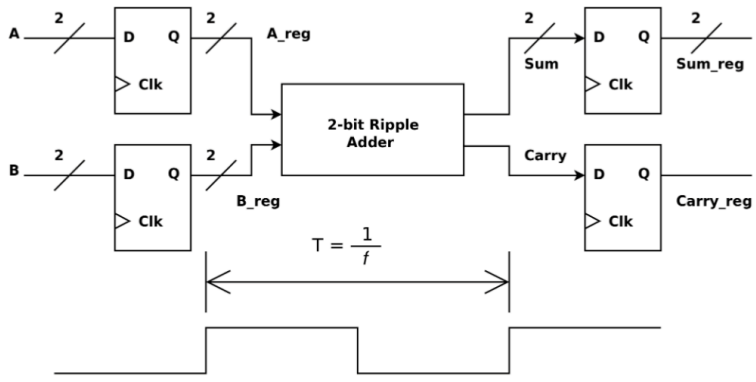

Figure 7: Example Synchronous Logic Circuit

3. compare all the three memory components discussed in the background part in the same table. Ex- plain their differences and improvement

Latches and flip-flops are sequential logic elements used for storing data. Latches, like the SRlatch and D latch, respond immediately to input changes, while flip-flops, such as the D flip-flop, are edge-triggered and synchronized to a clock signal. Latches are common in asynchronous circuits, while flip-flops are preferred in synchronous circuits due to their precise timing control. In simulations, latches may reflect input changes instantly, while flip-flops hold their output until the next clock edge. Master-Slave D flip-flops can be constructed using two D latches, offering both rising and falling edge sensitivity. Understanding these differences is essential for designing effective digital systems.