ECEN 248 - Lab Report

Lab Number: 3

Lab Title: Rudimentary Adder Circuits

Section Number: 510

Student’s Name: Paola Avila

Student’s UIN: 731007033

Date: 02/15/2025

Objective

The primary objective of this lab is to gain a comprehensive understanding of adder design and functionality. This includes the observation and analysis of ripple carry adders, full adders, and half adders. By constructing these adders using integrated circuits (ICs), we will examine their outputs, specifically the sum (S) and carry-out (Cout) values. Through this process, we aim to develop a deeper insight into the operational principles and practical implementation of digital adders in computational circuits.

Design :

In this lab, we will systematically construct and analyze different adder circuits, beginning with the setup of a stable DC power supply. Before powering the circuit, we will ensure all necessary connections are properly made. The red lead will be connected to the power rail on the breadboard, while the black lead will be attached to the ground rail. Once the power supply is secured, we will proceed with assembling the circuit components for the half-adder, full-adder, and ripple carry adder.

Half-Adder Design

To construct a half-adder, we will utilize an XOR gate and an AND gate. Both gates will be correctly wired to power and ground to ensure functionality. The two input signals, A and B, will be supplied to both gates. The XOR gate will generate the sum output (S), while the AND gate will produce the carry-out output (Cout). To enhance the clarity of the output observation, we may connect LEDs to each output, ensuring the long lead (anode) is connected to the output and the short lead (cathode) is connected to ground.

Full-Adder Design

Building upon the half-adder, the full-adder circuit will incorporate an XOR gate, an AND gate, and an OR gate to accommodate a carry-in (Cin) input. The XOR gate will first process inputs A and B, generating an intermediate sum. This intermediate sum will then be XORed with Cin to produce the final sum output (S).

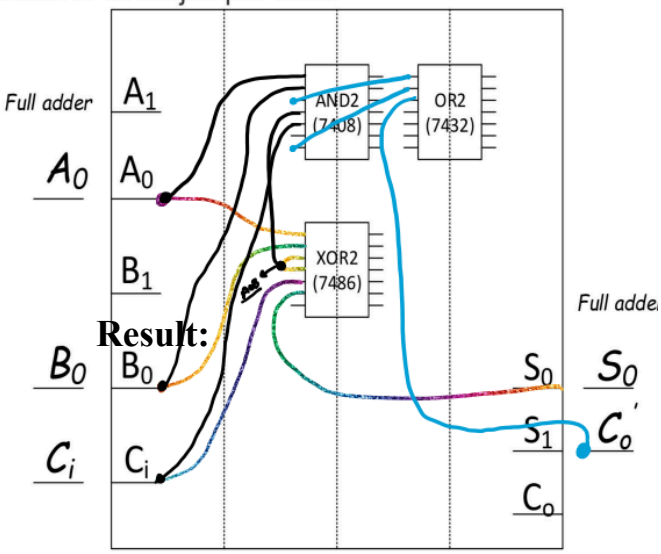
To determine the carry-out (Cout), the output of the XOR operation between A and B will be used as an input to an AND gate, alongside Cin. Additionally, the original inputs A and B will be fed into a separate AND gate. The outputs from both AND gates will then be processed through an OR gate, and the resulting output from this OR gate will represent the Cout of the full-adder.

Ripple Carry Adder Design

To construct a ripple carry adder, multiple full adders will be cascaded together. The Cout from the first full-adder will serve as the Cin for the next full-adder stage. This process will be repeated to allow the carry to propagate through successive stages, enabling multi-bit binary addition. By implementing this design, we will observe the working principles of different adder circuits and analyze their outputs.

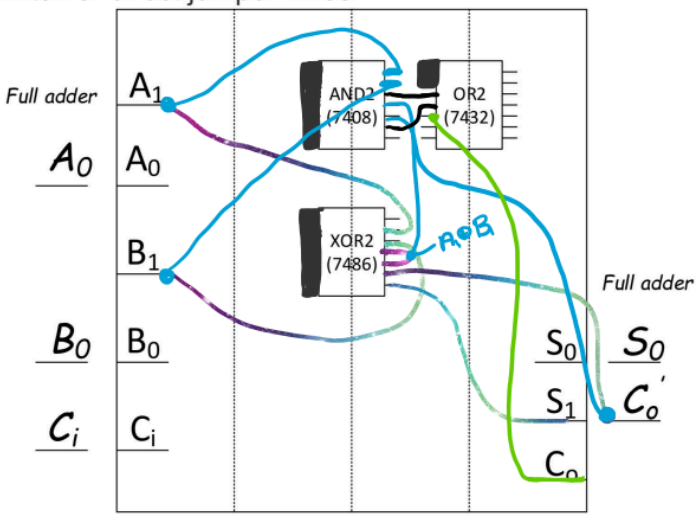
By following this structured design approach, we will gain practical insight into the behavior of combinational circuits, particularly in the context of arithmetic operations within digital systems. The observations from this lab will reinforce theoretical concepts and enhance our understanding of adder implementations using integrated circuits (ICs).

step3: Define your input pins $A_1\ A_0\ B_1\ B_0\ C_i$ using DIP switch or direct jumper wires



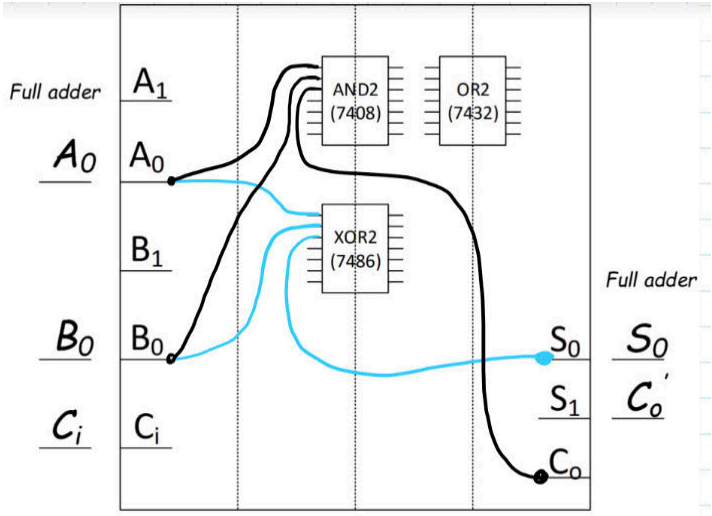
Result:

step3: Define your input pins $A_1\ A_0\ B_1\ B_0\ C_i$ using DIP switch or direct jumper wires



$$S_0 = A_0 \oplus B_0 \oplus C_i$$
$$C_0' = A_0B_0 + (A_0 \oplus B_0)C_i$$

$$S_1 = A_1 \oplus B_1 \oplus C_0'$$
$$C_o = A_1B_1 + (A_1 \oplus B_1)C_0'$$



$$C_o = AB$$
$$S = A \oplus B$$

Results : The circuits were successfully constructed according to the schematics. All output values aligned with the corresponding truth tables, confirming that the circuits functioned as expected.

Half adder (Truth table confirmed in lab)

Inputs : A , B ; Outputs : S , Cout

A	B	S	Cout
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full adder (Truth table confirmed in lab)

Inputs : A , B , Cin ; Outputs : S , Cout

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Two - bit Ripple Carry adder (Truth table confirmed in lab)

Inputs : A1,B1,A0,B0,CIn ; Outputs: CO, S1, S0

A1	A0	BI	B0	CIn	CO	S1	S0
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	0	1	0
0	0	1	0	0	0	1	0
0	0	1	0	1	0	1	1
0	0	1	1	0	0	1	1
0	0	1	1	1	1	0	0
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	0	1	1
0	1	1	0	0	0	1	1
0	1	1	0	1	1	0	0
0	1	1	1	0	1	0	0
0	1	1	1	1	1	0	1
1	0	0	0	0	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	0	0	1	1

1	0	0	1	1	1	0	0
1	0	1	0	0	1	0	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	1
1	1	0	0	1	1	0	0
1	1	0	1	0	1	0	0
1	1	0	1	1	1	0	1
1	1	1	0	0	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

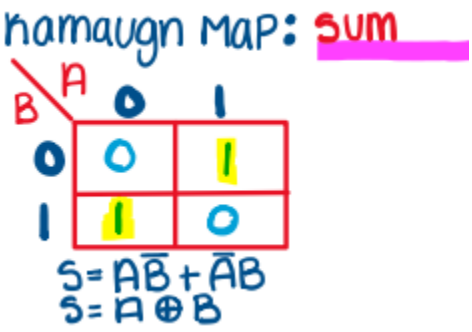
Conclusion:

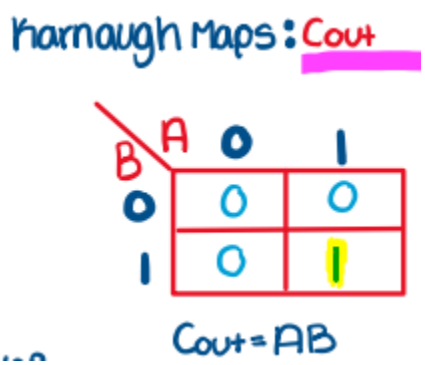
The implementation of rudimentary adder circuits, including the half adder and full adder, was successfully completed. Additionally, two full adders were utilized to construct a combinational 2-bit ripple carry adder. Through this process, a deeper understanding of the functionality and operation of these circuits was achieved. Furthermore, proficiency in truth tables and Karnaugh maps was reinforced, enabling effective debugging of the digital circuit.

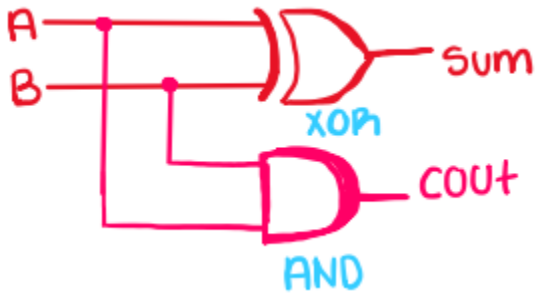
Post lab deliverables :

1. **Provide all design items found in the pre-lab deliverables. If you found that a design needed correc-tions while executing the lab, supply the updated version of that material**

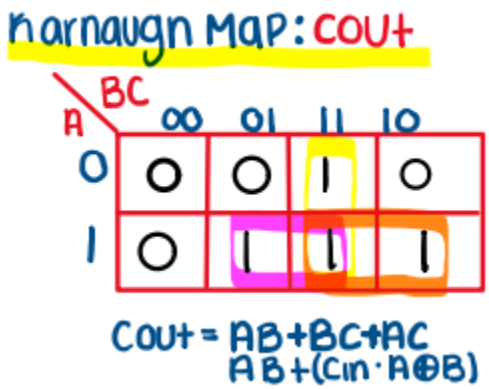
Half adder :

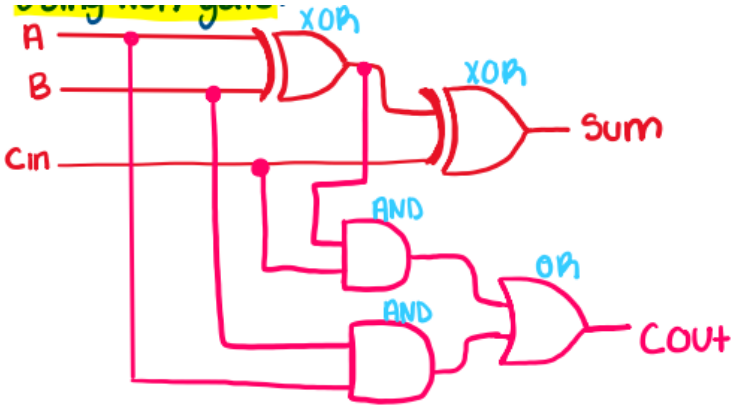




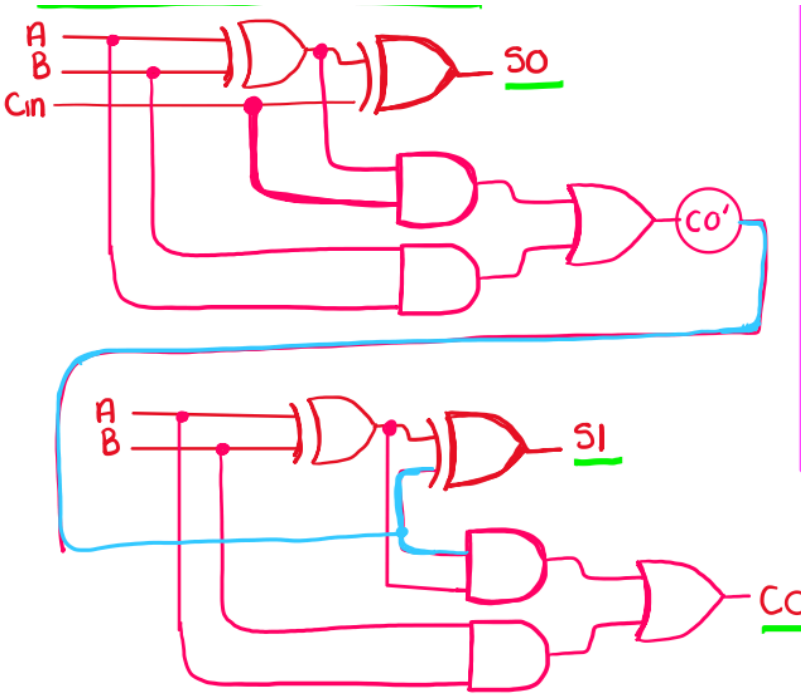


Full adder :



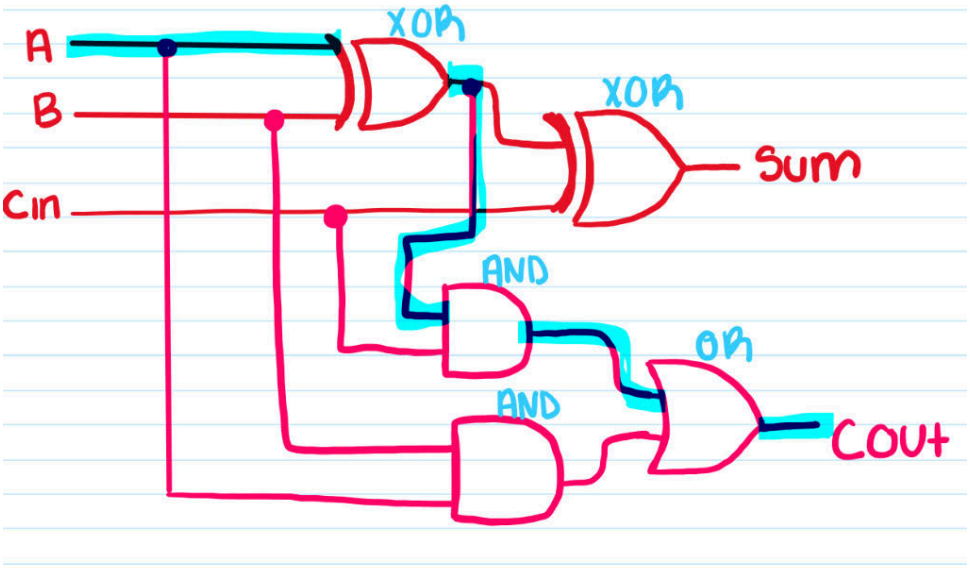


2-Bit Carry Ripple Adder:

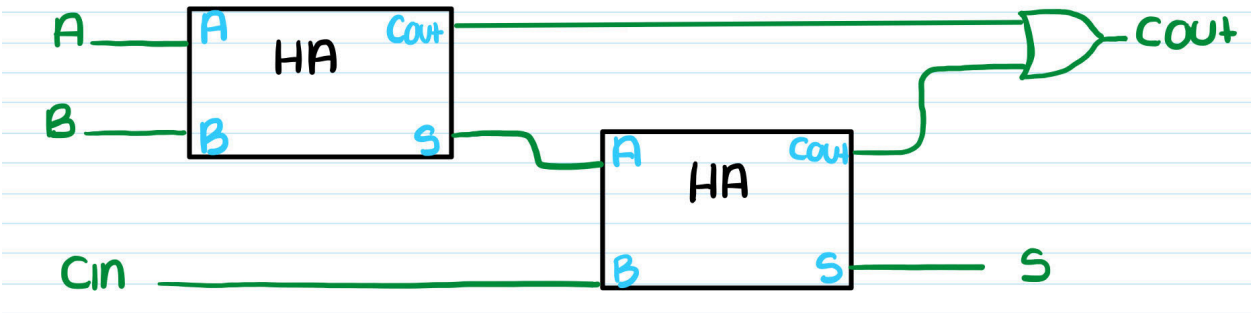


2.Determine the worst case propagation delay for your full adder design. Assume each gate has the same delay of 1 unit. Show the maximum delay path in your schematic. The maximum delay path is known as the critical path for that particular combinational block.

My worst case propagation delay is 3 unit delay highlighted in the schematic :



3. Design a 2-bit carry ripple adder assuming you only have half adder circuits and OR gates to work with. Draw up a schematic for your design using half adder building blocks and OR gates. Be sure the clearly label all inputs and outputs of your blocks



Student feedback :

Overall, the lab proved to be engaging and provided an excellent opportunity to grasp the subject matter. However, it would have been beneficial if the lab had offered more guidance on setting up the breadboard and inputting the truth table using the outputs. Such guidance would have been particularly advantageous at the beginning of the lesson