

ECEN 248 - Lab Report

Lab Number: 4

Lab Title:Simple Arithmetic Logic Unit

Section Number: 510

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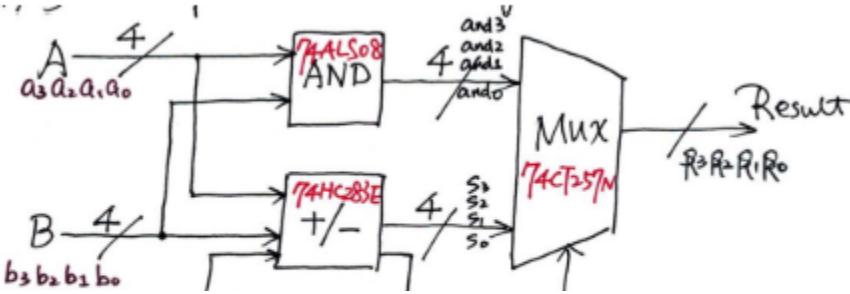
Objectives:

This lab aims to teach students Two's Complement Arithmetic for signed binary numbers and familiarize them with multiplexers. Designing and implementing a 4-bit ALU capable of addition, subtraction, and AND operations. Through hands-on experimentation, they'll gain practical experience in breadboarding and circuit testing, analyzing circuit behavior. Emphasis is placed on documentation and reporting skills, ensuring thorough documentation of procedures and results. Overall, the lab enhances understanding of digital circuit design principles and practical implementation of ALUs.

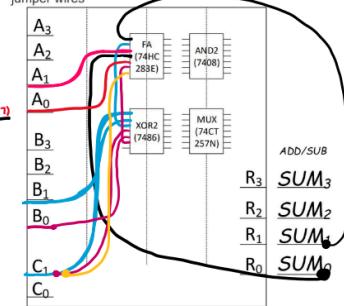
Design:

The initial step of the laboratory experiment involved setting up the necessary components on the breadboard. These included the AND gate (7408), XOR gate (7486), full adder (74HC 292E), and the multiplexer (74CT257N). After this, the wiring was systematically arranged to accommodate the A0 to A3 and B0 to B3 inputs, in conjunction with the two C inputs, C1, and C0. The XOR gate and FA circuit were then employed to execute 3-bit addition and subtraction. In more specific terms, the SUM1 output was acquired by routing S1 to the XOR gate and tying the second input to (C1 XOR B1) and the third input to A1. From the fourth gate, the SUM0 output was obtained, whereas on the FA Circuit's left side, connections were established for A0, (C1 XOR B0), and C1. Moving to the right side, (C1 XOR B2) was linked to A2 to achieve the SUM2 output. This was then followed by inputs for A3 and (C1 XOR B3) to generate the SUM3 output. Subsequently, the inputs were linked to the AND gate, starting from the right side and proceeding downwards. Then, all the outputs were connected to the MUX circuit, beginning

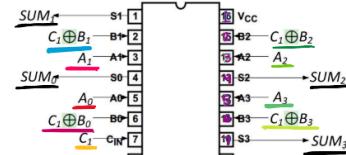
with C0, AND0, and SUM0 to derive R0. The left side of the MUX was then completed with connections for AND1, SUM1, and R1. On the right side, the ground connection was established before linking AND3, SUM3, and R3, and finally, AND2, SUM2, and R2 to conclude the circuit arrangement



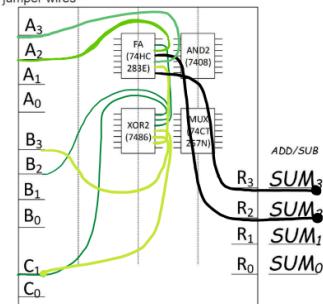
step3: Define your input pins using DIP switch or direct jumper wires



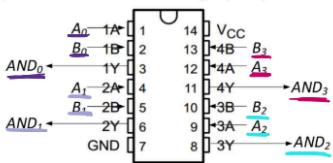
step4: implement 4 bit addition/subtraction with XOR(7486) gates and FA circuit (74HC283E), and verify use simple examples like 8+5=13 and 8-5=3



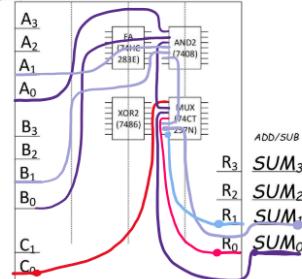
step3: Define your input pins using DIP switch or direct jumper wires



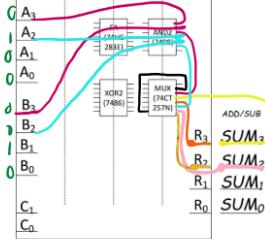
step5: connect 4 bit and with AND gate(7408)



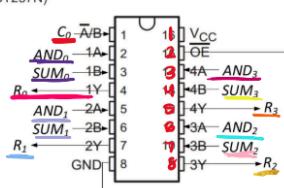
step3: Define your input pins using DIP switch or direct jumper wires



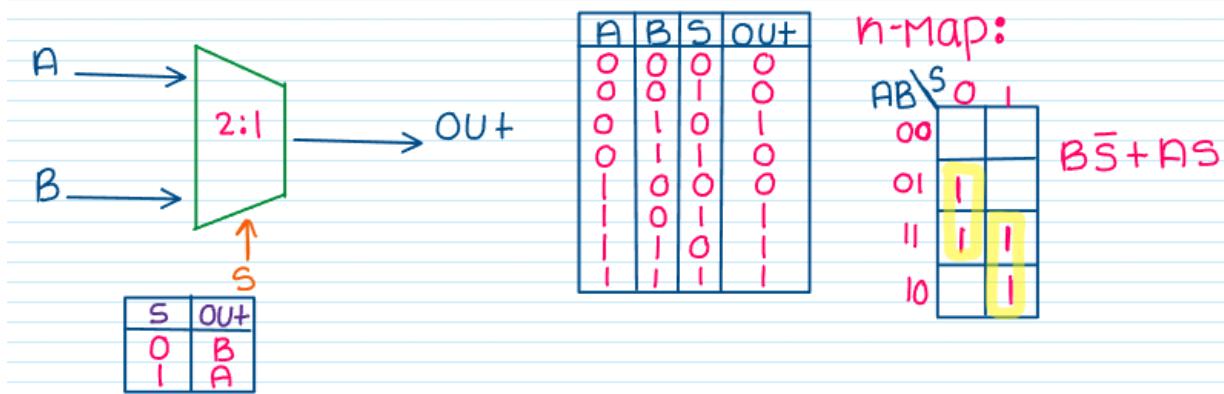
step3: Define your input pins using DIP switch or direct jumper wires



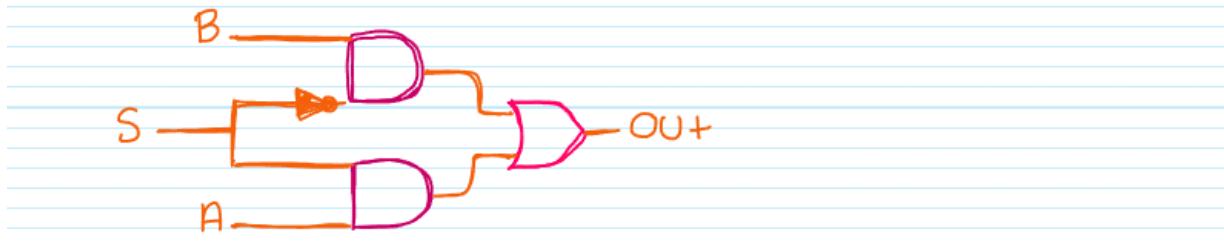
step6: implement 4-bit 2:1 mux using 2:1 MUX circuit (74CT257N)



Truth table and minimized Boolean expression for a 1-bit wide 2:1 MUX:



CIRCUIT For 2:1



Result :

In my demo, I conducted addition, subtraction, and the AND operation to evaluate the functionality of the multiplexer (MUX). The results confirmed the successful implementation of the MUX, demonstrating all three objectives of the lab. For testing and demonstration, addition was implemented as shown. I set inputs as follows: 5 (0101) and 3 (0011), 7 (0111) and 3 (0011). These inputs successfully produced the correct outputs for both addition, subtraction and the AND implementation.

Ex:

1	0	0	0
0	1	0	1
+			
0	1	1	0

$$\left(\begin{array}{c} 8 \\ + 5 \\ \hline 13 \end{array} \right)$$

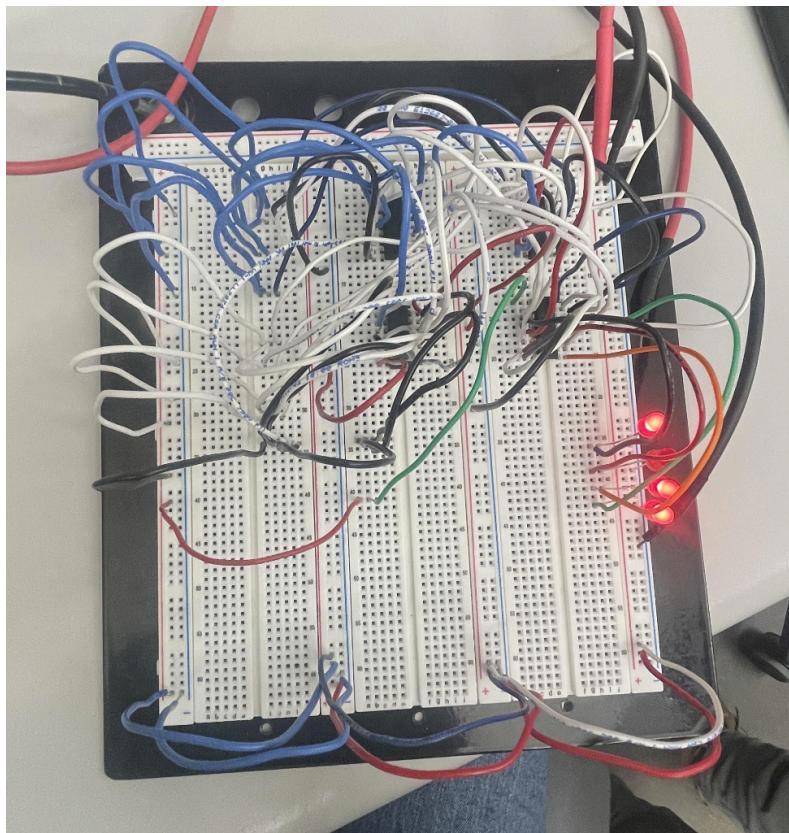
$$= \frac{1 \ 0 \ 0 \ 0}{1 \ 0 \ 1 \ 0} \quad \left(\begin{array}{c} 8 \\ - 5 \\ \hline 3 \end{array} \right)$$

Demo Time [5,3] [7,3]

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		a_3	a_2	a_1	a_0	b_3	b_2	b_1	b_0		
0	0	AND	0	1	0	1	(5)	0	0	1	1
0	1	AND	0	1	0	1	(5)	0	0	1	1
1	0	ADD	0	1	0	1	(5)	0	0	1	0
1	1	SUB	0	1	0	1	(5)	0	0	1	0



Conclusion:

The objective of the lab is to execute and verify the functionality of a 4-bit Arithmetic Logic Unit (ALU), a fundamental component in digital computing. The ALU seemed to be tasked with conducting basic arithmetic operations which include addition, subtraction and logical AND functions. through this lap procedure I gain knowledge about the two fundamental concepts of complement arithmetic towards handling sign numbers and binary representation and also the operation of multiplexers Essentials components for selecting outputs towards multiple inputs in the digital circuits

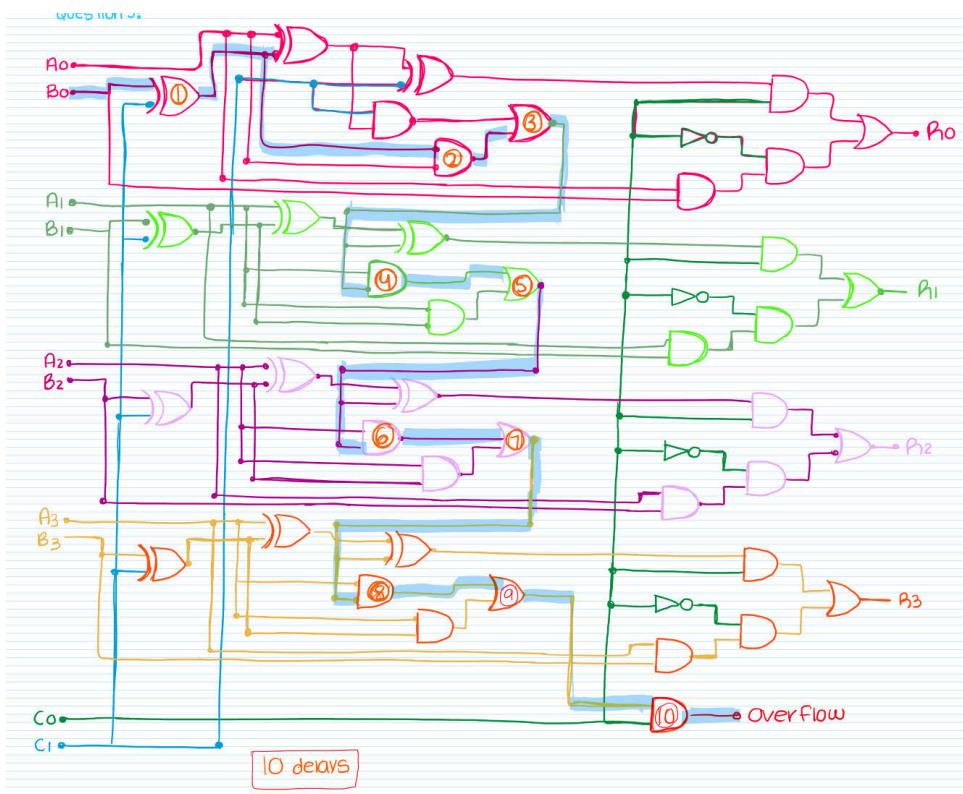
Post-lab Deliverables:

Question 1:

Table 1: c_0 and c_1 operation.

c_0	c_1	Operation	A	B	Result	Overflow
0	0	AND	0100	0110	0100	NO overflow
0	1	AND	0110	1101	0000	NO overflow
1	0	ADD	0100	0110	1010	overflow
1	0	ADD	0100	1101	0001	NO overflow
1	0	ADD	1101	1001	0110	overflow
1	1	SUB	0100	0111	1101	overflow
1	1	SUB	0110	1001	1101	NO overflow

Question 2 :



Question 3

