1. Suppose we want to build a 32-bit counter using the circuit in Figure 1. If the gates used to construct the half-adders in the circuit are assumed to have a 2ns delay each, and the flip-flop overhead is assumed to be negligible, what is the maximum clock frequency we could use to drive our counter? Given the clock frequency you just calculated, how long would it take this counter to roll over (i.e. return to 0). Please show your calculations.

Delay per half-adder : 2ns

Total delay = 32 x 2 = 64ns

Max clock frequency :

$$f = \frac{1}{64 \times 10^{-9}} = 15.625$$

Max clock frequency : 15.625

- Rollover time :

$2^{32} \times 64ns = 4,294,967,296 \times 64 \times 10^{-9} = 275.2$

Max Frequency : 15.625MHz
Time to Roll over: 275.2 seconds

2. Consider the use of a counter to divide an incoming clock. If our incoming clock signal is 32.768 kHz and we need a 64 Hz signal, how many bits would our counter need to have (i.e. what is n) to divide the incoming clock correctly.

$$\frac{32,768}{64} = 512 = 2^9$$

$n = 9$

3. If the Seconds per Division setting for Figure 3 was set to 1 ms/div (ie. the time between axis markings is 1 millisecond), what do you think would be a good bit width for the counter in Figure 4, assuming a 50 MHz clock signal was driving the counter? Explain your answer

$$T_{clk} = \frac{1}{50 \times 10^6} = 20ns$$

To ensure the most significant bit (MSB) of the counter does not toggle during the bouncing period, we want :

$$2^n \times 20ns \geq 5ms \Rightarrow 2^n \geq 250,000$$

- $2^{17} = 131,072 \Rightarrow 2.62ms \rightarrow$ Too short
- $2^{18} = 262,144 \Rightarrow 262,144 \times 20ns = 5.24ms \rightarrow$ good
- $2^{19} = 524,288 \Rightarrow 10.49ms \rightarrow$ outside required range

n = 18, because it gives a counter delay of ~5.24 ms, which is long enough to cover the bouncing seen in Figure 3