

3 Pre-lab**3.1 Half Adder Design**

Construct a truth table for a half adder circuit. From the truth table, create Karnaugh Maps for each output signal (i.e. S and $Cout$) and provide the minimized boolean algebra expressions for each output. Examine the truth table and boolean expression for an XOR gate (you should have created these for the previous post-lab write-up). If you were able to use XOR gates in addition to AND or OR gates in your half adder circuit, how many total gates would the half adder require? Is there an advantage to using XOR gates? Draw a gate-level schematic for the half-adder using a minimum number of gates. Assume you have XOR gates available for use.

3.2 Full Adder Design

Repeat the previous step for a full adder. Assume you can cascade XOR gates when more than 2 inputs are required.

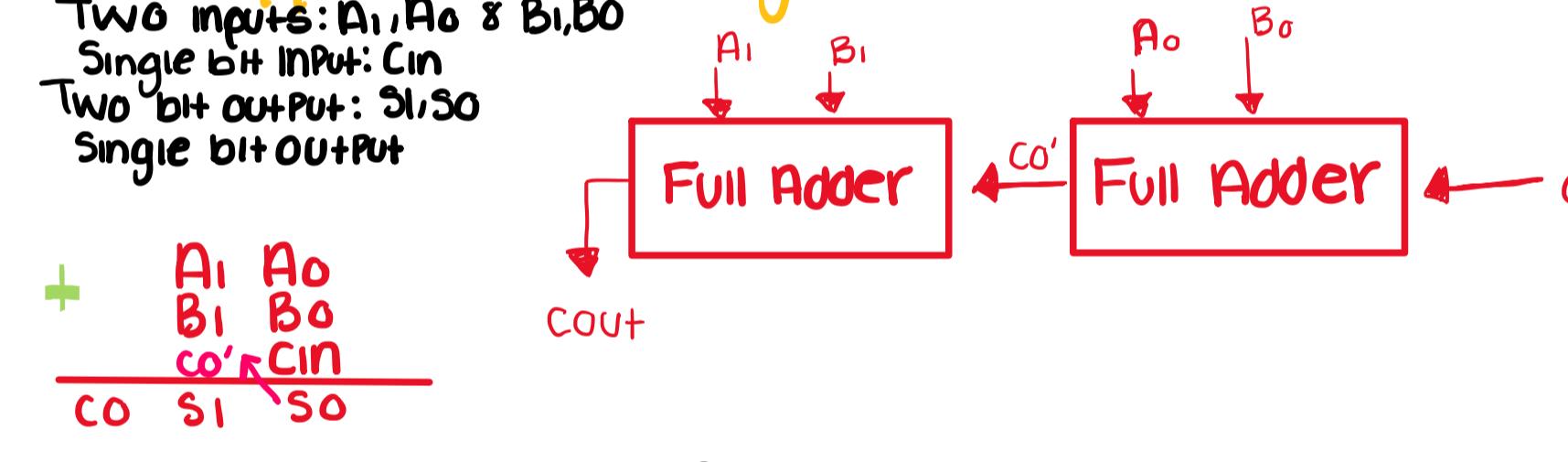
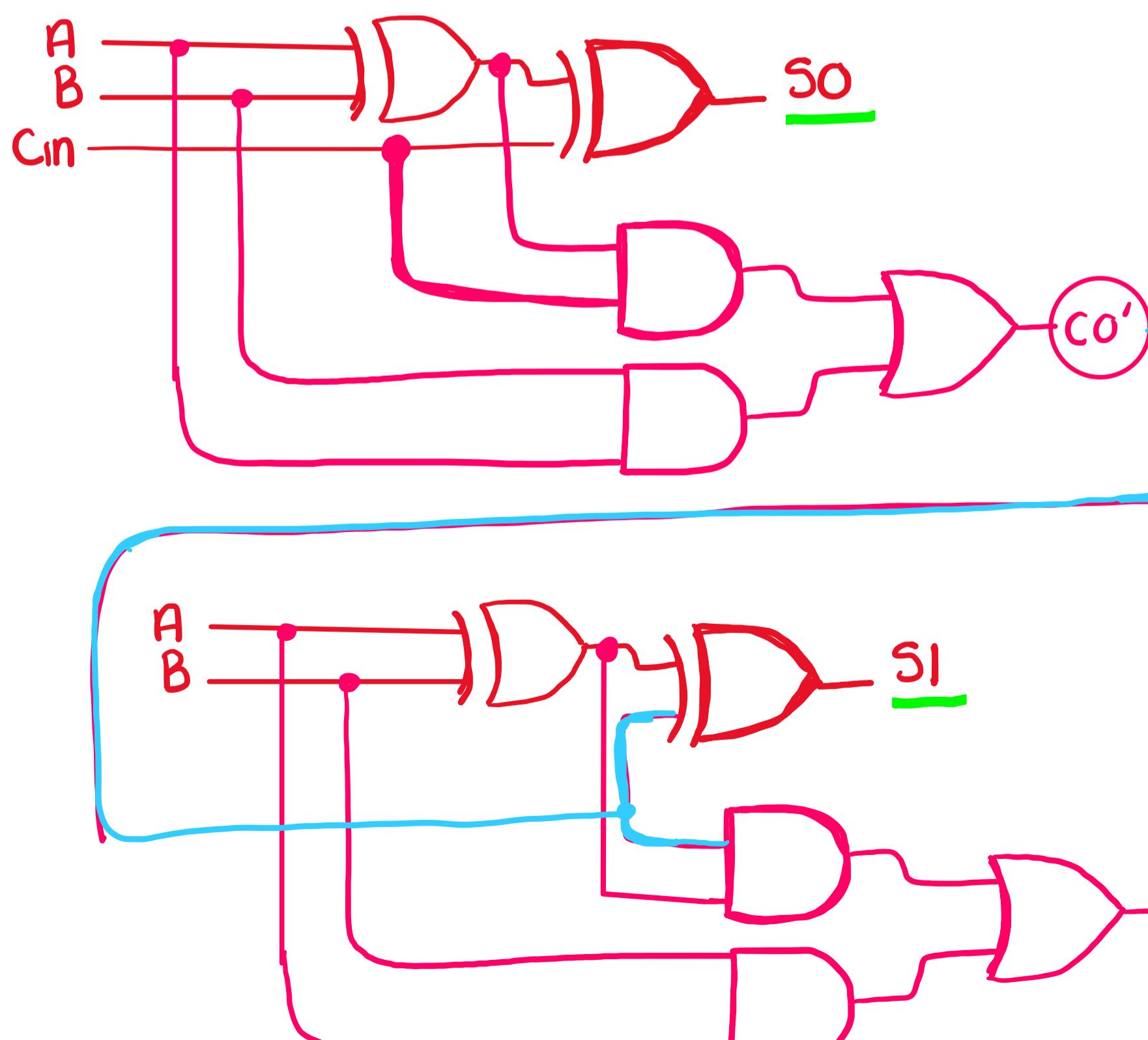
3.3 Ripple Carry Adder Design

Design a 2-bit ripple carry adder using the full adder designed in the previous step. Consult Figure 3 for guidance. Your digital circuit should have two 2-bit inputs, {A1, A0} and {B1, B0}, and one single bit input, {Cin}. Similarly, it should have a 2-bit output, {S1 S0}, and a single bit output, {Cout}. Provide the truth table for the 2-bit adder. You do not have to compute the boolean expressions. Draw the gate-level schematic for the 2-bit ripple carry adder.

3.4 Pre-lab Deliverables

Please include the following items in your pre-lab write-up.

1. Truth table, K-maps, logic expressions without XORs, logic expressions with XORs, and gate-level schematic (reduced gate count) for Half Adder.
2. Truth table, K-maps, logic expressions without XORs, logic expressions with XORs, and gate-level schematic (reduced gate count) for Full Adder.
3. Truth table and gate-level schematic (reduced gate count) for 2-bit Ripple Carry Adder.

3.3 Ripple Adder Design:**GATE LEVEL SCHEMATIC****3.1: HALF ADDER Design****HALF ADDER:**

		A	B	S	Cout
		0	0	0	0
		0	1	1	0
		1	0	1	0
		1	1	0	1

Karnaugh Map: Sum

		A	B	Sum
		0	0	0
		0	1	1
		1	0	1
		1	1	0

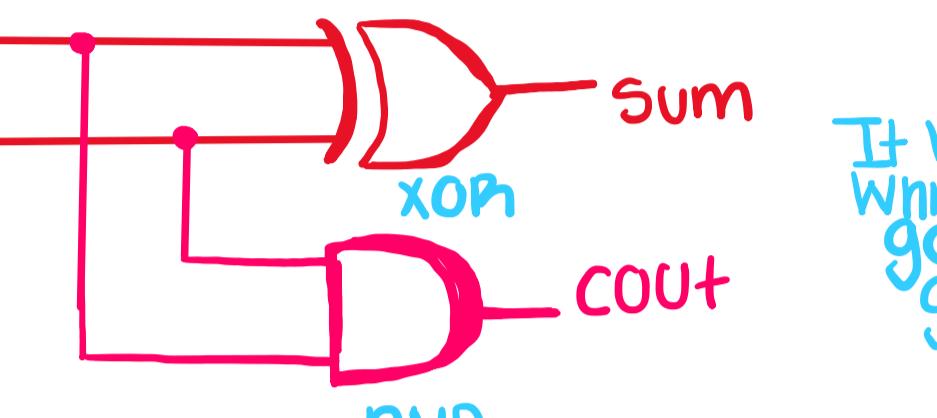
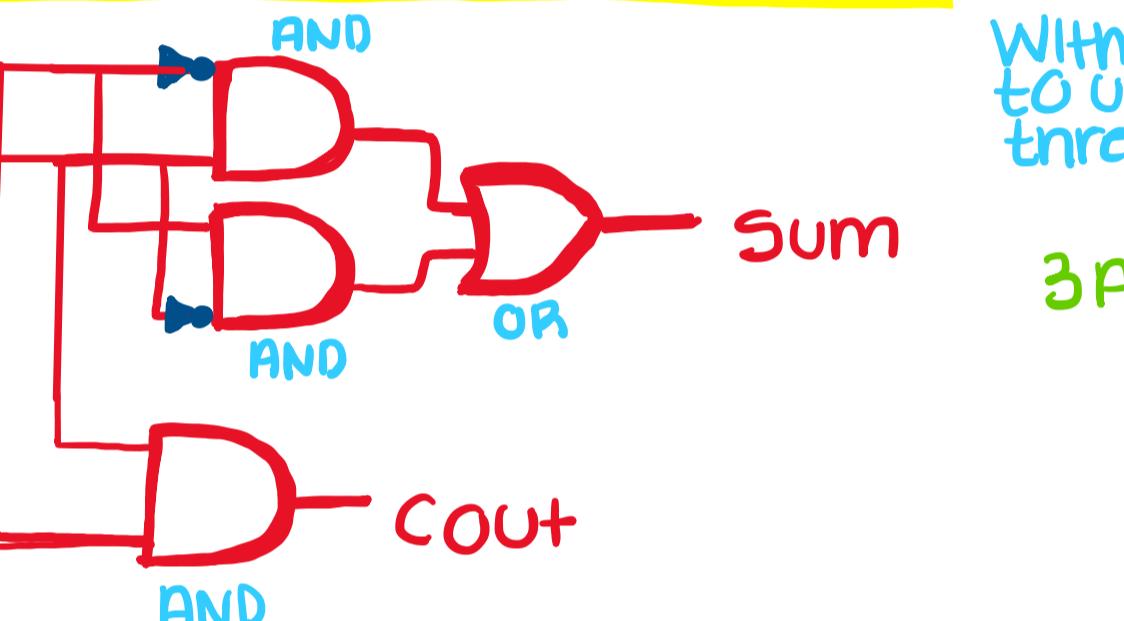
Karnaugh Map: Cout

		A	B	Cout
		0	0	0
		0	1	0
		1	0	0
		1	1	1

$$\begin{aligned} S &= AB + \bar{A}\bar{B} \\ S &= A \oplus B \\ \text{Cout} &= AB \end{aligned}$$

Truth Table of XOP gate

A	B	X	XOP: $A \oplus B$	XOP: $\bar{A} \bar{B} + A\bar{B}$
0	0	0	0	0
0	1	1	1	0
1	0	1	0	1
1	1	0	0	0

Gate level Schematic with XOP**Gate level Schematic without XOP**

It would only require 2 gates which is one xor and one and gate. Using the xor gate makes a simple gate level schematic compared to without it. 1 XOP, 1 AND

Without the xor gate you will have to use a total of four gates. Which are three and gates and one or gate.

3 AND, 1 OR

3.2 Full Adder

		A	B	Cin	Cout	S
		0	0	0	0	0
		0	0	1	0	0
		0	1	0	0	1
		0	1	1	1	0
		1	0	0	1	0
		1	0	1	1	1
		1	1	0	0	1
		1	1	1	0	0

		A	B	Cin	Cout	S
		0	0	0	0	0
		0	0	1	0	0
		0	1	0	0	1
		0	1	1	1	0
		1	0	0	1	0
		1	0	1	1	1
		1	1	0	0	1
		1	1	1	0	0

		A	B	Cin	Cout	S
		0	0	0	0	0
		0	0	1	0	0
		0	1	0	0	1
		0	1	1	1	0
		1	0	0	1	0
		1	0	1	1	1
		1	1	0	0	1
		1	1	1	0	0

		A	B	Cin	Cout	S
		0	0	0	0	0
		0	0	1	0	0
		0	1	0	0	1
		0	1	1	1	0
		1	0	0	1	0
		1	0	1	1	1
		1	1	0	0	1
		1	1	1	0	0