

ModelSim PE Student Edition 10.4a

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

Layout Simulate

sim - Default

Instance Design unit Design unit type

- circuit_I_test_1 circuit_I_te... Module
- test1 circuitI Module
- circuitI circuitI Module
- x1 xor_16_gate Module
- a1 and_16_gate Module
- o16 or_16_gate Module
- m416 mux_4way... Module
- n16[15] nor_gate Module
- n16[14] nor_gate Module
- n16[13] nor_gate Module
- n16[12] nor_gate Module
- n16[11] nor_gate Module
- n16[10] nor_gate Module
- n16[9] nor_gate Module
- n16[8] nor_gate Module
- n16[7] nor_gate Module
- n16[6] nor_gate Module
- n16[5] nor_gate Module
- n16[4] nor_gate Module
- n16[3] nor_gate Module
- n16[2] nor_gate Module
- n16[1] nor_gate Module
- n16[0] nor_gate Module
- n16[15] nor_gate Module
- n16[14] nor_gate Module
- n16[13] nor_gate Module
- n16[12] nor_gate Module
- n16[11] nor_gate Module
- n16[10] nor_gate Module
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- n16[8] nor_gate Module
- n16[7] nor_gate Module
- n16[6] nor_gate Module
- n16[5] nor_gate Module
- n16[4] nor_gate Module
- n16[3] nor_gate Module

Wave - Default

Mags

/circuit_I_test_1/O...	16h0000	000016h0...
/circuit_I_test_1/IN...	16h000c	16h000c
/circuit_I_test_1/IN...	16h000d	16h000d
/circuit_I_test_1/S	2h3	0002h3
/circuit_I_test_1/i	32h00000002	000032h0...
/circuit_I_test_1/fj	32h00000002	000032h0...

Now 100 ns

Cursor 1 0 ns

0 ns 100 ns 200 ns 300 ns 400 ns 500 ns 600 ns 700 ns 800 ns 900 ns 1000 ns

Objects Wave Dataflow Pavithra_B190632CS_Q01_TB_TEST.v Pavithra_B190632CS_Q01_TEST1.v

Transcript

```
# Loading work.mux
# Loading work.nor_gate
# Loading work.nor_gate
# Loading work.xnor_gate
add wave -position insertpoint sim:/circuit_I_test_1/*
VSIM 3> run
# S0=x, S1=x, INPUT_A=0000000000001100, INPUT_B=0000000000001101, OUTPUT=xxxxxxxxxxxxxxx
# S0=0, S1=0, INPUT_A=0000000000001100, INPUT_B=0000000000001101, OUTPUT=0000000000000001
# S0=0, S1=1, INPUT_A=0000000000001100, INPUT_B=0000000000001101, OUTPUT=0000000000001101
# S0=1, S1=0, INPUT_A=0000000000001100, INPUT_B=0000000000001101, OUTPUT=1111111111110010
# S0=1, S1=1, INPUT_A=0000000000001100, INPUT_B=0000000000001101, OUTPUT=0000000000000000
VSIM 4>
```

0 ns to 1 us Project: Assignment_1 Now: 100 ns Delta: 0 sim:/circuit_I_test_1

Type here to search

13:27 23/11/2020