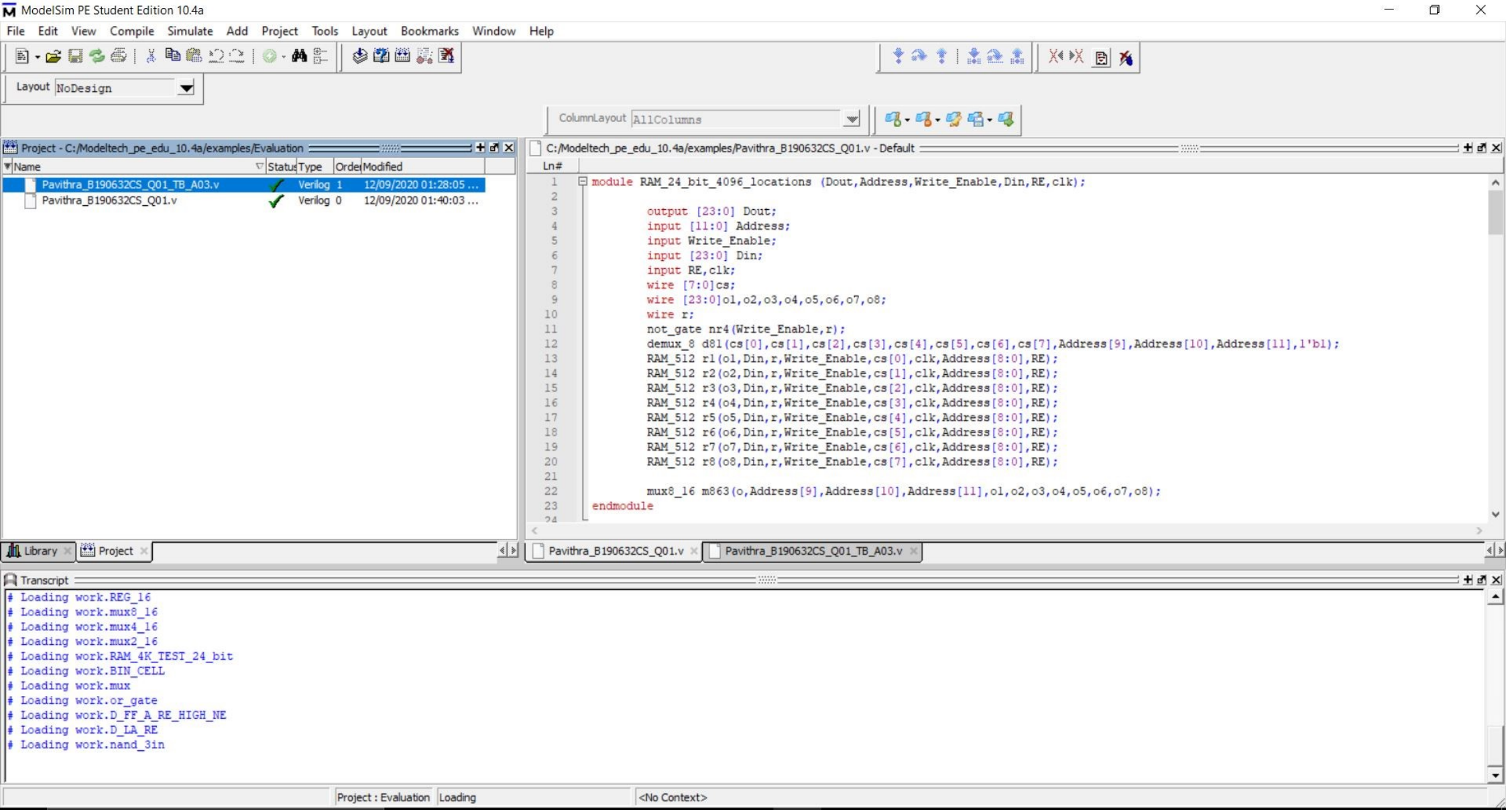
ModelSim PE Student Edition 10.4a
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Layout NoDesign
ColumnLayout AllColumns
Project - C:/Modeltech_pe_edu_10.4a/examples/Evaluation
Name Status Type Order Modified
Pavithra_B190632CS_Q01_TB_A03.v Verilog 1 12/09/2020 01:28:05 ...
Pavithra_B190632CS_Q01.v Verilog 0 12/09/2020 01:40:03 ...
Library Project
C:/Modeltech_pe_edu_10.4a/examples/Pavithra_B190632CS_Q01.v - Default
Ln#
1 module RAM_24_bit_4096_locations (Dout,Address,Write_Enable,Din,RE,clk);
2
3 output [23:0] Dout;
4 input [11:0] Address;
5 input Write_Enable;
6 input [23:0] Din;
7 input RE,clk;
8 wire [7:0]cs;
9 wire [23:0]o1,o2,o3,o4,o5,o6,o7,o8;
10 wire r;
11 not_gate nr4(Write_Enable,r);
12 demux_8 d81(cs[0],cs[1],cs[2],cs[3],cs[4],cs[5],cs[6],cs[7],Address[9],Address[10],Address[11],1'b1);
13 RAM_512 r1(o1,Din,r,Write_Enable,cs[0],clk,Address[8:0],RE);
14 RAM_512 r2(o2,Din,r,Write_Enable,cs[1],clk,Address[8:0],RE);
15 RAM_512 r3(o3,Din,r,Write_Enable,cs[2],clk,Address[8:0],RE);
16 RAM_512 r4(o4,Din,r,Write_Enable,cs[3],clk,Address[8:0],RE);
17 RAM_512 r5(o5,Din,r,Write_Enable,cs[4],clk,Address[8:0],RE);
18 RAM_512 r6(o6,Din,r,Write_Enable,cs[5],clk,Address[8:0],RE);
19 RAM_512 r7(o7,Din,r,Write_Enable,cs[6],clk,Address[8:0],RE);
20 RAM_512 r8(o8,Din,r,Write_Enable,cs[7],clk,Address[8:0],RE);
21
22 mux8_16 m863(o,Address[9],Address[10],Address[11],o1,o2,o3,o4,o5,o6,o7,o8);
23 endmodule
Pavithra_B190632CS_Q01.v
Pavithra_B190632CS_Q01_TB_A03.v
Transcript
Loading work.REG_16
Loading work.mux8_16
Loading work.mux4_16
Loading work.mux2_16
Loading work.RAM_4K_TEST_24_bit
Loading work.BIN_CELL
Loading work.mux
Loading work.or_gate
Loading work.D_FF_A_RE_HIGH_NE
Loading work.D_LA_RE
Loading work.nand_3in
Project : Evaluation
Loading
<No Context>