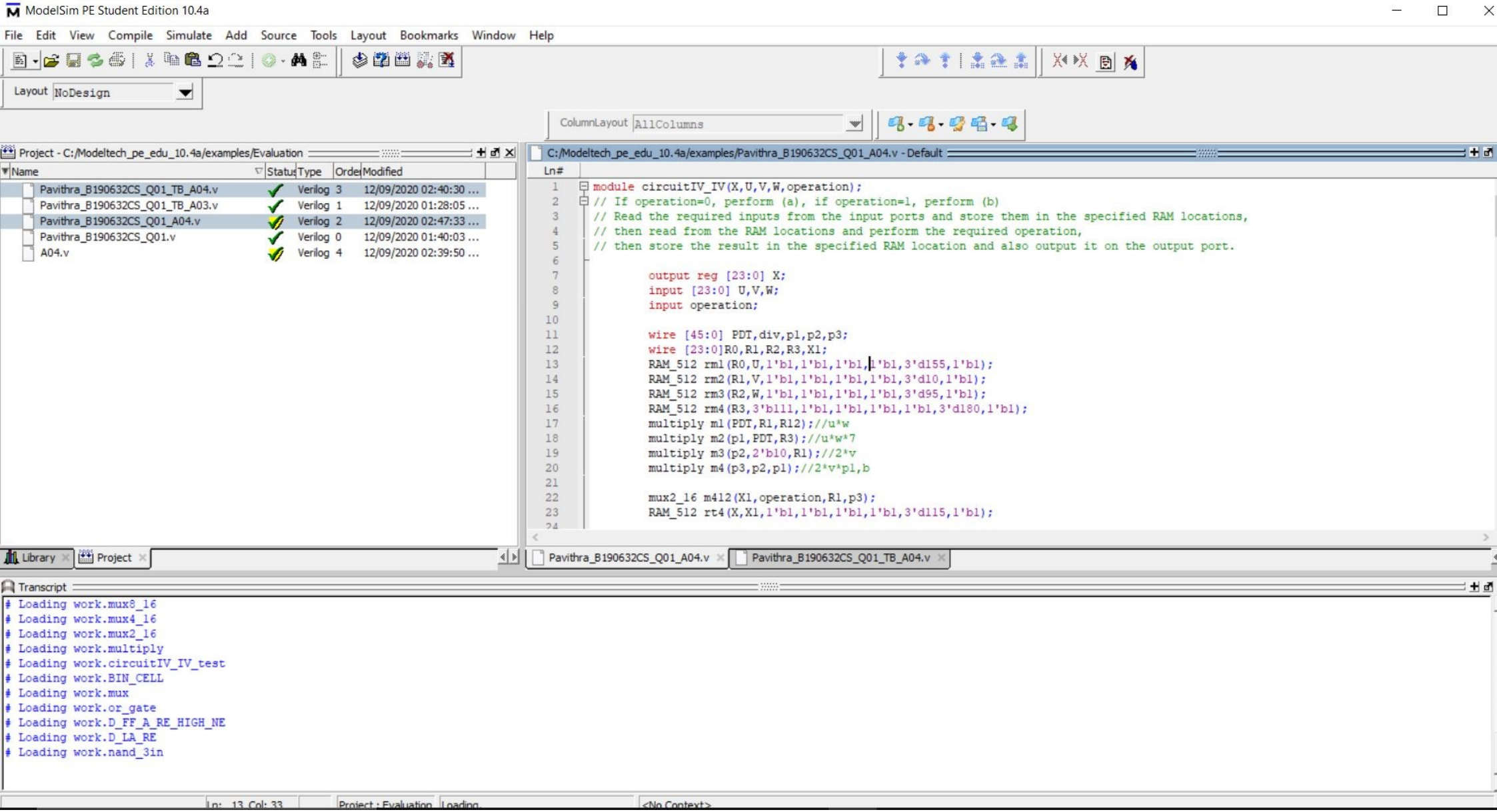
ModelSim PE Student Edition 10.4a
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Layout NoDesign
ColumnLayout AllColumns
Project - C:/Modeltech_pe_edu_10.4a/examples/Evaluation
Name Status Type Order Modified
Pavithra_B190632CS_Q01_TB_A04.v Verilog 3 12/09/2020 02:40:30 ...
Pavithra_B190632CS_Q01_TB_A03.v Verilog 1 12/09/2020 01:28:05 ...
Pavithra_B190632CS_Q01_A04.v Verilog 2 12/09/2020 02:47:33 ...
Pavithra_B190632CS_Q01.v Verilog 0 12/09/2020 01:40:03 ...
A04.v Verilog 4 12/09/2020 02:39:50 ...
Library Project
C:/Modeltech_pe_edu_10.4a/examples/Pavithra_B190632CS_Q01_A04.v - Default
Ln#
1 module circuitIV_IV(X,U,V,W,operation);
2 // If operation=0, perform (a), if operation=1, perform (b)
3 // Read the required inputs from the input ports and store them in the specified RAM locations,
4 // then read from the RAM locations and perform the required operation,
5 // then store the result in the specified RAM location and also output it on the output port.
6
7 output reg [23:0] X;
8 input [23:0] U,V,W;
9 input operation;
10
11 wire [45:0] PDT,div,p1,p2,p3;
12 wire [23:0]R0,R1,R2,R3,X1;
13 RAM_512 rm1(R0,U,1'b1,1'b1,1'b1,1'b1,3'd155,1'b1);
14 RAM_512 rm2(R1,V,1'b1,1'b1,1'b1,1'b1,3'd10,1'b1);
15 RAM_512 rm3(R2,W,1'b1,1'b1,1'b1,1'b1,3'd95,1'b1);
16 RAM_512 rm4(R3,3'b111,1'b1,1'b1,1'b1,1'b1,3'd180,1'b1);
17 multiply m1(PDT,R1,R12);//u*w
18 multiply m2(p1,PDT,R3);//u*w*7
19 multiply m3(p2,2'b10,R1);//2*v
20 multiply m4(p3,p2,p1);//2*v*p1,b
21
22 mux2_16 m412(X1,operation,R1,p3);
23 RAM_512 rt4(X,X1,1'b1,1'b1,1'b1,1'b1,3'd115,1'b1);
Pavithra_B190632CS_Q01_A04.v
Pavithra_B190632CS_Q01_TB_A04.v
Transcript
Loading work.mux8_16
Loading work.mux4_16
Loading work.mux2_16
Loading work.multiply
Loading work.circuitIV_IV_test
Loading work.BIN_CELL
Loading work.mux
Loading work.or_gate
Loading work.D_FF_A_RE_HIGH_NE
Loading work.D_LA_RE
Loading work.nand_3in
Ln: 13 Col: 33
Project : Evaluation
Loading
<No Context>