**Design of Adders and Multipliers using Transmission Gate Logic and CMOS Logic**

Name- Pawan kumar

---

## Delay Analysis of 1 bit, 4 bit, 8 bit and 16 bit Ripple Carry Full Adders

VDD= 1.8 V

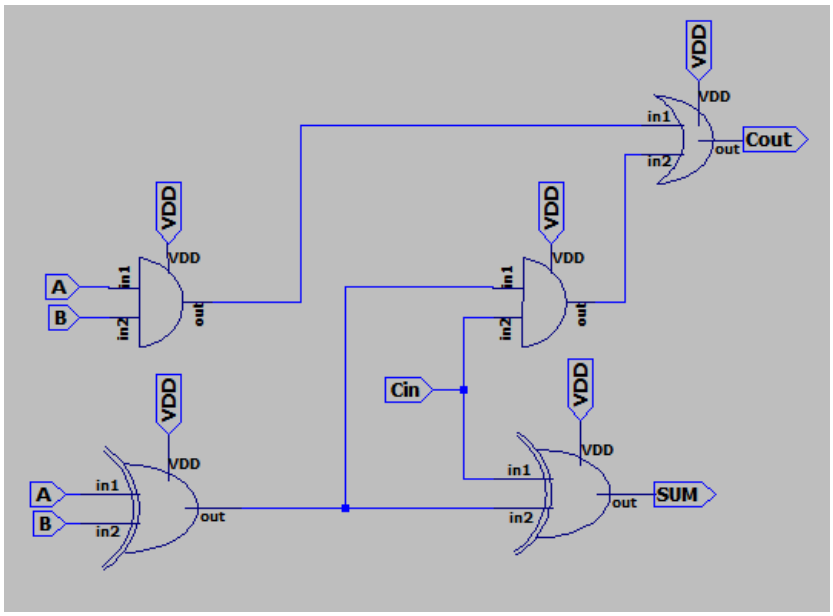
Lengths of all PMOS and NMOS is L=180 nm

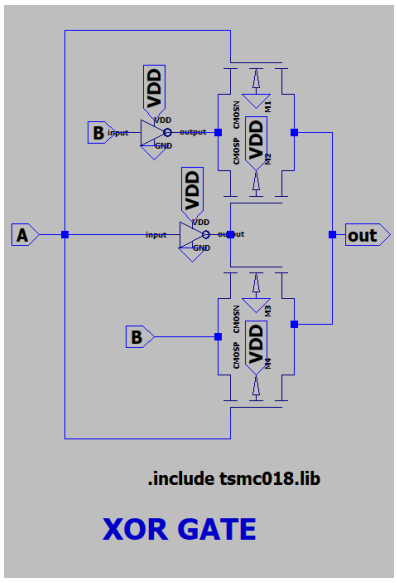
Width of all PMOS is Wp=600 nm

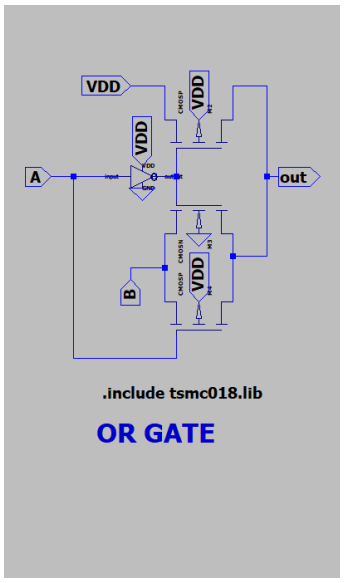
Width of all NMOS is Wn=200 nm

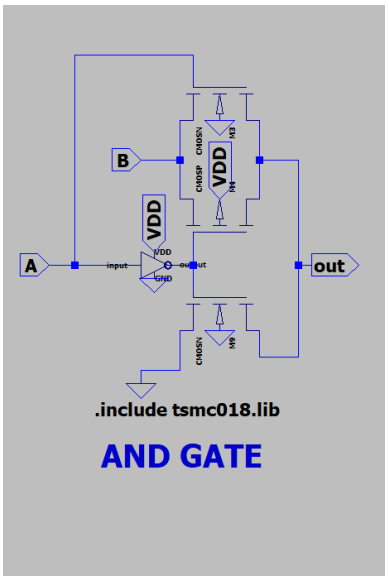
Input capacitance of CMOS inverter is Cin=1.8 fF

**1-bit full adder using Transmission Gate** total transistor = 27



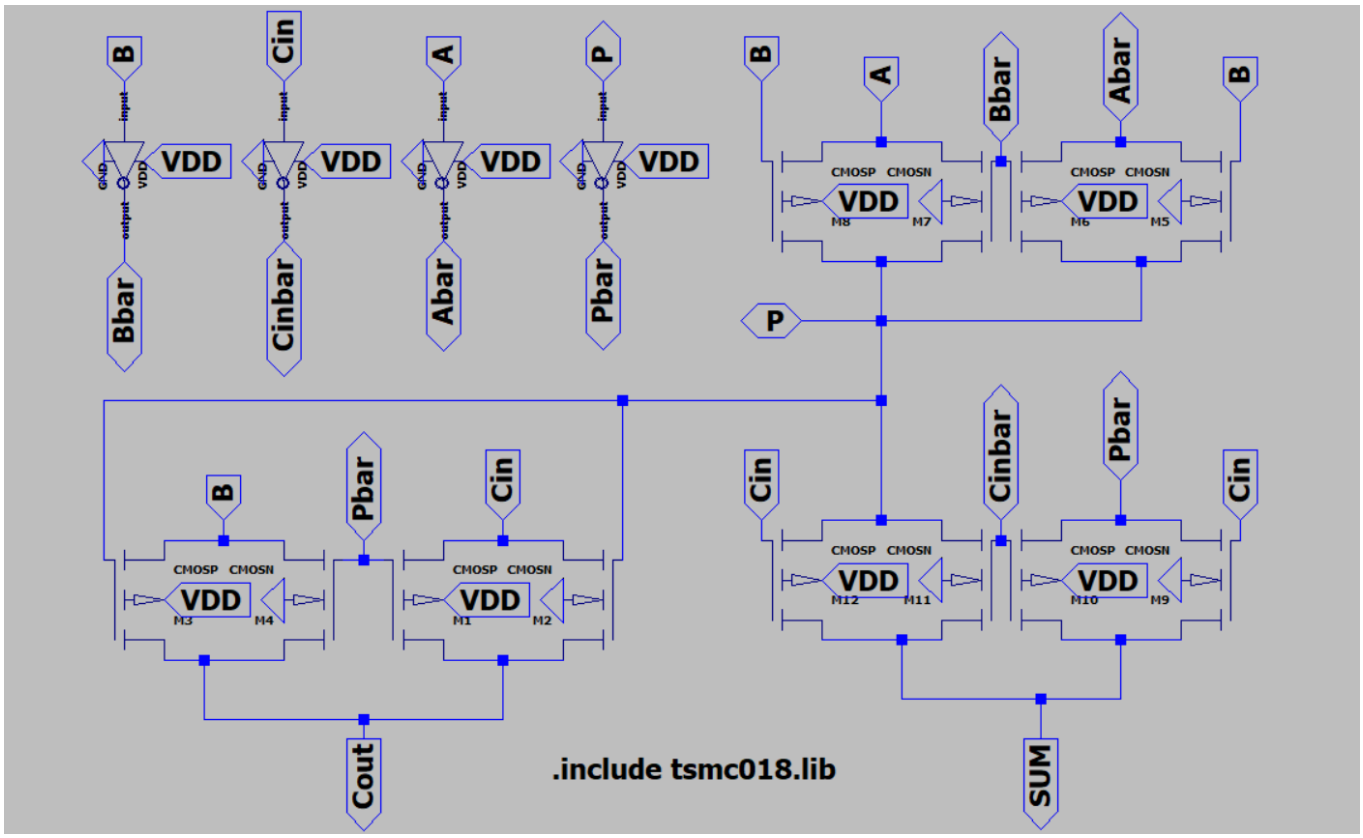



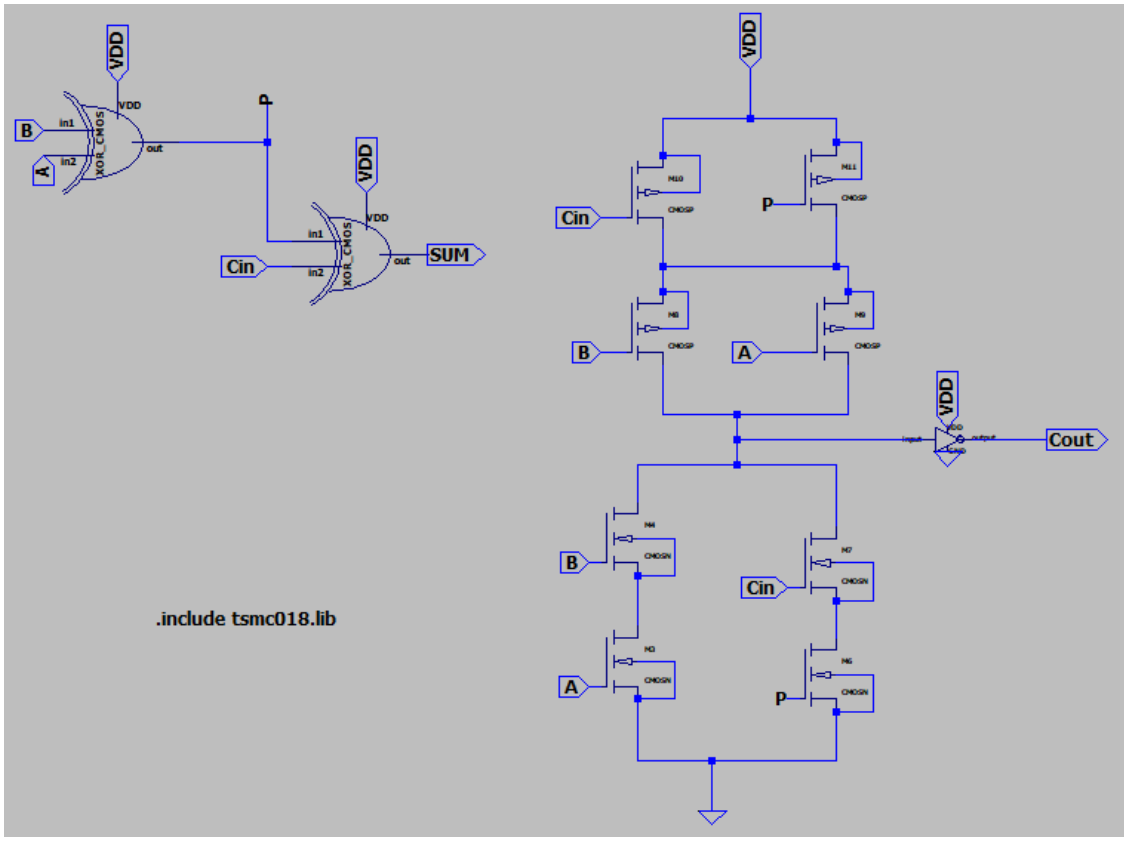



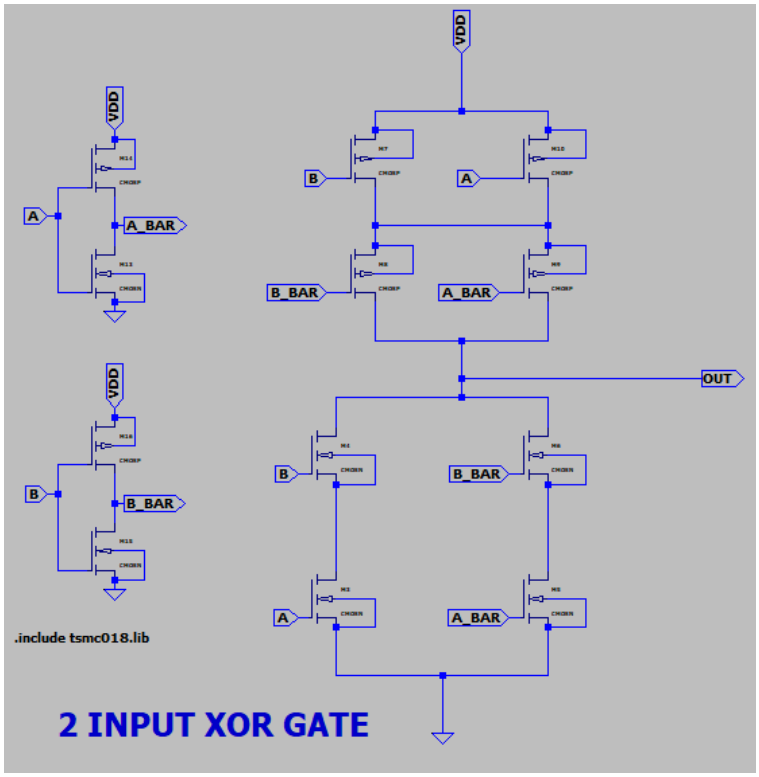
**1-bit full adder using Transmission Gate*** ** total transistor = 20

*** here adder is designed using XOR GATE and MULTIPLEXER

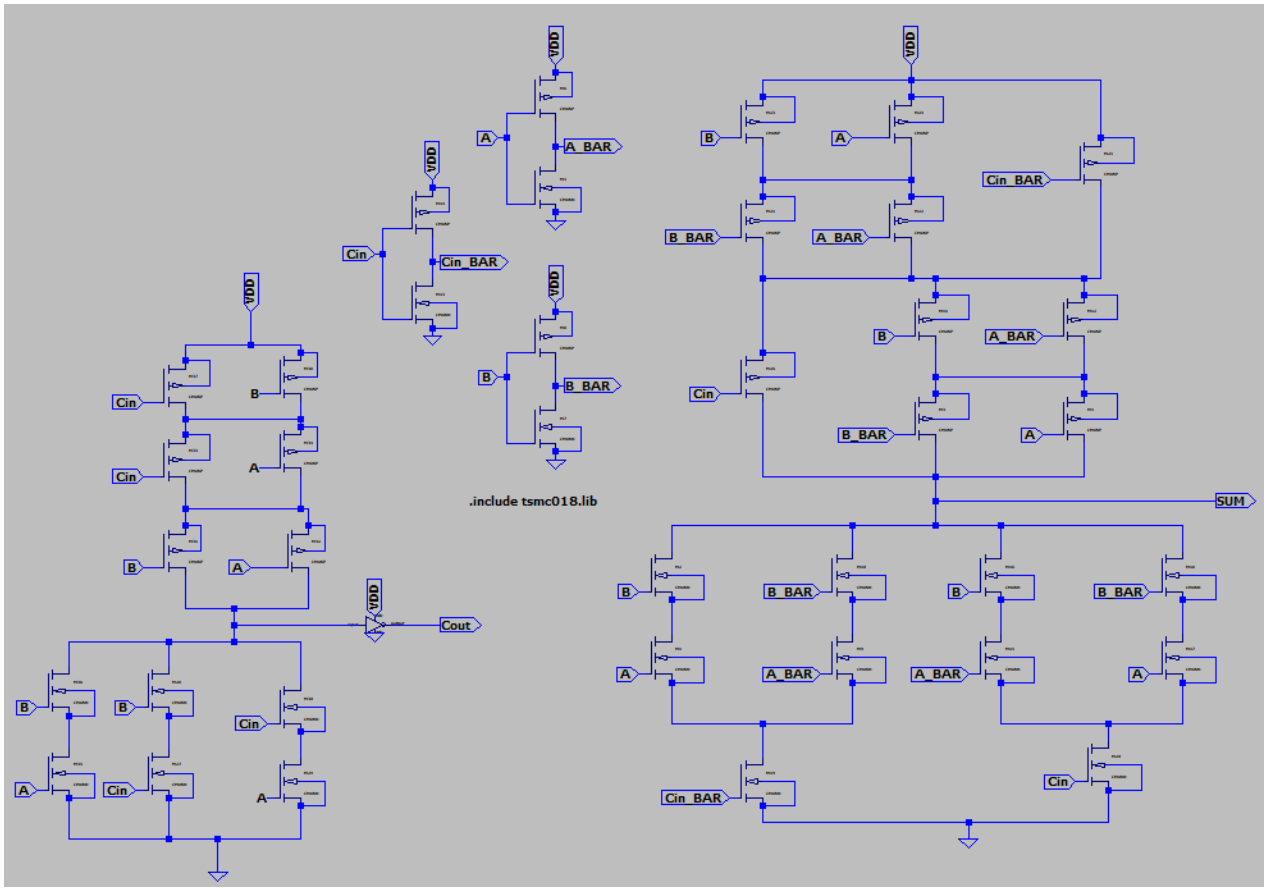


**1-bit full adder using CMOS with two input XOR** total transistor = 34



**1-bit full adder using CMOS with three input XOR** total transistor = 40



# 1-bit adder

Without any loading on output

| Type of 1-bit adder | Inherent delay($t_{id}$) |
|---|---|
| 1-bit full adder using Transmission Gate | 112 ps $t$(A-Cout)<br>110 ps $t$(A-SUM) |
| 1-bit full adder using CMOS with two input XOR | 193 ps $t$(A-Cout)<br>140 ps $t$(A-SUM) |
| 1-bit full adder using CMOS with three input XOR | 98 ps $t$(A-Cout)<br>110 ps $t$(A-SUM) |
| 1-bit full adder using TG+Mux | 86ps $t$(A-Cout) |

Let's Fanout=4 $C_{load}$ =7.2 fF

| | Inherent delay($t_{id}$) |
|---|---|
| 1-bit full adder using Transmission Gate | 216 ps $t$(A-Cout)<br>109 ps $t$(A-SUM) |
| 1-bit full adder using CMOS with two input XOR | 243 ps $t$(A-Cout)<br>201 ps $t$(B-SUM) |
| 1-bit full adder using CMOS with three input XOR | 155 ps $t$(B-Cout)<br>102 ps $t$(B-SUM) |
| 1-bit full adder using TG+Mux | 134ps $t$(A-Cout) |

For 1 bit addition transmission gate full adder has least delay.
Also used least no of transistor (27)

# 4-bit adder

Without any loading on output

| Type of 4-bit adder | Inherent delay($t_{id}$) | Average delay | Number of Transistor used |
|---|---|---|---|
| 4-bit full adder using Transmission Gate Without buffer | 471 ps discharging<br>590 ps charging | 530.5 ps | 4*27=108 |
| 4-bit full adder using CMOS with two input XOR | 558 ps discharging<br>566 ps charging<br>t(B0-Cout) | 562 ps | 4*34=136 |
| 4-bit full adder using CMOS with three input XOR | 716 ps discharging<br>536 ps charging<br>t(A0-Cout) | 626 ps | 4*40=160 |
| 4-bit full adder using Transmission Gate Replacing third full adder with a full adder using CMOS with two input XOR | 435 ps discharging<br>457 ps charging<br>t(B0-Cout) | 446 ps | 3*27+34=115 |
| 4-bit full adder using Transmission Gate Replacing third full adder with a full adder using CMOS with three input XOR | 511 ps discharging<br>491 ps charging<br>t(A0-Cout) | 501 ps | 3*27+40=121 |
| 4-bit full adder using Transmission Gate With buffer<br>Adding Buffer after every two Adder, except the last stage. | 445 ps discharging<br>480 ps charging<br>t(A0-Cout) | 462 ps | 4*27+4=112 |
| 4-bit full adder using Transmission Gate And Multiplexer*** Replacing third full adder with a full adder using CMOS with two input XOR | 362 ps discharging<br>380 ps charging<br>t(A0-SUM3) | 371 ps | 20*3+34=96 |
| 4-bit full adder using Transmission Gate And Multiplexer*** Adding Buffer after every two Adder, except the last stage. | 356 ps discharging<br>370 ps charging<br>t(A0-SUM3) | 363 ps | 20*4+4=84 |

*** here adder is designed using XOR GATE and MULTIPLEXER

Let's Fanout=4 $C_{load}$ =7.2 fF

| Type of 4-bit adder | Inherent delay($t_{id}$) $t_{(B0\text{-}Cout)}$ | Average delay ($t_{charging}$ +$t_{discharging}$)/2 |
|---|---|---|
| 4-bit full adder using Transmission Gate Without buffer | 651 ps discharging<br>780 ps charging | 715.5 ps |
| 4-bit full adder using CMOS with two input XOR | 609 ps discharging<br>617 ps charging | 613 ps |
| 4-bit full adder using CMOS with three input XOR | 667 ps discharging<br>572 ps charging | 619.5 ps |
| 4-bit full adder using Transmission Gate. Replacing 3 full adder with a full adder using CMOS with three input XOR | 550 ps discharging<br>570 ps charging | 560 ps |
| 4-bit full adder using Transmission Gate. Replacing third full adder with a full adder using CMOS with two input XOR | 507 ps discharging<br>540 ps charging | 523.5 ps |
| 4-bit full adder using Transmission Gate With buffer<br>Adding Buffer after every two Adder, except the last stage. | 544 ps discharging<br>581 ps charging | 562.5 ps |

Without any loading on output

| Type of 16-bit adder | Inherent delay($t_{id}$) $t_{(B0\text{-}Cout)}$ | Average delay | Number of Transistor used |
|---|---|---|---|
| 16-bit full adder using Transmission Gate Without buffer | 5.9 ns discharging<br>9.6 ns charging | 7.75 ns | 432 |
| 16-bit full adder using CMOS with two input XOR | 2.07 ns discharging<br>2.02 ns charging | 2.045 ns | 544 |
| 16-bit full adder using CMOS with three input XOR | 2.52 ns discharging<br>2.18 ns charging | 2.35 ns | 640 |
| 16-bit full adder using Transmission Gate Replacing **3*K** full adder with a full adder using CMOS with two input XOR | 2.39 ns discharging<br>2.46 ns charging | 2.425 ns | 11*27+5*34=467 |
| 16-bit full adder using Transmission Gate Replacing **3*K** full adder with a full adder using CMOS with three input XOR | 2.08 ns discharging<br>2.33 ns charging | 2.205 ns | 11*27+5*40=497 |
| 16-bit full adder using Transmission Gate With buffer<br>Adding Buffer after every two Adder, except the last stage. | 2.14 ns discharging<br>2.30 ns charging | 2.22 ns | 16*27+7+4=460 |
| 16-bit full adder using Transmission Gate with Multiplexer<br>Replacing **3*K** full adder with a full adder using CMOS with two input XOR | 1.56 ns discharging<br>1.68 ns charging | 1.62 ns | 11*20+5*34=390 |

Let's Fanout=4 $C_{load}$ =7.2 fF

| | Inherent delay($t_{id}$) $t_{(B0\text{-}Cout)}$ | Average delay ($t_{charging}$ +$t_{discharging}$)/2 |
|---|---|---|
| 16-bit full adder using Transmission Gate Without buffer | 6.25 ns discharging<br>10.26 ns charging | 8.255 ns |
| 16-bit full adder using CMOS with two input XOR | 2.12 ns discharging<br>2.08 ns charging | 2.1 ns |
| 16-bit full adder using CMOS with three input XOR | 2.57 ns discharging<br>2.23 ns charging | 2.4 ns |
| 16-bit full adder using Transmission Gate Replacing **3*K** full adder with a full adder using CMOS with three input XOR | 2.15 ns discharging<br>2.42 ns charging | 2.295 ns |
| 16-bit full adder using Transmission Gate Replacing **3*K** full adder with a full adder using CMOS with two input XOR | 2.46 ns discharging<br>2.54 ns charging | 2.5 ns |
| 16-bit full adder using Transmission Gate With buffer<br>Adding Buffer after every two Adder, except the last stage. | 2.25 ns discharging<br>2.43 ns charging | 2.34 ns |

For 16 bit addition CMOS full adder with two input XOR has least delay.

Total component required for **4-bit multiplier**

AND gate = 16
Half Adder = 4
Full Adder = 8

Without any loading on output

| Type of 4-bit multiplier | Inherent delay($t_{id}$) t (P6 - B0 ) | Number of Transistor used |
|---|---|---|
| 4-bit multiplier using Transmission Gate technology | 976 ps | 16*5+4*11+8*27=340 |
| 4-bit Multiplier using CMOS technology | 965 ps | 16*6+4*18+8*34=440 |
| 4-bit Multiplier using both CMOS and Transmission Gate technology | 836 ps | 16*5+(3*11+18)+(6*27+2*34) =361 |
| 4-bit Multiplier using CMOS and Transmission Gate technology*** | 803 ps | 16*5+(3*11+18)+(6*20+2*34) =319 |

*** here adder is designed using XOR GATE and MULTIPLEXER

Total component required for **8-bit multiplier**

AND gate = 64
Half Adder = 8
Full Adder = 48

Without any loading on output

| Type of 8-bit multiplier | Inherent delay($t_{id}$) t (P11 - B0 ) | Number of Transistor used |
|---|---|---|
| 8-bit multiplier using only Transmission Gate Technology | 2.77 ns | 64*5+8*11+48*27=1704 |
| 8-bit Multiplier using CMOS technology | 1.93 ns | 64*6+8*18+48*34=2160 |
| 8-bit Multiplier using both CMOS and Transmission Gate technology | 1.82 ns | 64*5+8*11+(32*27+16*34) =1816 |
| 8-bit Multiplier using both CMOS and Transmission Gate technology*** | 1.75 ns | 64*5+(7*11+18)+(35*20+13*34) =1557 |

*** here adder is designed using XOR GATE and MULTIPLEXER

**Implementing 8 - bit Multiplier using 4 - bit Multiplier**

Component required

- 4 4-bit multiplier
- 2 8-bit Full adder
- 2 half adder
- 1 Xor gate

| Type of 8-bit multiplier | Inherent delay($t_{id}$) t (P11 - B0 ) | Number of Transistor used |
|---|---|---|
| 8-bit multiplier using 4 - bit Multiplier | 1.64 ns | 4*361+2*230+2*11+8=1934 |
| 8-bit multiplier using 4 - bit Multiplier*** | 1.62 ns | 4*319+2*230+2*11+8=1766 |

*** here adder is designed using XOR GATE and MULTIPLEXER

**Implementing 16 - bit Multiplier using 8 - bit Multiplier**

Component required

- 4 8-bit multiplier
- 4 8-bit Full adder
- 6 half adder
- 1 Xor gate

| Type of 16-bit multiplier | Number of Transistor used |
|---|---|
| 16-bit multiplier using 8 - bit Multiplier | 4*1934+4*230+6*11+8=8730 |
| 16-bit multiplier using 8 - bit Multiplier*** | 4*1766+4*230+6*11+8=8058 |

*** here adder is designed using XOR GATE and MULTIPLEXER