UART driver for Serial I/O on the Versatile board

The ARM Versatile board supports four PL011 UART devices for serial I/O .

Each UART device has a base address in the system memory map.

The base addresses of the 4 UARTs are

UART0: 0x101F1000

UART1: 0x101F2000

UART2: 0x101F3000

UART3: 0x10090000

UART Functional diagram

2.2 Functional description 2.2

Figure 2-1 shows a block diagram of the UART.

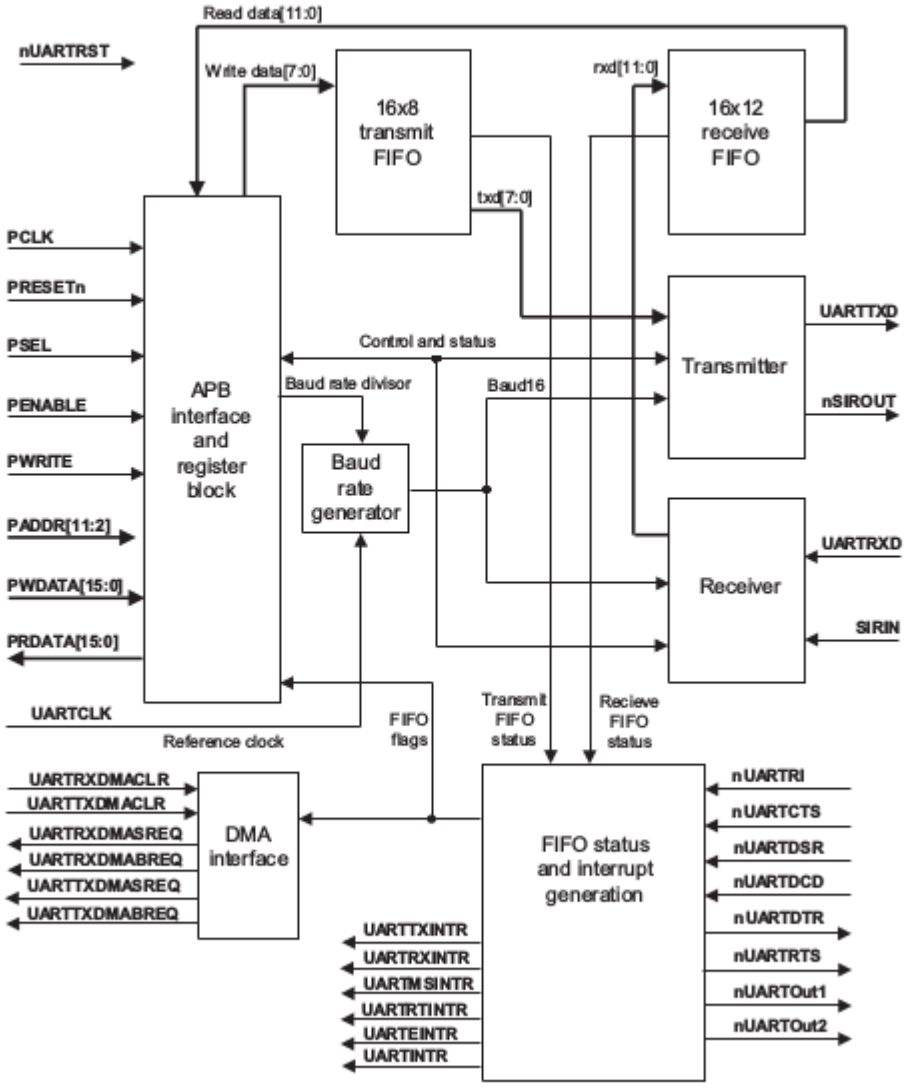

Figure 2-1 UART block diagram

UART driver for Serial I/O

Each UART has a number of registers, which are byte offsets from the base address. The following lists the most important UART registers.

0x00 UARTDR - Data register: for read/write chars

0x18 UARTFR - Flag register: TxEmpty, RxFull, etc.

0x24 UARIBRD - Baud rate register: set baud rate

0x2C UARTLCR - Line control register: bits per char, parity, etc.

0x38 UARTIMIS - Interrupt mask register for TX and RX interrupts

PL011 registers from technical Ref manual

0x004	RW	4/0	0x0	UARTRSR/ UARTECR	*Receive status register/error clear register, UARTRSR/UARTECR* on page 3-6
0x008-0x014	-	-	-	-	Reserved
0x018	RO	9	0b-10010---	UARTFR	*Flag register, UARTFR* on page 3-8
0x01C	-	-	-	-	Reserved
0x020	RW	8	0x00	UARTILPR	*IrDA low-power counter register, UARTILPR* on page 3-9
0x024	RW	16	0x0000	UARTIBRD	*Integer baud rate register, UARTIBRD* on page 3-10
0x028	RW	6	0x00	UARTFBRD	*Fractional baud rate register, UARTFBRD* on page 3-10
0x02C	RW	8	0x00	UARTLCR_H	*Line control register, UARTLCR_H* on page 3-1
0x030	RW	16	0x0300	UARTCR	*Control register, UARTCR* on page 3-15
0x034	RW	6	0x12	UARTIFLS	*Interrupt FIFO level select register, UARTIFLS* page 3-17

Initialise the UART

(1) Write a divisor value to the baud rate register for a desired baud rate.

The ARM PL011 technical reference manual lists the following integer divisor values (based on 7.38 MHz UART clock) for the commonly used baud rates:

0x4 = 1152000

OxC = 38400

Ox18 = 192000

0x20 = 14400

0x30 = 9600

Initialise the UART

(2). Write to Line Control register to specify the number of bits per char and parity, e.g. 8 bits per char with no parity.

(3). Write to Interrupt Mask register to enable/disable RX and TX interrupts

Initialise the UART

When using the emulated ARM Versatilepb board, it seems that QEMU automatically uses default values for both baud rate and line control parameters, making steps (1) and (2) either optional or unnecessary.

For the emulated Versatilepb board, all we need to do is to program the Interrupt Mask register (if using interrupts) and check the Flag register during serial 1/0.

UART Data register

0x00 UARTDR - Data register: for read/write chars

To begin with, we shall implement the UART I/O by polling, which only checks the Flag status register.

We read from the data register when the flag register indicates that there is data available

We write to the data register when the flag register indicates that there is no to be trasmitted

Flag Register

7	6	5	4	3
TXFE	RXFF	TXFF	RXFE	BUSY

Where TXFE= Tx buffer empty

RXFF=Rx buffer full

TXFF=Tx buffer full

RXFE = Rx buffer empty

BUSY = device is busy

UART Flag register

3.3.3 Flag register, UARTFR

The UARTFR register is the flag register. After reset TXFF, RXFF, and BUSY are 0, and TXFE and RXFE are 1. Table 3-4 shows the bit assignment of the UARTFR register.

Table 3-4 UARTFR register

Bits	Name	Function
15:9	-	Reserved, do not modify, read as zero.
8	RI	Ring indicator. This bit is the complement of the UART ring indicator (**nUARTRI**) modem status input. That is, the bit is 1 when the modem status input is 0.
7	TXFE	Transmit FIFO empty. The meaning of this bit depends on the state of the FEN bit in the UARTLCR_H register. If the FIFO is disabled, this bit is set when the transmit holding register is empty. If the FIFO is enabled, the TXFE bit is set when the transmit FIFO is empty. This bit does not indicate if there is data in the transmit shift register.
6	RXFF	Receive FIFO full. The meaning of this bit depends on the state of the FEN bit in the UARTLCR_H register. If the FIFO is disabled, this bit is set when the receive holding register is full. If the FIFO is enabled, the RXFF bit is set when the receive FIFO is full.
5	TXFF	Transmit FIFO full. The meaning of this bit depends on the state of the FEN bit in the UARTLCR_H register. If the FIFO is disabled, this bit is set when the transmit holding register is full. If the FIFO is enabled, the TXFF bit is set when the transmit FIFO is full.
4	RXFE	Receive FIFO empty. The meaning of this bit depends on the state of the FEN bit in the UARTLCR_H register. If the FIFO is disabled, this bit is set when the receive holding register is empty.

Read a char from the uart Data Register

RXFE Receive FIFO empty

- the RXFE bit is set when the receive FIFO is empty.

```
int ugetc(UART *up)
{
// loop while the receive buffer is empty
  while( (up->FR) & 0x10);

// read the char when the RXFE bit goes to 0
  return (char)((up->DR) & 0xFF);
}
```

Write a char to UART Data Register

```
 int uputc(UART *up, char c)
{
  // loop while the transmit buffer is full
  while((up->FR & 0x20));
// send the char
  (up->DR) = (int)c;
}
```