LCD controller on the Versatile board

The ARM Versatile board supports a color LCD display.

The versatile board uses the ARM PL110 Color LCD controller .

On the versatile board the LCD controller is at the base address 0x10120020.

Table 4-22 from the Versatile Application Baseboard manual

Table 4-22 CLCDC implementation

Property	Value
Location	ARM926PXP development chip
Memory base address	`0x10120000` **Note** There are also a LCD power control register at `0x10000050`. See *CLCD Control Register, SYS_CLCD* on page 4-28.
Interrupt	16 on PIC
DMA	NA
Release version	ARM CLCDC PL110 r0p0-00alp0
Reference documentation	*ARM PrimeCell Color LCD Controller (PL110) Technical Reference Manual* (see also address modifications listed in *PrimeCell modifications* on page 4-35, *Display resolutions and display memory organization* on page 4-35, and *CLCDC interface* on page 3-40)

PL110 registers

The PrimeCell Color LCD Controller (PL110)

Technical Reference Manual gives the register layout of the lcd controller

The PrimeCell LCD Controller registers are shown in Table 3-1 of the technical reference manual.

For example the LCDTiming0 register is at 0x10120020 and the LCDControl register is at an offset of 0x1C from the base register address.

Table 3-1 PrimeCell CLCDC register summary

Address offset	Type	Width	Reset value	Name	Description
0x00	Read/write	32	0x00000000	LCDTiming0	See *Horizontal Axis Panel Control Register, LCDTiming0* on page 3-4
0x004	Read/write	32	0x00000000	LCDTiming1	See *Vertical Axis Panel Control Register, LCDTiming1* on page 3-5
0x08	Read/write	32	0x00000000	LCDTiming2	See *Clock and Signal Polarity Control Register, LCDTiming2* on page 3-7
0x0C	Read/write	17	0x00000	LCDTiming3	See *Line End Control Register, LCDTiming3* on page 3-9
0x010	Read/write	32	0x0000000	LCDUPBASE	See *Upper and Lower Panel Frame Base Address Registers, LCDUPBASE and LCDLPBASE* on page 3-9
0x14	Read/write	32	0x00000000	LCDLPBASE	See *Upper and Lower Panel Frame Base Address Registers, LCDUPBASE and LCDLPBASE* on page 3-9
0x18	Read/write	5	0x00	LCDIMSC	See *Interrupt Mask Set/Clear Register, LCDIMSC* on page 3-10
0x1C	Read/write	16	0x0000	LCDControl	See *Control Register, LCDControl* on page 3-11
0x20	Read	5	0x00	LCDRIS	See *Raw Interrupt Status Register, LCDRIS* on page 3-13
0x024	Read	5	0x00	LCDMIS	See *Masked Interrupt Status Register, LCDMIS* on page 3-13

LCD Controller

The LCD controller has several timing and control registers, which can be programmed to provide different display modes and resolutions.

To use the LCD display the controller's timing and control registers must be set up properly.

ARM Versatile Application Baseboard manual provides the following timing register settings for VGA and SVGA modes.

Timing registers

Table 4-24 Values for different display resolutions

Display resolution for external monitors	CLCDCLK frequency and SYS_OSC1 register value	CLCD_TIM0 register at 0x10120000	CLCD_TIM1 register 0x10120004	CLCD_TIM2 register at 0x10120008
QVGA(240x320) (portrait) on VGA	25MHz, 0x2C77	0xC7A7BF38	0x595B613F	0x04eF1800
QVGA (320x240) (landscape) on VGA	25MHz, 0x2C77	0x9F7FBF4C	0x818360eF	0x053F1800
QCIF (176x220) (portrait) on VGA	25MHz, 0x2C77	0xe7C7BF28	0x8B8D60DB	0x04AF1800
VGA (640x480) on VGA	25MHz, 0x2C77	0x3F1F3F9C	0x090B61DF	0x067F1800
SVGA (800x600) on SVGA	36MHz, 0x2CAC	0x1313A4C4	0x0505F657	0x071F1800

0x1000001c CLCDCLK

0x1000001c CLCDCLK

The clock frequency for the lcd controller is also set according to table Table 4-24

```
*(volatile unsigned int *)(0x1000001c) = 0x2C77;
```

Lcd example fbuf_init function

```
int fbuf_init()

                    /*********  for  640x480
**********************/
        *(volatile unsigned int *)(0x1000001c) =
0x2C77;
        *(volatile unsigned int *)(0x10120000) =
0x3F1F3F9C;
        *(volatile unsigned int *)(0x10120004) =
0x090B61DF;
        *(volatile unsigned int *)(0x10120008) =
0x067F1800;
```

framebuffer

The LCD's frame buffer address register must point to a frame buffer in memory.

Code in vid.c example C2.7

```
int fbuf_init()
{
    fb = (int *)0x200000;
*(volatile unsigned int *)(0x10120010) = 0x200000;
```

framebuffer

With 24 bits per pixel, each pixel is represented by a 32-bit integer.

The low 3 bytes of this integer are the BGR (Blue Green Red) of the pixel.

For VGA mode, the frame buffer size is 640*480 bytes. For SVGA mode the framebuffer size is 800*600

Framebuffer in vid.c

In order to support both VGA and SVGA modes, the vid.c code allocates a frame buffer of 2 MB.

Assuming that the system control program runs in the lowest 1 MB of physical memory, vid.c allocates the memory area from 2 to 4 MB for the frame buffer.

LCD Control register

The LCD control register bit assignments are detailed in table 3-9 of the PL110 TRM.

In the LCD Control register (0x1010001C), bit 0, is LCD enable and *power on* is bit 11 , both must be set to 1.

Other bits are for byte order, number of bits per pixel, mono or color mode. etc.

LCD Control register

In the LCD example code, bits3-1 are set to 101 for 24 bits per pixel, all other bits are 0s for little-Endian byte order by default.

Bit [5] TLcdTFT Read/write LCD is TFT:

0 = LCD is an STN display, use gray scaler

1 = LCD is TFT, do not use gray scaler.

1000 0010 1011

8 2 B

Code in c2.7

```
*(volatile unsigned int *)(0x10120018) = 0x82B;
```

LCD Control register

You can change the value mid-frame to enable double-buffered video displays to be created.

These registers are copied to the corresponding current registers at each LCD vertical synchronization.

This event causes the LNBU bit and an optional interrupt to be generated.

You can use the interrupt to reprogram the base address when generating double-buffered video.

Table 3-9 LCDControl Register bit assignments

Bit	Name	Type	Description
[31:17]	-	-	Reserved, do not modify, read as zero, write as zero.
[16]	WATERMARK	Read/write	LCD DMA FIFO Watermark level: 0 = **HBUSREQM** is raised when either of the two DMA FIFOs have four or more empty locations 1 = **HBUSREQM** is raised when either of the DMA FIFOs have eight or more empty locations.
[15:14]	-	-	Reserved, do not modify, read as zero, write as zero.
[13:12]	LcdVComp	Read/write	Generate interrupt at: 00 = start of vertical synchronization 01 = start of back porch 10 = start of active video 11 = start of front porch.
[11]	LcdPwr	Read/write	LCD power enable: 0 = power not gated through to LCD panel and **CLD[23:0]** signals disabled, (held LOW) 1 = power gated through to LCD panel and **CLD[23:0]** signals enabled, (active). See *LCD powering up and powering down sequence support* on page 1-5 for details on LCD power sequencing.
[10]	BEPO	Read/write	Big-endian pixel ordering within a byte: 0 = little-endian pixel ordering within a byte 1= big-endian pixel ordering within a byte. The BEPO bit selects between little and big-endian pixel packing for 1, 2, and 4 bpp display modes. It has no effect on 8 or 16 bpp pixel formats. See *Pixel serializer* on page 2-5 for more information on the data format.

Control Register at offset 0x18 in the versatile board – table 4-23 in the versatile TRM

The register map for the variant of the PL110 used in the ARM926PXP development chip is not the same as that listed for the standard PL110. The differences are listed in Table 4-23.

Table 4-23 PrimeCell CLCDC register differences

Address (Dev. Chip)	Reset value (Dev. Chip)	Description	Difference
0x10120018	0x0	LCDControl, LCD panel pixel parameters	listed as address0x1012001C in CLCDC TRM
0x1012001C	0x0	LCDIMSC, interrupt mask set and clear	listed as address 0x10120018 in CLCDC TRM
0x10120800–0x10120C2C	0x0	Not present	Hardware cursor registers from PL111 (see the *ARM926EJ-S Technical Reference Manual* for details)
0x10120FE0	0x93	CLCDPeriphID0	listed as 0x10 in CLCDC TRM
0x10120FE4	0x10	CLCDPeriphID1	listed as 0x11 in CLCDC TRM